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1. FEATURES

- Interface: HyperBus
- Power supply: 1.7V~2.0V
- Maximum clock rate: 200MHz
- Double-Data Rate (DDR) Up to 400 MT/s
- Clock:
  - Single ended clock (CK)
  - Differential clock (CK/CK#)
- Chip Select (CS#)
- 8-bit data bus (DQ[7:0])
- Hardware reset (RESET#)
- Read-Write Data Strobe (RWDS)
  - Bidirectional Data Strobe / Mask
  - Output at the start of all transactions to indicate refresh latency
  - Output during read transactions as Read Data Strobe
  - Input during write transactions as Write Data Mask

Performance and Power

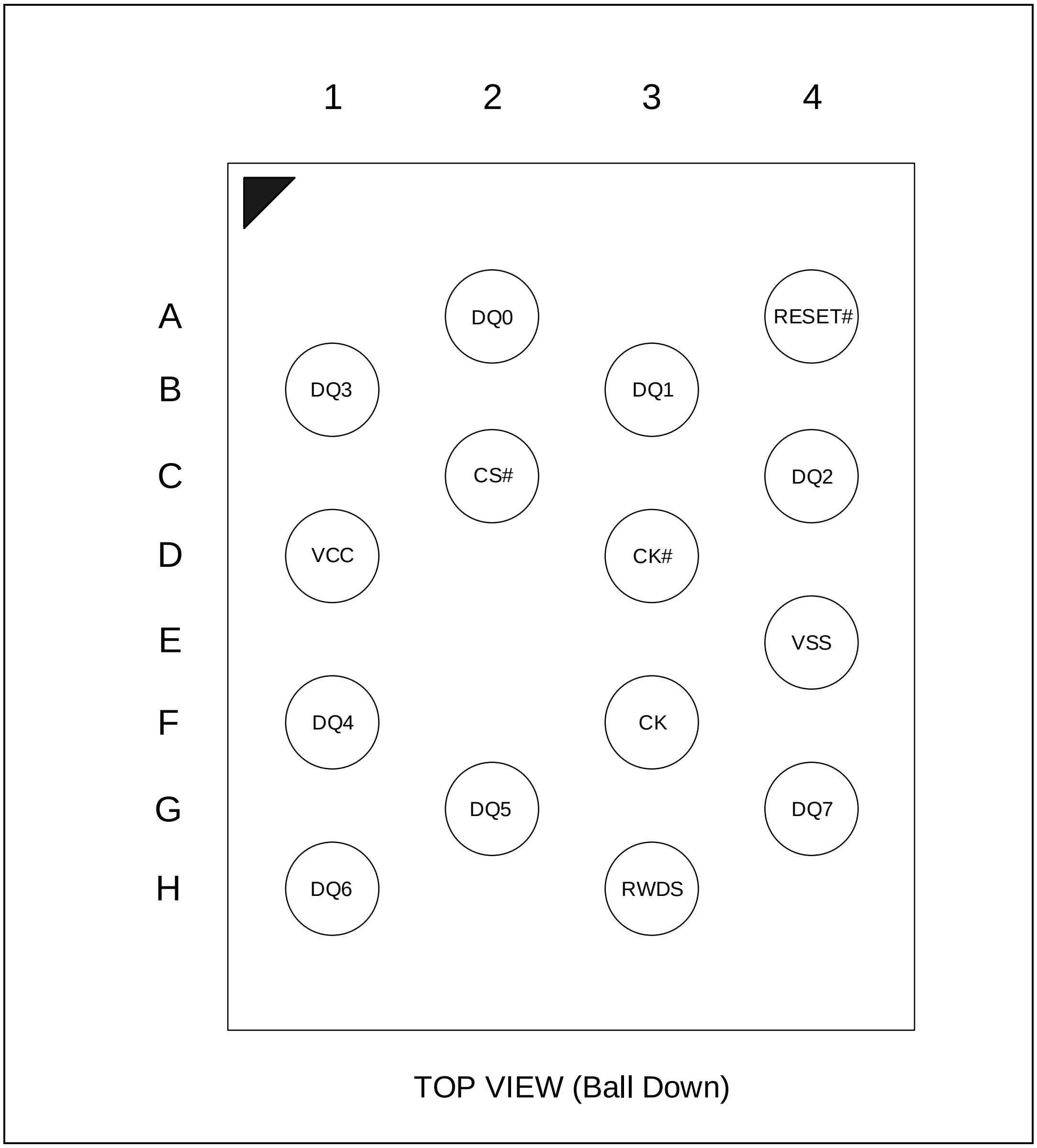
- Configurable output drive strength
- Power Saving Modes
  - Hybrid Sleep Mode
  - Deep Power Down
- Configurable Burst Characteristics
  - Linear burst
  - Wrapped burst lengths:
    - 16 bytes (8 clocks)
    - 32 bytes (16 clocks)
    - 64 bytes (32 clocks)
    - 128 bytes (64 clocks)
  - Hybrid burst - one wrapped burst followed by linear burst
- Array Refresh Modes
  - Full Array Refresh
  - Partial Array Refresh
- Operating temperature range:

  -40°C ≤ TCASE ≤ 85°C

2. ORDER INFORMATION

Part Number	VCC/VCCQ	I/O Width	Interface	Others
W956D8MWSX5I	1.8V	8	HyperBus	WLCSP 15 ball, 200MHz, -40°C~85°C

3. BALL ASSIGNMENT


1
2
3
4
A
B
C
D
E
F
G
H
DQ0
RESET#
DQ3
DQ1
CS#
DQ2
VCC
CK#
VSS
DQ4
CK
DQ5
DQ7
DQ6
RWDS
TOP VIEW (Ball Down)

WLCSP 15 Balls, Top View

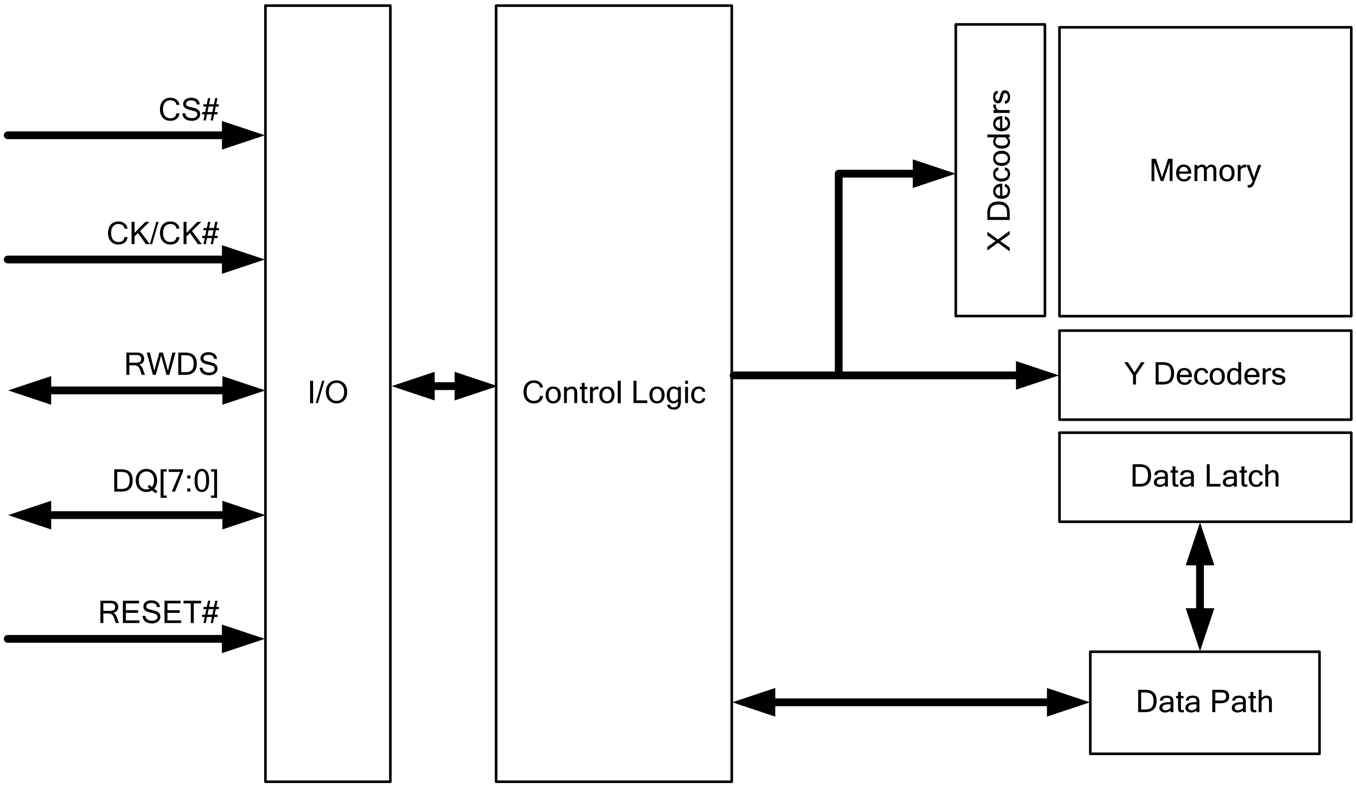
Notes:

1. The VCCQ mentioned in this datasheet is internally shorted to VCC.
2. The VSSQ mentioned in this datasheet is internally shorted to VSS.

4. BALL DESCRIPTIONS

Signal Name	Type	Description
CS#	Input	**Chip Select:** Bus transactions are initiated with a High to Low transition. Bus transactions are terminated with a Low to High transition. The master device has a separate CS# for each slave.
CK, CK#	Input	**Differential Clock:** Command, address, and data information is output with respect to the crossing of the CK and CK# signals. **Single Ended Clock:** CK# is not used, only a single ended CK is used. The clock is not required to be free-running.
DQ[7:0]	Input / Output	**Data Input / Output:** Command, Address, and Data information is transferred on these signals during Read and Write transactions.
RWDS	Input / Output	**Read Write Data Strobe:** During the Command/Address portion of all bus transactions RWDS is a slave output and indicates whether additional initial latency is required. Slave output during read data transfer, data is edge aligned with RWDS. Slave input during data transfer in write transactions to function as a data mask. (High = additional latency, Low = no additional latency).
RESET#	Input, Internal Pull-up	**Hardware Reset:** When Low the slave device will self-initialize and return to the Standby state. RWDS and DQ[7:0] are placed into the High-Z state when RESET# is Low. The slave RESET# input includes a weak pull-up, if RESET# is left unconnected it will be pulled up to the High state. **Note:** The RESET# pin is maximum 4V tolerant.
VCC	Power Supply	**VCC Power Supply:** For supplying input buffer of CK, CK#, CS#, RESET#, DQ[7:0], RWDS, internal circuitry and memory array.
VSS	Power Supply	**VSS Ground:** Ground of VCC.

5. BLOCK DIAGRAM


CS#
CK/CK#
RWDS
DQ[7:0]
RESET#
I/O
Control Logic
X Decoders
Memory
Y Decoders
Data Latch
Data Path

6. FUNCTIONAL DESCRIPTION

6.1 HyperBus Interface

HyperBus is a low signal count, Double Data Rate (DDR) interface, that achieves high speed read and write throughput. The DDR protocol transfers two data bytes per clock cycle on the DQ input/output signals. A read or write transaction on HyperBus consists of a series of 16-bit wide, one clock cycle data transfers at the internal HyperRAM array with two corresponding 8-bit wide, one-half-clock-cycle data transfers on the DQ signals. All inputs and outputs are LV-CMOS compatible.

Command, address, and data information is transferred over the eight HyperBus DQ[7:0] signals. The clock (CK#, CK) is used for information capture by a HyperBus slave device when receiving command, address, or data on the DQ signals. Command or Address values are center aligned with clock transitions.

Every transaction begins with the assertion of CS# and Command-Address (CA) signals, followed by the start of clock transitions to transfer six CA bytes, followed by initial access latency and either read or write data transfers, until CS# is de-asserted.

Read and write transactions require two clock cycles to define the target row address and burst type, then an initial access latency of t_{ACC}. During the CA part of a transaction, the memory will indicate whether an additional latency for a required refresh time (t_{RFH}) is added to the initial latency; by driving the RWDS signal to the High state. During the CA period the third clock cycle will specify the target word address within the target row. During a read (or write) transaction, after the initial data value has been output (or input), additional data can be read from (or written to) the row on subsequent clock cycles in either a wrapped or linear sequenced. When configured in linear burst mode, the device will automatically fetch the next sequential row from the memory array to support a continuous linear burst. Simultaneously accessing the next row in the array while the read or write data transfer is in progress, allows for a linear sequential burst operation that can provide a sustained data rate of 400 MB/s (1 byte (8 bit data bus) * 2 (data clock edges) * 200 MHz = 400 MB/s).

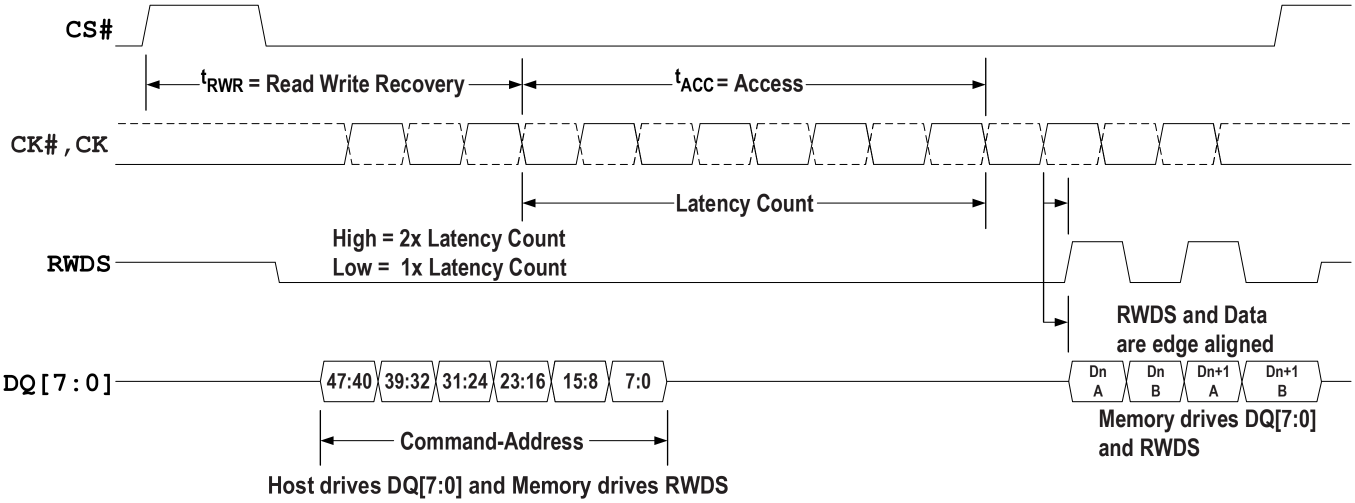

CS#
tRWR = Read Write Recovery
tACC = Access
CK#,CK
Latency Count
RWDS
High = 2x Latency Count
Low = 1x Latency Count
RWDS and Data
are edge aligned
DQ[7:0]
47:40
39:32
31:24
23:16
15:8
7:0
Dn A
Dn B
Dn+1 A
Dn+1 B
Command-Address
Host drives DQ[7:0] and Memory drives RWDS
Memory drives DQ[7:0] and RWDS

Figure 1 - Read Transaction, Single Initial Latency Count

The Read/Write Data Strobe (RWDS) is a bidirectional signal that indicates:

- When data will start to transfer from a HyperRAM device to the master device in read transactions (initial read latency)
- When data is being transferred from a HyperRAM device to the master device during read transactions (as a source synchronous read data strobe)
- When data may start to transfer from the master device to a HyperRAM device in write transactions (initial write latency)
- Data masking during write data transfers

During the CA transfer portion of a read or write transaction, RWDS acts as an output from a HyperRAM device to indicate whether additional initial access latency is needed in the transaction.

During read data transfers, RWDS is a read data strobe with data values edge aligned with the transitions of RWDS.

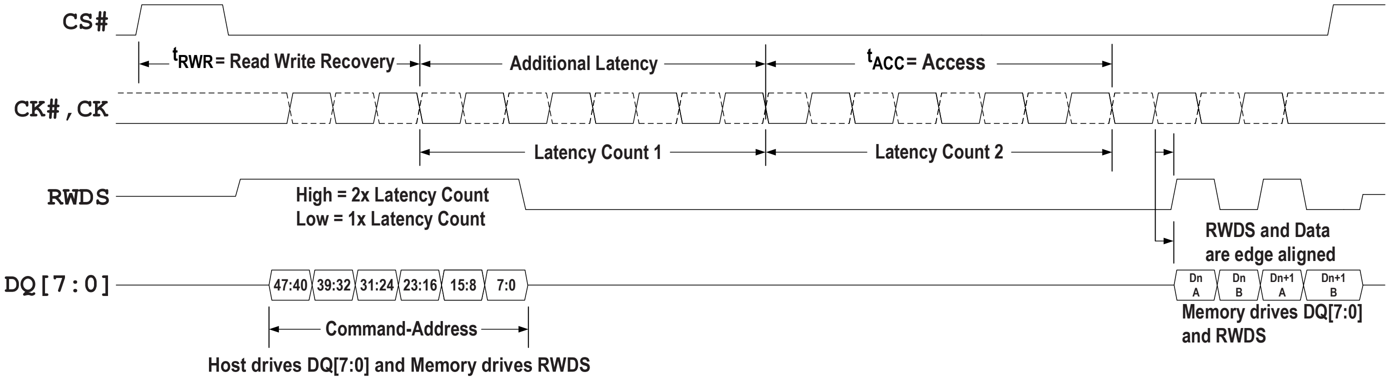

CS#
tRWR = Read Write Recovery
Additional Latency
tACC = Access
CK#,CK
Latency Count 1
Latency Count 2
RWDS
High = 2x Latency Count
Low = 1x Latency Count
RWDS and Data are edge aligned
DQ[7:0]
47:40
39:32
31:24
23:16
15:8
7:0
Dn A
Dn B
Dn+1 A
Dn+1 B
Memory drives DQ[7:0] and RWDS
Command-Address
Host drives DQ[7:0] and Memory drives RWDS

Figure 2 - Read Transaction, Additional Latency Count

During write data transfers, RWDS indicates whether each data byte transfer is masked with RWDS High (invalid and prevented from changing the byte location in a memory) or not masked with RWDS Low (valid and written to a memory). Data masking may be used by the host to byte align write data within a memory or to enable merging of multiple non-word aligned writes in a single burst write. During write transactions, data is center aligned with clock transitions.

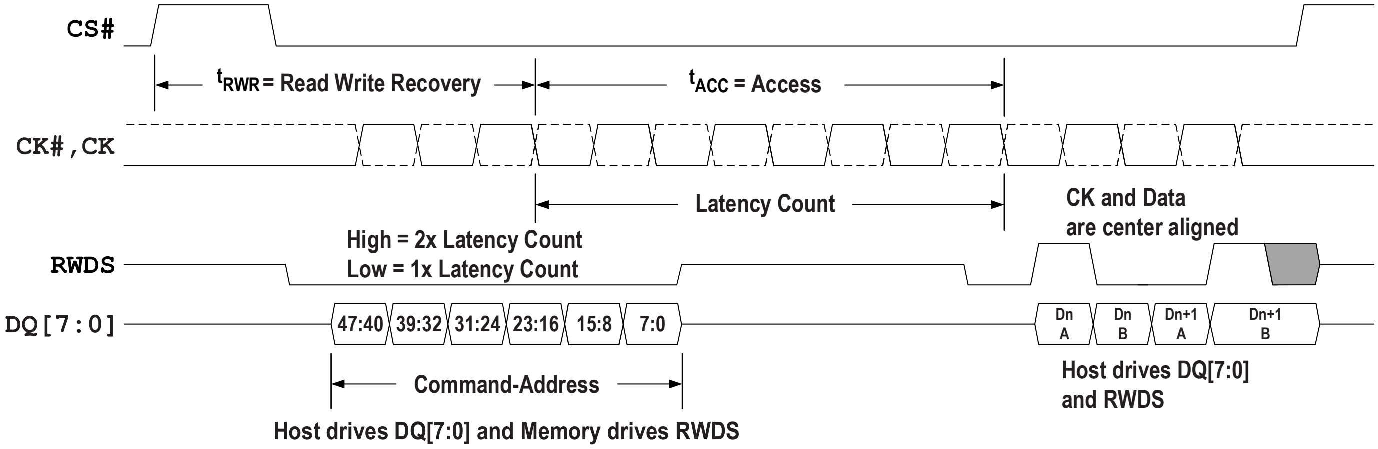

CS#
tRWR = Read Write Recovery
tACC = Access
CK#,CK
Latency Count
CK and Data are center aligned
High = 2x Latency Count
Low = 1x Latency Count
RWDS
DQ[7:0]
47:40
39:32
31:24
23:16
15:8
7:0
Dn A
Dn B
Dn+1 A
Dn+1 B
Host drives DQ[7:0] and RWDS
Command-Address
Host drives DQ[7:0] and Memory drives RWDS

Figure3 - Write Transaction, Single Initial Latency Count

Note: The last write data can be masked or not masked.

Read and write transactions are burst oriented, transferring the next sequential word during each clock cycle. Each individual read or write transaction can use either a wrapped or linear burst sequence.

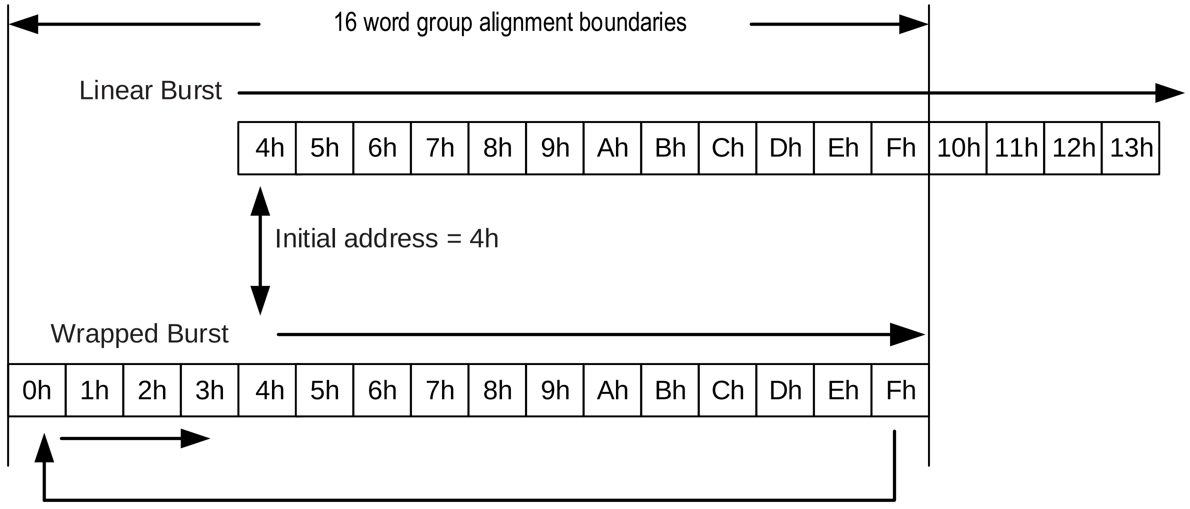

16 word group alignment boundaries
Linear Burst
4h
5h
6h
7h
8h
9h
Ah
Bh
Ch
Dh
Eh
Fh
10h
11h
12h
13h
Initial address = 4h
Wrapped Burst
0h
1h
2h
3h
4h
5h
6h
7h
8h
9h
Ah
Bh
Ch
Dh
Eh
Fh

Figure 4 - Linear Versus Wrapped Burst Sequence

During wrapped transactions, accesses start at a selected location and continue to the end of a configured word group aligned boundary, then wrap to the beginning location in the group, then continue back to the starting location. Wrapped bursts are generally used for critical word first cache line fill read transactions. During linear transactions, accesses start at a selected location and continue in a sequential manner until the transaction is terminated when CS# returns High. Linear transactions are generally used for large contiguous data transfers such as graphic images. Since each transaction command selects the type of burst sequence for that transaction, wrapped and linear bursts transactions can be dynamically intermixed as needed.

7. HYPERBUS TRANSACTION DETAILS

7.1 Command/Address Bit Assignments

All HyperRAM bus transactions can be classified as either read or write. A bus transaction is started with CS# going Low with clock in idle state (CK=Low and CK#=High). The first three clock cycles transfer three words of Command/Address (CA0, CA1, CA2) information to define the transaction characteristics. The Command/Address words are presented with DDR timing, using the first six clock edges. The following characteristics are defined by the Command/Address information:

- Read or Write transaction
- Address Space: memory array space or register space
  - Register space is used to access Device Identification (ID) registers and Configuration Registers (CR) that identify the device characteristics and determine the slave specific behavior of read and write transfers on the HyperBus interface.
- Whether a transaction will use a linear or wrapped burst sequence
- The target row (and half-page) address (upper order address)
- The target column (word within half-page) address (lower order address)

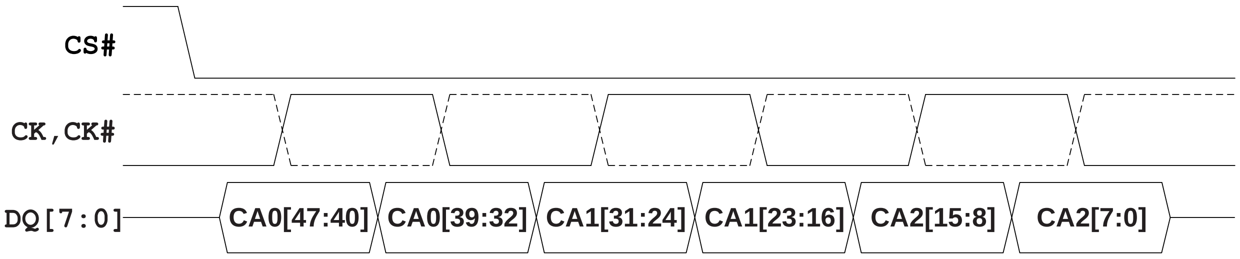


Figure 5 - Command-Address (CA) Sequence

Notes:

1. Figure shows the initial three clock cycles of all transactions on the HyperBus.
2. CK# of differential clock is shown as dashed line waveform.
3. CA information is “center aligned” with the clock during both Read and Write transactions.
4. Data bits in each byte are always in high to low order with bit 7 on DQ7 and bit 0 on DQ0.

Table 1 - CA Bit Assignment to DQ Signals

Signal	CA0[47:40]	CA0[39:32]	CA1[31:24]	CA1[23:16]	CA2[15:8]	CA2[7:0]
DQ[7]	CA[47]	CA[39]	CA[31]	CA[23]	CA[15]	CA[7]
DQ[6]	CA[46]	CA[38]	CA[30]	CA[22]	CA[14]	CA[6]
DQ[5]	CA[45]	CA[37]	CA[29]	CA[21]	CA[13]	CA[5]
DQ[4]	CA[44]	CA[36]	CA[28]	CA[20]	CA[12]	CA[4]
DQ[3]	CA[43]	CA[35]	CA[27]	CA[19]	CA[11]	CA[3]
DQ[2]	CA[42]	CA[34]	CA[26]	CA[18]	CA[10]	CA[2]
DQ[1]	CA[41]	CA[33]	CA[25]	CA[17]	CA[9]	CA[1]
DQ[0]	CA[40]	CA[32]	CA[24]	CA[16]	CA[8]	CA[0]

Table 2 - Command/Address Bit Assignments

CA Bit#	Bit Name	Bit Function
47	R/W#	Identifies the transaction as a read or write. R/W#=1 indicates a Read transaction R/W#=0 indicates a Write transaction
46	Address Space (AS)	Indicates whether the read or write transaction accesses the memory or register space. AS=0 indicates memory space AS=1 indicates the register space The register space is used to access device ID and Configuration registers.
45	Burst Type	Indicates whether the burst will be linear or wrapped. Burst Type=0 indicates wrapped burst Burst Type=1 indicates linear burst
44-16	Row & Upper Column Address	Row & Upper Column component of the target address: System word address bits A31-A3 Any upper Row address bits not used by a particular device density should be set to 0 by the host controller master interface. The size of Rows and therefore the address bit boundary between Row and Column address is slave device dependent.
15-3	Reserved	Reserved for future column address expansion. Reserved bits are don’t care in current HyperBus devices but should be set to 0 by the host controller master interface for future compatibility.
2-0	Lower Column Address	Lower Column component of the target address: System word address bits A2-A0 selecting the starting word within a half-page.

Notes:

1. The Column address selects the burst transaction starting word location within a Row. The Column address is split into an upper and lower portion. The upper portion selects an 8-word (16-byte) Half-page and the lower portion selects the word within a Half-page where a read or write transaction burst starts.
2. The initial read access time starts when the Row and Upper Column (Half-page) address bits are captured by a slave interface. Continuous linear read burst is enabled by memory devices internally interleaving access to 16 byte half-pages.
3. HyperBus protocol address space limit, assuming:
   29 Row &Upper Column address bits
   3 Lower Column address bits
   Each address selects a word wide (16 bit = 2 byte) data value
   29 + 3 = 32 address bits = 4G addresses supporting 8Gbyte (64Gbit) maximum address space

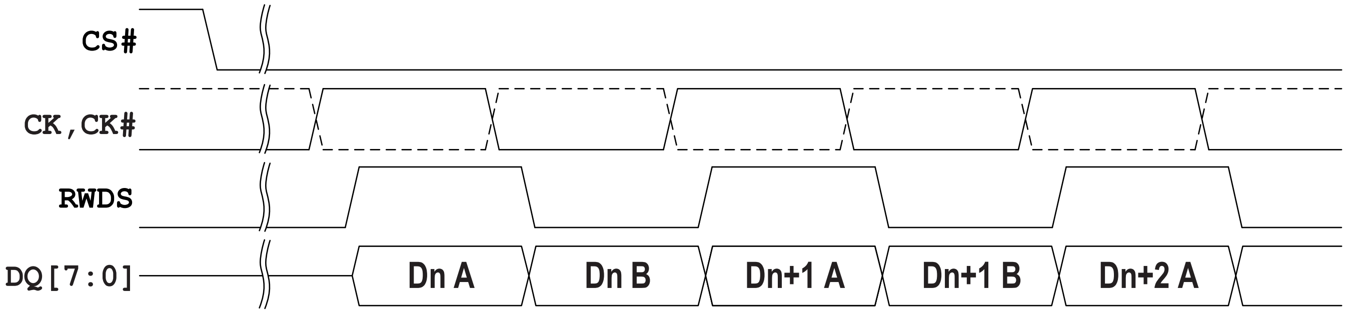


Figure 6 - Data Placement during a Read Transaction

Notes:

1. Figure shows a portion of a Read transaction on the HyperBus. CK# of differential clock is shown as dashed line waveform.
2. Data is “edge aligned” with the RWDS serving as a read data strobe during read transactions.
3. Data is always transferred in full word increments (word granularity transfers).
4. Word address increments in each clock cycle. Byte A is between RWDS rising and falling edges and is followed by byte B between RWDS falling and rising edges, of each word.
5. Data bits in each byte are always in high to low order with bit 7 on DQ7 and bit 0 on DQ0.

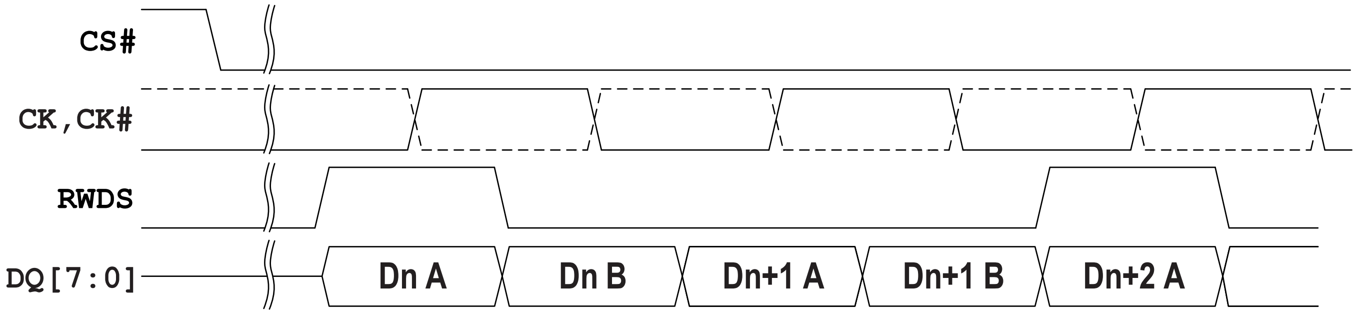


Figure 7 - Data Placement during a Write Transaction

Notes:

1. Figure shows a portion of a Write transaction on the HyperBus.
2. Data is “center aligned” with the clock during a Write transaction.
3. RWDS functions as a data mask during write data transfers with initial latency. Masking of the first and last byte is shown to illustrate an unaligned 3 byte write of data.
4. RWDS is not driven by the master during write data transfers with zero initial latency. Full data words are always written in this case. RWDS may be driven Low or left High-Z by the slave in this case.

7.2 Read Transactions

The HyperBus master begins a transaction by driving CS# Low while clock is idle. The clock then begins toggling while CA words are transferred.

In CA0, CA[47] = 1 indicates that a Read transaction is to be performed. CA[46] = 0 indicates the memory space is being read or CA[46] = 1 indicates the register space is being read. CA[45] indicates the burst type (wrapped or linear). Read transactions can begin the internal array access as soon as the row and upper column address has been presented in CA0 and CA1 (CA[47:16]). CA2 (CA(15:0]) identifies the target Word address within the chosen row.

The HyperBus master then continues clocking for a number of cycles defined by the latency count setting in Configuration Register 0. The initial latency count required for a particular clock frequency is based on RWDS. If RWDS is Low during the CA cycles, one latency count is inserted. If RWDS is High during the CA cycles, an additional latency count is inserted. Once these latency clocks have been completed the memory starts to simultaneously transition the Read-Write Data Strobe (RWDS) and output the target data.

New data is output edge aligned with every transition of RWDS. Data will continue to be output as long as the host continues to transition the clock while CS# is Low. However, the HyperRAM device may stop RWDS transitions with RWDS Low, between the deliveries of words, in order to insert latency between words when crossing memory array boundaries.

Wrapped bursts will continue to wrap within the burst length and linear burst will output data in a sequential manner across row boundaries. When a linear burst read reaches the last address in the array, continuing the burst beyond the last address will provide data from the beginning of the address range. Read transfers can be ended at any time by bringing CS# High when the clock is idle.

The clock is not required to be free-running. The clock may remain idle while CS# is High.

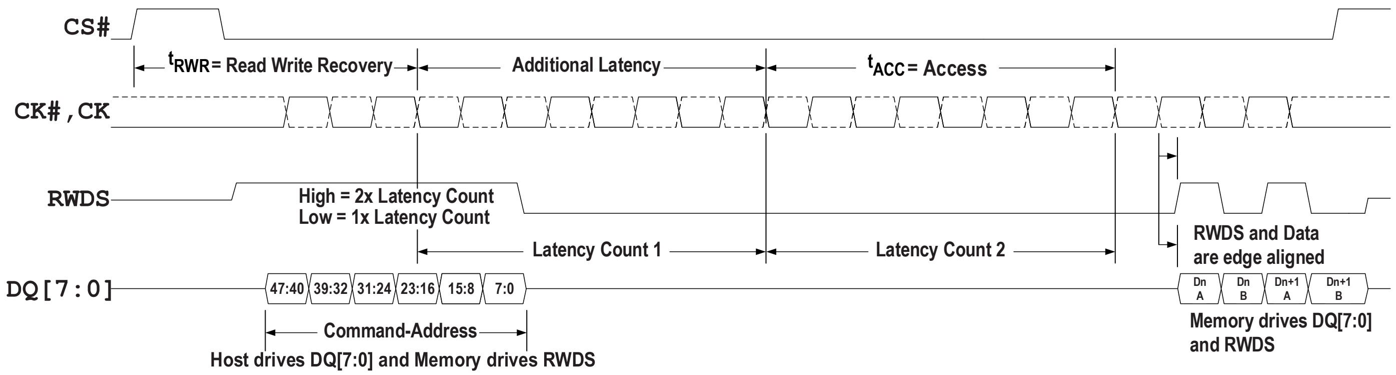

CS#
tRWR = Read Write Recovery
Additional Latency
tACC = Access
CK#,CK
RWDS
High = 2x Latency Count
Low = 1x Latency Count
Latency Count 1
Latency Count 2
RWDS and Data are edge aligned
DQ[7:0]
47:40
39:32
31:24
23:16
15:8
7:0
Dn A
Dn B
Dn+1 A
Dn+1 B
Command-Address
Host drives DQ[7:0] and Memory drives RWDS
Memory drives DQ[7:0] and RWDS

Figure 8 - Read Transaction with Additional Initial Latency

Notes:

1. Transactions are initiated with CS# falling while CK=Low and CK#=High.
2. CS# must return High before a new transaction is initiated.
3. CK# is the complement of the CK signal.CK# of a differential clock is shown as a dashed line waveform.
4. Read access array starts once CA[23:16] is captured.
5. The read latency is defined by the initial latency value in a configuration register.
6. In this read transaction example the initial latency count was set to four clocks.
7. In this read transaction a RWDS High indication during CA delays output of target data by an additional four clocks.
8. The memory device drives RWDS during read transactions.
9. **For register read, the output data Dn A is RG[15:8], Dn B is RG[7:0], Dn+1 A is RG[15:8], Dn+1 B is RG[7:0].**

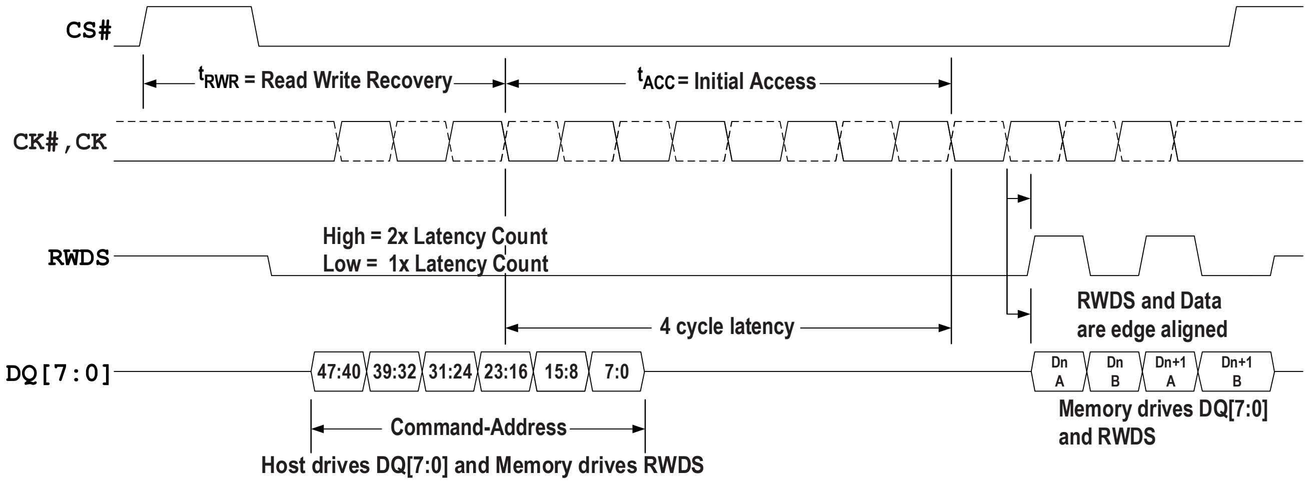

CS#
tRWR = Read Write Recovery
tACC = Initial Access
CK#,CK
RWDS
High = 2x Latency Count
Low = 1x Latency Count
RWDS and Data
are edge aligned
4 cycle latency
DQ[7:0]
47:40
39:32
31:24
23:16
15:8
7:0
Dn A
Dn B
Dn+1 A
Dn+1 B
Memory drives DQ[7:0]
and RWDS
Command-Address
Host drives DQ[7:0] and Memory drives RWDS

Figure 9 - Read Transaction without Additional Initial Latency

Note:

1. RWDS is Low during the CA cycles. In this Read Transaction there is a single initial latency count for read data access because, this read transaction does not begin at a time when additional latency is required by the slave.
2. **For register read, the output data Dn A is RG[15:8], Dn B is RG[7:0], Dn+1 A is RG[15:8], Dn+1 B is RG[7:0].**

7.3 Write Transactions (Memory Array Write)

The HyperBus master begins a transaction by driving CS# Low while clock is idle. Then the clock begins toggling while CA words are transferred.

In CA0, CA[47] = 0 indicates that a Write transaction is to be performed. CA[46] = 0 indicates the memory space is being written. CA[45] indicates the burst type (wrapped or linear). Write transactions can begin the internal array access as soon as the row and upper column address has been presented in CA0 and CA1 (CA[47:16]). CA2 (CA(15:0]) identifies the target word address within the chosen row.

The HyperBus master then continues clocking for a number of cycles defined by the latency count setting in configuration register 0. The initial latency count required for a particular clock frequency is based on RWDS. If RWDS is Low during the CA cycles, one latency count is inserted. If RWDS is High during the CA cycles, an additional latency count is inserted.

Once these latency clocks have been completed the HyperBus master starts to output the target data. Write data is center aligned with the clock edges. The first byte of data in each word is captured by the memory on the rising edge of CK and the second byte is captured on the falling edge of CK.

During the CA clock cycles, RWDS is driven by the memory.

During the write data transfers, RWDS is driven by the host master interface as a data mask. When data is being written and RWDS is High the byte will be masked and the array will not be altered. When data is being written and RWDS is Low the data will be placed into the array. Because the master is driving RWDS during write data transfers, neither the master nor the HyperRAM device is able to indicate a need for latency within the data transfer portion of a write transaction. The acceptable write data burst length setting is also shown in configuration register 0.

Data will continue to be transferred as long as the HyperBus master continues to transition the clock while CS# is Low. Legacy format wrapped bursts will continue to wrap within the burst length. Hybrid wrap will wrap once then switch to linear burst starting at the next wrap boundary. Linear burst accepts data in a sequential manner across page boundaries. Write transfers can be ended at any time by bringing CS# High when the clock is idle.

When a linear burst write reaches the last address in the memory array space, continuing the burst will write to the beginning of the address range.

The clock is not required to be free-running. The clock may remain idle while CS# is High.

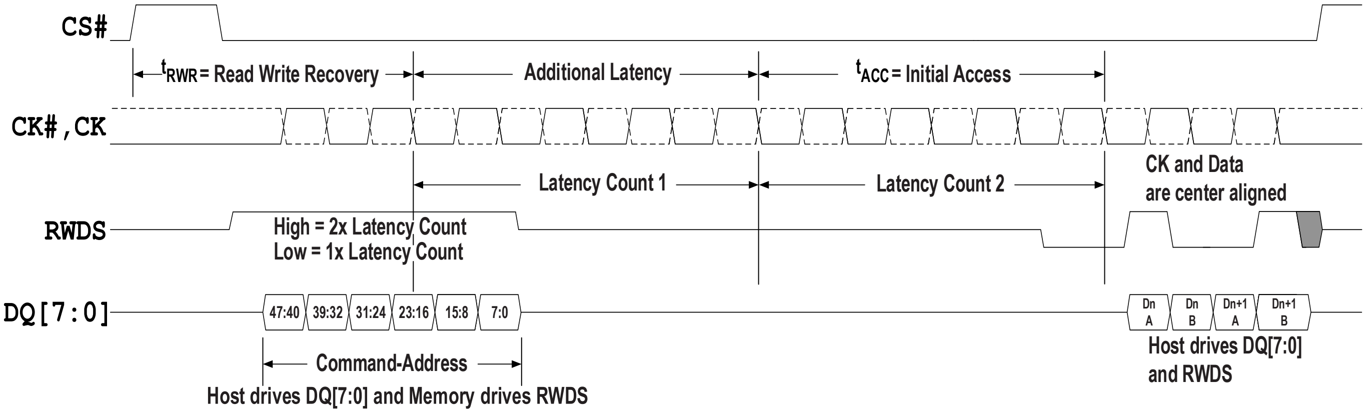

CS#
tRWR = Read Write Recovery
Additional Latency
tACC = Initial Access
CK#,CK
Latency Count 1
Latency Count 2
CK and Data are center aligned
RWDS
High = 2x Latency Count
Low = 1x Latency Count
DQ[7:0]
47:40
39:32
31:24
23:16
15:8
7:0
Dn A
Dn B
Dn+1 A
Dn+1 B
Command-Address
Host drives DQ[7:0] and Memory drives RWDS
Host drives DQ[7:0] and RWDS

Figure 10 - Write Transaction with Additional Initial Latency

Notes:

1. Transactions must be initiated with CK=Low and CK#=High.
2. CS# must return High before a new transaction is initiated.
3. During CA, RWDS is driven by the memory and indicates whether additional latency cycles are required.
4. In this example, RWDS indicates that additional initial latency cycles are required.
5. At the end of CA cycles the memory stops driving RWDS to allow the host HyperBus master to begin driving RWDS. The master must drive RWDS to a valid Low before the end of the initial latency to provide a data mask preamble period to the slave.
6. During data transfer, RWDS is driven by the host to indicate which bytes of data should be either masked or loaded into the array.
7. The figure shows RWDS masking byte Dn A and byte Dn+1 B to perform an unaligned word write to bytes Dn B and Dn+1 A.

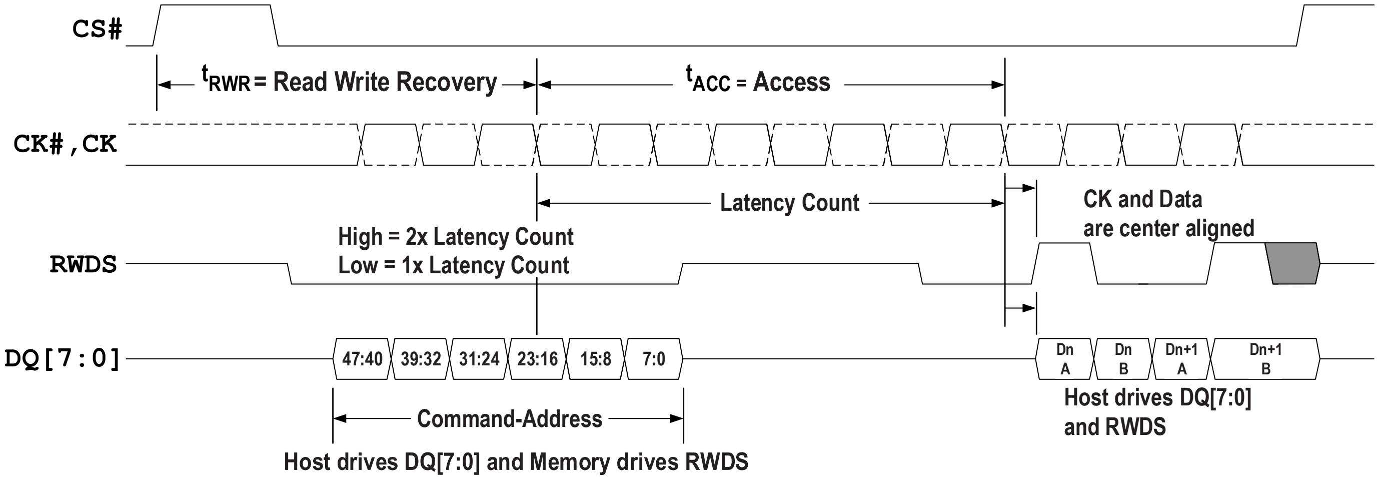

CS#
tRWR = Read Write Recovery
tACC = Access
CK#,CK
Latency Count
CK and Data are center aligned
RWDS
High = 2x Latency Count
Low = 1x Latency Count
DQ[7:0]
47:40
39:32
31:24
23:16
15:8
7:0
Dn A
Dn B
Dn+1 A
Dn+1 B
Command-Address
Host drives DQ[7:0] and Memory drives RWDS
Host drives DQ[7:0] and RWDS

Figure 11 - Write Transaction without Additional Initial Latency

Notes:

1. During CA, RWDS is driven by the memory and indicates whether additional latency cycles are required.
2. In this example, RWDS indicates that there is no additional latency required.
3. At the end of CA cycles the memory stops driving RWDS to allow the host HyperBus master to begin driving RWDS. The master must drive RWDS to a valid Low before the end of the initial latency to provide a data mask preamble period to the slave.
4. During data transfer, RWDS is driven by the host to indicate which bytes of data should be either masked or loaded into the array.
5. The figure shows RWDS masking byte Dn A and byte Dn+1 B to perform an unaligned word write to bytes Dn B and Dn+1 A.

7.4 Write Transactions without Initial Latency (Register Write)

A Write transaction starts with the first three clock cycles providing the Command/Address information indicating the transaction characteristics. CA0 may indicate that a Write transaction is to be performed and also indicates the address space and burst type (wrapped or linear).

Writes without initial latency are used for register space writes. HyperRAM device write transactions with zero latency mean that the CA cycles are followed by write data transfers. Writes with zero initial latency, do not have a turnaround period for RWDS. The HyperRAM device will always drive RWDS during the CA period to indicate whether extended latency is required for a transaction that has initial latency. However, the RWDS is driven before the HyperRAM devices has received the first byte of CA i.e. before the HyperRAM device knows whether the transaction is a read or write to register space. In the case of a write with zero latency, the RWDS state during the CA period does not affect the initial latency of zero. Since master write data immediately follows the CA period in this case, the HyperRAM device may continue to drive RWDS Low or may take RWDS to High-Z during write data transfer. The master must not drive RWDS during Writes with zero latency. Writes with zero latency do not use RWDS as a data mask function. All bytes of write data are written (full word writes).

The first byte of data in each word is presented on the rising edge of CK and the second byte is presented on the falling edge of CK. Write data is center aligned with the clock inputs. Write transfers can be ended at any time by bringing CS# High when clock is idle. The clock is not required to be free-running.

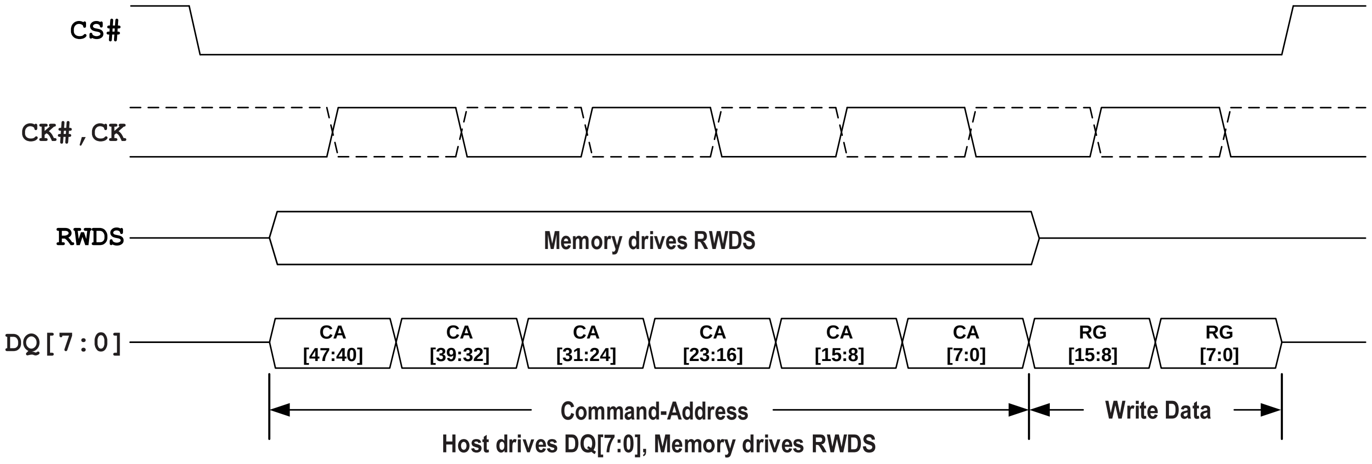


Figure 12 - Write Operation without Initial Latency

8. MEMORY SPACE

8.1 HyperBus Interface Memory Space addressing

Table 3 - Memory Space Address Map (word based - 16 bits)

Unit Type	Count	System Word Address Bits	CA Bits	Notes
Rows within 64 Mb device	8192 (Rows)	A21~A9	34~22	
Row	1 (row)	A8~A3	21~16	512 (word addresses) 1K bytes
Half-Page	8 (word addresses)	A2~A0	2~0	8 words (16 bytes)

Table 4 - Memory Space Address Map (word based - 16 bits)

		64Mb
Row Address	System Word Address Bits	A21~A9
	CA Bits	34~22
Column Address	System Word Address Bits	A8~A0
	CA Bits	21~16; 2~0
Half-Page (HP) Address	System Word Address Bits	A8~A3
	CA Bits	21~16
Word of HP Address	System Word Address Bits	A2~A0
	CA Bits	2~0

Notes:

1. Each row has 64 Half-pages. Each Half-page has 8 words. Each column has 512 words (1K bytes).
2. Half-Page address is also named as upper column address. Word of HP address is also named as lower column address.

8.1.1 Density and Row Boundaries

The DRAM array size (density) of the device can be determined from the total number of system address bits used for the row and column addresses as indicated by the Row Address Bit Count and Column Address Bit Count fields in the ID0 register. For example: a 64-Mbit HyperRAM device has 9 column address bits and 13 row address bits for a total of 22 word address bits = 2^{22} = 4M words = 8M bytes. The 9 column address bits indicate that each row holds 2^9 = 512 words = 1K bytes. The row address bit count indicates there are 8192 rows to be refreshed within each array refresh interval. The row count is used in calculating the refresh interval.

9. REGISTER SPACE

9.1 HyperBus Interface Register Addressing

Table 5 - Register Space Address Map

Register	System Address	—	—	—	31~27	26~19	18~11	10~3	—	2~0
	CA Bits	**47**	**46**	**45**	**44~40**	**39~32**	**31~24**	**23~16**	**15~8**	**7~0**
Identification Register 0 (read only)		C0h or E0h				00h	00h	00h	00h	00h
Identification Register 1 (read only)		C0h or E0h				00h	00h	00h	00h	01h
Configuration Register 0 Read		C0h or E0h				00h	01h	00h	00h	00h
Configuration Register 0 Write		60h				00h	01h	00h	00h	00h
Configuration Register 1 Read		C0h or E0h				00h	01h	00h	00h	01h
Configuration Register 1 Write		60h				00h	01h	00h	00h	01h

Notes:

1. When CA[46] is 1 a read or write transaction accesses the Register Space.
2. CA[45] may be either 0 or 1 for either wrapped or linear read. CA[45] must be 1 as only linear single word register writes are supported.
3. The Burst type (wrapped/linear) definition is not supported in Register Reads. Hence C0h/E0h have the same effect.

9.2 Register Space Access

Register default values are loaded upon power-up or hardware reset. The registers can be altered at any time while the device is in the standby state.

Loading a register is accomplished with write transaction without initial latency using a single 16-bit word write transaction.

Each register is written with a separate single word write transaction. Register write transactions have zero latency, the single word of data immediately follows the CA. RWDS is not driven by the host during the write because RWDS is always driven by the memory during the CA cycles to indicate whether a memory array refresh is in progress. Because a register space write goes directly to a register, rather than the memory array, there is no initial write latency, related to an array refresh that may be in progress. In a register write, RWDS is also not used as a data mask because both bytes of a register are always written and never masked.

Reserved register fields must be written with their default value. Writing reserved fields with other than default values may produce undefined results.

Note: The host must not drive RWDS during a write to register space.

Note: The RWDS signal is driven by the memory during the CA period based on whether the memory array is being refreshed. This refresh indication does not affect the writing of register data.

Note: The RWDS signal returns to high impedance after the CA period. Register data is never masked. Both data bytes of the register data are loaded into the selected register.

Reading of a register is accomplished with read transaction with single or double initial latency using a single 16 bit read transaction. If more than one word is read, the same register value is repeated in each word read. The contents of the register is returned in the same manner as reading array data, with one or two latency counts, based on the state of RWDS during the CA period. The latency count is defined in the Configuration Register 0 Read Latency field (CR0[7:4]).

9.3 Device Identification Registers

There are two read only, non-volatile, word registers, that provide information on the device selected when CS# is low. The device information fields identify:

- Manufacture
- Type
- Density
  – Row address bit count
  – Column address bit count

Table 6 - ID Register 0 Bit Assignments

Bits	Function	Settings (Binary)
[15:14]	Reserved	00b - (default)
[13]	Reserved	0b - (default)
[12:8]	Row Address Bit Count	01100b - The 13th row address bits
[7:4]	Column Address Bit Count	1000b - The 9th column address bits
[3:0]	Manufacturer	**0110b - Winbond**

Table 7 - ID Register 1 Bit Assignments

Bits	Function	Settings (Binary)
[15:4]	Reserved	0000_0000_0000b (default)
[3:0]	Device Type	0001b - HyperRAM 2.0 0000b, 0010b to 1111b - Reserved

9.4 Configuration Register 0

Configuration Register 0 (CR0) is used to define the power state and access protocol operating conditions for the HyperRAM device. Configurable characteristics include:

- Wrapped Burst Length (16, 32, 64, or 128 byte aligned and length data group)
- Wrapped Burst Type
  – Legacy wrapped burst (sequential access with wrap around within a selected length and aligned group)
  – Hybrid wrap (Legacy wrapped burst once then linear burst at start of the next sequential group)
- Initial Latency
- Variable Latency
  – Whether an array read or write transaction will use fixed or variable latency. If fixed latency is selected the memory will always indicate a refresh latency and delay the read data transfer accordingly. If variable latency is selected, latency for a refresh is only added when a refresh is required at the same time a new transaction is starting.
- Output Drive Strength
- Deep Power Down Mode

Table 8 - Configuration Register 0 Bit Assignments

CR0 Bit	Function	Settings (Binary)
[15]	Deep Power Down Enable	1b - Normal operation (default) 0b - Writing 0 to CR0[15] causes the device to enter Deep Power Down (DPD) Note: 1: HyperRAM will automatically set the value of CR0[15] to "1" after exit DPD.
[14:12]	Drive Strength	000b - 34 ohms (default) 001b - 115 ohms 010b - 67 ohms 011b - 46 ohms 100b - 34 ohms 101b - 27 ohms 110b - 22 ohms 111b - 19 ohms
[11:8]	Reserved	1b - Reserved (default) Reserved for Future Use. When writing this register, these bits should be set to 1 for future compatibility.
[7:4]	Initial Latency	0000b - 5 Clock Latency @ 133MHz Max Frequency 0001b - 6 Clock Latency @ 166MHz Max Frequency 0010b - 7 Clock Latency @ 200MHz Max Frequency (default) 0011b - Reserved 0100b - Reserved ... 1101b - Reserved 1110b - 3 Clock Latency @ 83MHz Max Frequency 1111b - 4 Clock Latency @ 100MHz Max Frequency
[3]	Fixed Latency Enable	0b - Variable Latency – 1 or 2 times Initial Latency depending on RWDS during CA cycles. 1b - Fixed 2 times Initial Latency (default)
[2]	Hybrid Burst Enable	0b: Wrapped burst sequences to follow hybrid burst sequencing 1b: Wrapped burst sequences in legacy wrapped burst manner (default)
[1:0]	Burst Length	00b - 128 bytes 01b - 64 bytes 10b - 16 bytes 11b - 32 bytes (default)

9.4.1 Wrapped Burst

A wrapped burst transaction accesses memory within a group of words aligned on a word boundary matching the length of the configured group. Wrapped access groups can be configured as 16, 32, 64, or 128 bytes alignment and length. During wrapped transactions, access starts at the CA selected location within the group, continues to the end of the configured word group aligned boundary, then wraps around to the beginning location in the group, then continues back to the starting location. Wrapped bursts are generally used for critical word first instruction or data cache line fill read accesses.

9.4.2 Hybrid Burst

The beginning of a hybrid burst will wrap within the target address wrapped burst group length before continuing to the next half-page of data beyond the end of the wrap group. Continued access is in linear burst order until the transfer is ended by returning CS# High. This hybrid of a wrapped burst followed by a linear burst starting at the beginning of the next burst group, allows multiple sequential address cache lines to be filled in a single access. The first cache line is filled starting at the critical word. Then the next sequential line in memory can be read in to the cache while the first line is being processed.

Table 9 - CR0[2] Control of Wrapped Burst Sequence

Bit	Default Value	Name
2	1	Hybrid Burst Enable CR0[2]= 0b: Wrapped burst sequences to follow hybrid burst sequencing CR0[2]= 1b: Wrapped burst sequences in legacy wrapped burst manner

Table 10 - Example Wrapped Burst Sequences (HyperBus Addressing)

Burst Type	Wrap Boundary (Bytes)	Start Address (Hex)	Address Sequence (Hex) (Words)
Hybrid 128	128 Wrap once then Linear	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, 2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 00, 01, 02 (Wrap complete, now linear beyond the end of the initial 128 byte wrap group) 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 4A, 4B, 4C, 4D, 4E, 4F, 50, 51, ...
Hybrid 64	64 Wrap once then Linear	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00, 01, 02, (Wrap complete, now linear beyond the end of the initial 64 byte wrap group) 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, 2E, 2F, 30, 31, ...
Hybrid 64	64 Wrap once then Linear	XXXXXX2E	2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, (Wrap complete, now linear beyond the end of the initial 64 byte wrap group) 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 4A, 4B, 4C, 4D, 4E, 4F, 50, 51, ...
Hybrid 16	16 Wrap once then Linear	XXXXXX02	02, 03, 04, 05, 06, 07, 00, 01, (Wrap complete, now linear beyond the end of the initial 16 byte wrap group) 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, ...
Hybrid 16	16 Wrap once then Linear	XXXXXX0C	0C, 0D, 0E, 0F, 08, 09, 0A, 0B, (Wrap complete, now linear beyond the end of the initial 16 byte wrap group) 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, ...
Hybrid 32	32 Wrap once then Linear	XXXXXX0A	0A, 0B, 0C, 0D, 0E, 0F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09 (Wrap complete, now linear beyond the end of the initial 32 byte wrap group) 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, ...
Wrap 64	64	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 1A, 1B, 1C, 1D, 1E, 1F, 00, 01, 02, ...
Wrap 64	64	XXXXXX2E	2E, 2F, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 3A, 3B, 3C, 3D, 3E, 3F, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 2A, 2B, 2C, 2D, ...
Wrap 16	16	XXXXXX02	02, 03, 04, 05, 06, 07, 00, 01, ...
Wrap 16	16	XXXXXX0C	0C, 0D, 0E, 0F, 08, 09, 0A, 0B, ...
Wrap 32	32	XXXXXX0A	0A, 0B, 0C, 0D, 0E, 0F, 00, 01, 02, 03, 04, 05, 06, 07, 08, 09, ...
Linear	Linear Burst	XXXXXX03	03, 04, 05, 06, 07, 08, 09, 0A, 0B, 0C, 0D, 0E, 0F, 10, 11, 12, 13, 14, 15, 16, 17, 18, ...

9.4.3 Initial Latency

Memory Space read and write transactions or Register Space read transactions require some initial latency to open the row selected by the CA. This initial latency is t_{ACC}. The number of latency clocks needed to satisfy t_{ACC} depends on the HyperBus frequency and can vary from 3 to 7 clocks. The value in CR0[7:4] selects the number of clocks for initial latency. The default value is 7 clocks, allowing for operation up to a maximum frequency of 200MHz prior to the host system setting a lower initial latency value that may be more optimal for the system.

In the event a distributed refresh is required at the time a Memory Space read or writes transaction or Register Space read transaction begins, the RWDS signal goes High during the CA to indicate that an additional initial latency is being inserted to allow a refresh operation to complete before opening the selected row.

Register Space write transactions always have zero initial latency. RWDS may be High or Low during the CA period. The level of RWDS during the CA period does not affect the placement of register data immediately after the CA, as there is no initial latency needed to capture the register data. A refresh operation may be performed in the memory array in parallel with the capture of register data.

9.4.4 Fixed Latency

A configuration register option bit CR0[3] is provided to make all Memory Space read and write transactions or Register Space read transactions require the same initial latency by always driving RWDS High during the CA to indicate that two initial latency periods are required. This fixed initial latency is independent of any need for a distributed refresh; it simply provides a fixed (deterministic) initial latency for all of these transaction types. The fixed latency option may simplify the design of some HyperBus memory controllers or ensure deterministic transaction performance. Fixed latency is the default POR or reset configuration. The system may clear this configuration bit to disable fixed latency and allow variable initial latency with RWDS driven High only when additional latency for a refresh is required.

9.4.5 Drive Strength

DQ and RWDS signal line loading, length, and impedance vary depending on each system design. Configuration register bits CR0[14:12] provide a means to adjust the DQ[7:0] and RWDS signal output impedance to customize the DQ and RWDS signal impedance to the system conditions to minimize high speed signal behaviors such as overshoot, undershoot, and ringing. The default POR or reset configuration value is 000b to select the mid-point of the available output impedance options.

The impedance values shown are typical for both pull-up and pull-down drivers at typical silicon process conditions, nominal operating voltage (1.8V) and 50°C. The impedance values may vary from the typical values depending on the Process, Voltage, and Temperature (PVT) conditions. Impedance will increase with slower process, lower voltage, or higher temperature. Impedance will decrease with faster process, higher voltage, or lower temperature.

Each system design should evaluate the data signal integrity across the operating voltage and temperature ranges to select the best drive strength settings for the operating conditions.

9.4.6 Deep Power Down

When the HyperRAM device is not needed for system operation, it may be placed in a very low power consuming state called Deep Power Down (DPD), by writing 0 to CR0[15]. When CR0[15] is cleared to 0, the device enters the DPD state within t_{DPDIN} time and all refresh operations stop. The data in RAM is lost, (becomes invalid without refresh) during DPD state. Exiting DPD requires driving CS# Low then High, POR, or a reset. Only CS# and RESET# signals are monitored during DPD mode. All register content might lost in Deep Power Down State.

9.5 Configuration Register 1

Configuration Register 1 (CR1) is used to define the refresh array size, refresh rate and Hybrid Sleep for the HyperRAM device. Configurable characteristics include:

- Partial Array Refresh
- Hybrid Sleep State
- Refresh Rate

Table 11 - Configuration Register 1 Bit Assignments

CR1 Bit	Function	Settings (Binary)
[15-8]	Reserved	FFh - Reserved (default) Reserved for Future Use. When writing this register, these bits should keep FFh for future compatibility.
[7]	Reserved	1b - Reserved (default) When writing this register, this bit should keep 1b.
[6]	Master Clock Type	1b - Single Ended - CK (default) 0b - Differential - CK#, CK
[5]	Hybrid Sleep	1b - Writing 1 to CR1[5] causes the device to enter Hybrid Sleep (HS) State 0b - Normal operation (default)
[4:2]	Partial Array Refresh	000b - Full Array (default) 001b - Bottom 1/2 Array 010b - Bottom 1/4 Array 011b - Bottom 1/8 Array 100b - None 101b - Top 1/2 Array 110b - Top 1/4 Array 111b - Top 1/8 Array Note: The array means default 64Mb density.
[1:0]	Distributed Refresh Interval	10b - Reserved 11b - Reserved 00b - Reserved 01b - 4µS (t_{CSM})

Note:

1. CR1[1:0] is read only.

9.5.1 Master Clock Type

Two clock types, namely single ended and differential, are supported by HyperRAM. CR1[6] selects which type to use.

9.5.2 Partial Array Refresh

The partial array refresh configuration restricts the refresh operation in HyperRAM to a portion of the memory array specified by CR1[4:2]. This reduces the standby current. The default configuration refreshes the whole array.

9.5.3 Hybrid Sleep

When the HyperRAM is not needed for system operation, it may be placed in Hybrid Sleep state if data in the device needs to be retained. Enter Hybrid Sleep state by writing 1 to CR1[5]. Bringing CS# Low will cause the device to exit HS state and set CR1[5] to 0. Also, POR, or a hardware reset will cause the device to exit Hybrid Sleep state. Note that a POR or a hardware reset disables refresh where the memory core data can potentially get lost.

9.5.4 Distributed Refresh Interval

The DRAM array requires periodic refresh of all bits in the array. This can be done by the host system by reading or writing a location in each row within a specified time limit. The read or write access copies a row of bits to an internal buffer. At the end of the access the bits in the buffer are written back to the row in memory, thereby recharging (refreshing) the bits in the row of DRAM memory cells.

HyperRAM devices include self-refresh logic that will refresh rows automatically. The automatic refresh of a row can only be done when the memory is not being actively read or written by the host system. The refresh logic waits for the end of any active read or write before doing a refresh, if a refresh is needed at that time. If a new read or write begins before the refresh is completed, the memory will drive RWDS high during the CA period to indicate that an additional initial latency time is required at the start of the new access in order to allow the refresh operation to complete before starting the new access.

The required refresh interval for the entire memory array varies with temperature as shown in Table 12 - Array Refresh Interval per Temperature. This is the time within which all rows must be refreshed. Refresh of all rows could be done as a single batch of accesses at the beginning of each interval, in groups (burst refresh) of several rows at a time, spread throughout each interval, or as single row refreshes evenly distributed throughout the interval. The self-refresh logic distributes single row refresh operations throughout the interval so that the memory is not busy doing a burst of refresh operations for a long period, such that the burst refresh would delay host access for a long period.

Table 12 - Array Refresh Interval per Temperature

Device Temperature (TCASE °C)	Array Refresh Interval (mS)	Array Rows	Recommended tCSM (µS)	CR1[1:0]
TCASE < 85	64	8192	4	01b

The distributed refresh method requires that the host does not do burst transactions that are so long as to prevent the memory from doing the distributed refreshes when they are needed. This sets an upper limit on the length of read and writes transactions so that the refresh logic can insert a refresh between transactions. This limit is called the CS# low maximum time (t_{CSM}). The t_{CSM} value is determined by the array refresh interval divided by the number of rows in the array, then reducing this calculation by half to ensure that a distributed refresh interval cannot be entirely missed by a maximum length host access starting immediately before a distributed refresh is needed. Because t_{CSM} is set to half the required distributed refresh interval, any series of maximum length host accesses that delay refresh operations will catch up on refresh operations at twice the rate required by the refresh interval divided by the number of rows.

The host system is required to respect the t_{CSM} value by ending each transaction before violating t_{CSM}. This can be done by host memory controller logic splitting long transactions when reaching the t_{CSM} limit, or by host system hardware or software not performing a single read or write transaction that would be longer than t_{CSM}.

As noted in Table 12 - Array Refresh Interval per Temperature, the array refresh interval is longer at lower temperatures such that t_{CSM} could be increased to allow longer transactions. The host system can either use the t_{CSM} value from the table for the maximum operating temperature or, may determine the current operating temperature from a temperature sensor in the system in order to set a longer distributed refresh interval.

10. INTERFACE STATES

10.1 IO condition of interface states

Below Interface States table describes the required value of each signal for each interface state.

Table 13 - Interface States

Interface State	VCC / VCCQ	CS#	CK, CK#	DQ7-DQ0	RWDS	RESET#
Power-Off	$< V_{LKO}$	X	X	High-Z	High-Z	X
Power-On (Cold) Reset	VCC / VCCQ min	X	X	High-Z	High-Z	X
Hardware (Warm) Reset	VCC / VCCQ min	X	X	High-Z	High-Z	L
Interface Standby	VCC / VCCQ min	H	X	High-Z	High-Z	H
CA	VCC / VCCQ min	L	T	Master Output Valid	X	H
Read Initial Access Latency (data bus turn around period)	VCC / VCCQ min	L	T	High-Z	L	H
Write Initial Access Latency (RWDS turn around period)	VCC / VCCQ min	L	T	High-Z	High-Z	H
Read data transfer	VCC / VCCQ min	L	T	Slave Output Valid	Slave Output Valid X or T	H
Write data transfer with Initial Latency	VCC / VCCQ min	L	T	Master Output Valid	Master Output Valid X or T	H
Write data transfer without Initial Latency *[1]	VCC / VCCQ min	L	T	Master Output Valid	Slave Output L or High-Z	H
Active Clock Stop	VCC / VCCQ min	L	Idle	Master or Slave Output Valid or High-Z	X	H
Deep Power Down	VCC / VCCQ min	H	X or T	High-Z	High-Z	H
Hybrid Sleep	VCC / VCCQ min	H	X or T	High-Z	High-Z	H

Legend

L = VIL

H = VIH

X = Either VIL, VIH, VOL or VOH

L/H = Rising edge

H/L = Falling edge

T = Toggling during information transfer

Idle = CK is Low and CK# is High.

Valid = All bus signals have stable L or H level

Note:

1. Writes without initial latency (with zero initial latency), do not have a turnaround period for RWDS. The HyperRAM device will always drive RWDS during the CA period to indicate whether extended latency is required. Since master write data immediately follows the CA period the HyperRAM device may continue to drive RWDS Low or may take RWDS to High-Z. The master must not drive RWDS during Writes with zero latency. Writes with zero latency do not use RWDS as a data mask function. All bytes of write data are written (full word writes).

10.2 Power Conservation Modes

10.2.1 Interface Standby

Standby is the default, low power, state for the interface while the device is not selected by the host for data transfer (CS#= High). All inputs and outputs other than CS# and RESET# are ignored in this state.

10.2.2 Active Clock Stop

The Active Clock Stop state reduces device interface energy consumption to the ICC6 level during the data transfer portion of a read or writes operation. The device automatically enables this state when clock remains stable for t_{ACC} + 30 nS. While in Active Clock Stop state, read data is latched and always driven onto the data bus. Active Clock Stop state helps reduce current consumption when the host system clock has stopped to pause the data transfer. Even though CS# may be Low throughout these extended data transfer cycles, the memory device host interface will go into the Active Clock Stop current level at t_{ACC} + 30 nS. This allows the device to transition into a lower current state if the data transfer is stalled. Active read or write current will resume once the data transfer is restarted with a toggling clock. The Active Clock Stop state must not be used in violation of the t_{CSM} limit. CS# must go High before t_{CSM} is violated. Note that it is recommended to stop the clock when it is in Low state.

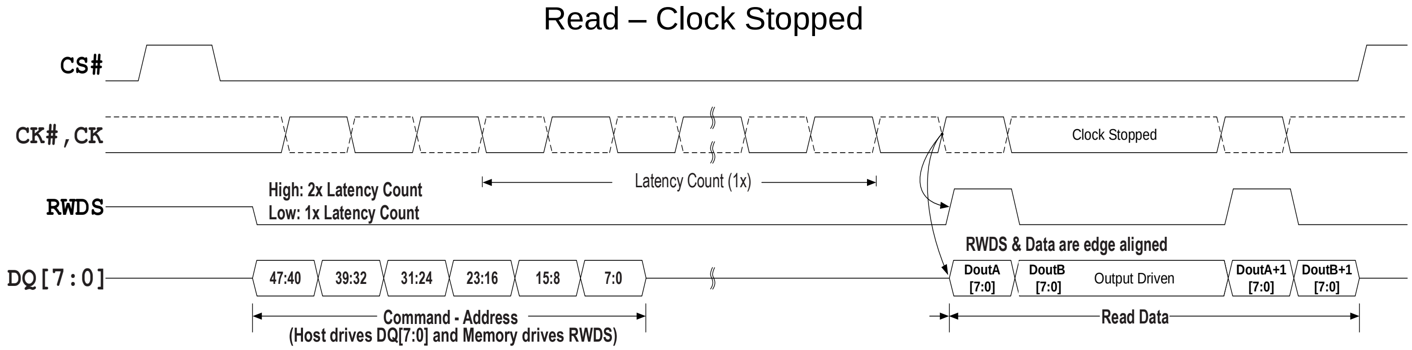

Read – Clock Stopped
CS#
CK#,CK
Clock Stopped
RWDS
High: 2x Latency Count
Low: 1x Latency Count
Latency Count (1x)
RWDS & Data are edge aligned
DQ[7:0]
47:40
39:32
31:24
23:16
15:8
7:0
DoutA [7:0]
DoutB [7:0]
Output Driven
DoutA+1 [7:0]
DoutB+1 [7:0]
Command - Address
(Host drives DQ[7:0] and Memory drives RWDS)
Read Data

Figure 13 - Active Clock Stop during Read Transaction (DDR)

10.2.3 Hybrid Sleep

In the Hybrid Sleep (HS) state, the current consumption is reduced (IHS). HS state is entered by writing a 1 to CR1[5]. The device reduces power within t_{HSIN} time. The data in Memory Space and Register Space is retained during HS state. Bringing CS# Low will cause the device to exit HS state and set CR1[5] to 0. Also, POR, or a hardware reset will cause the device to exit HS state. Returning to Standby state requires t_{EXTHS} time. Following the exit from HS due to any of these events, the device is in the same state as entering HS.

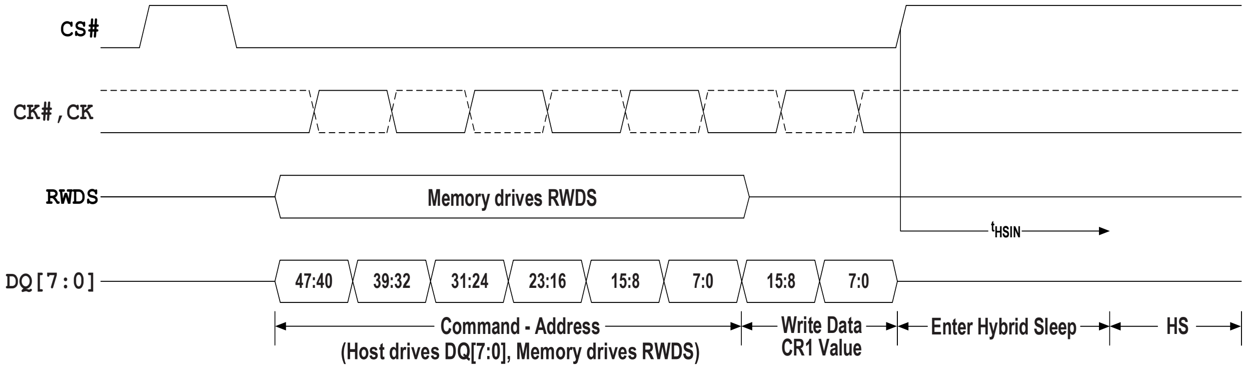

CS#
CK#,CK
RWDS
Memory drives RWDS
tHSIN
DQ[7:0]
47:40
39:32
31:24
23:16
15:8
7:0
15:8
7:0
Command - Address
(Host drives DQ[7:0], Memory drives RWDS)
Write Data
CR1 Value
Enter Hybrid Sleep
HS

Figure 14 - Enter Hybrid Sleep Transaction

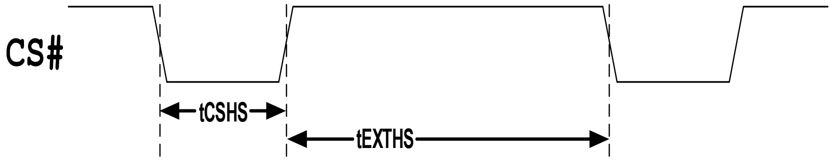

CS#
tCSHS
tEXTHS

Figure 15 - Exit Hybrid Sleep Transaction

10.2.4 Deep Power Down

In the Deep Power down (DPD) state, current consumption is driven to the lowest possible level (I_{DPD}). DPD state is entered by writing a 0 to CR0[15]. The device reduces power within t_{DPDIN} time and all refresh operations stop. The data in Memory Space is lost, (becomes invalid without refresh) during DPD state. Driving CS# Low then High will cause the device to exit DPD state. Also, POR, or a hardware reset will cause the device to exit DPD state. Returning to Standby state requires t_{EXTDPD} time. Returning to Standby state following a POR requires t_{VCS} time, as with any other POR. Following the exit from DPD due to any of these events, the device is in the same state as following POR.

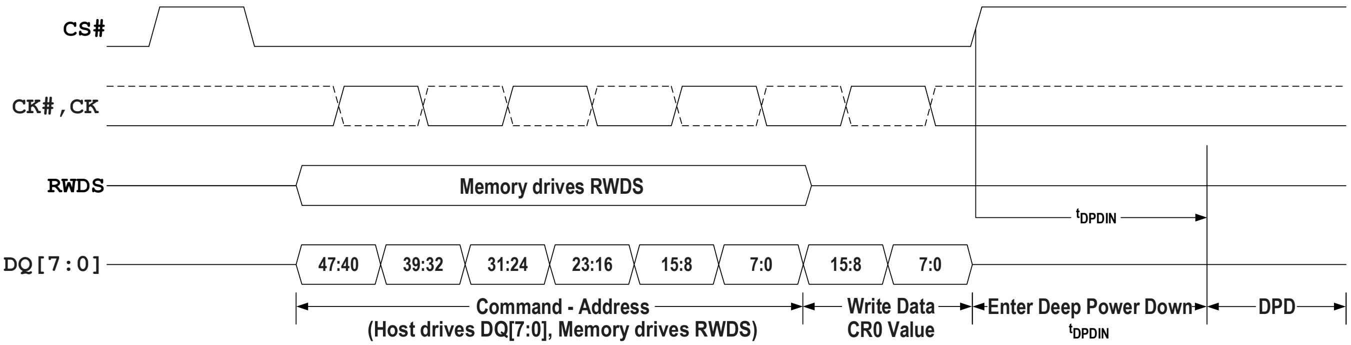

CS#
CK#,CK
RWDS
Memory drives RWDS
DQ[7:0]
47:40
39:32
31:24
23:16
15:8
7:0
15:8
7:0
tDPDIN
Command - Address
(Host drives DQ[7:0], Memory drives RWDS)
Write Data
CR0 Value
Enter Deep Power Down
tDPDIN
DPD

Figure 16 - Enter DPD Transaction

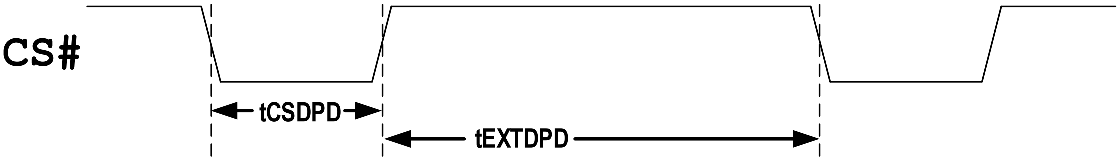

CS#
tCSDPD
tEXTDPD

Figure 17 - Exit DPD Transaction

11. ELECTRICAL SPECIFICATIONS

11.1 Absolute Maximum Ratings

Parameter	Min	Max	Unit	Notes
Voltage on VCC,VCCQ supply relative to VSS	-0.5	VCC +0.5	V	1
Voltage to any ball except VCC relative to VSS	-0.5	VCC +0.5	V	1
Soldering temperature and time 10s (solder ball only)	+260		°C	1
Storage temperature (plastic)	-65	+150	°C	1
Output Short Circuit Current		100	mA	1, 2

Notes:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.
2. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

11.2 Latch up Characteristics

Description	Min	Max	Unit
Input voltage with respect to V_{SS} on all input only connections	-1.0	V_{CC} + 1.0	V
Input voltage with respect to V_{SSQ} on all I/O connections	-1.0	V_{CCQ} + 1.0	V
VCCQ Current	-100	+100	mA

Note:

1. Excludes power supplies VCC/VCCQ. Test conditions: VCC = VCCQ, one connection at a time tested, connections not being tested are at VSS.

11.3 Operating Ranges

11.3.1 DC Characteristics

Parameter	Description	Test Conditions	Min	Max	Unit
VCC,VCCQ	Power Supply		1.7	2.0	V
VIL	Input Low Voltage		-0.15 x VCC	0.3 x VCC	V
VIH	Input High Voltage		0.7 x VCC	1.15 x VCC	V
VOL	Output Low Voltage	IOL = 100µA for DQ[7:0]	–	0.2	V
VOH	Output High Voltage	IOH = 100µA for DQ[7:0]	VCCQ - 0.2	–	V

Note:

1. All parts list in order information table (section 2) will not guarantee to meet functional and AC specification if the VCC, VCCQ operation condition out of range mentioned in above table.

11.3.2 Operating Temperature

Parameter	Symbol	Range	Unit	Note
Operating Temperature	TCASE	-40~85	°C	1

Note:

1. All parts list in order information table (section 2) will not guarantee to meet functional and AC specification if the operation temperature range out of range mentioned in above table.

11.3.3 ICC Characteristics

Parameter	Description	Test Conditions	Min	Typ*1	Max	Unit
ILI2	Input Leakage Current Device Reset Signal High Only	VIN = VSS to VCC, VCC = VCC max	–	–	2	µA
ILI4	Input Leakage Current Device Reset Signal Low Only*2	VIN = VSS to VCC, VCC = VCC max	–	–	15	µA
ICC1	VCC Active Read Current	CS# = VSS, @200 MHz, VCC = 2.0V	–	15	25	mA
ICC2	VCC Active Write Current	CS# = VSS, @200 MHz, VCC = 2.0V	–	15	25	mA
ICC5	Reset Current	CS# = VCC, RESET# = VSS, VCC = VCC max	–	–	1	mA
ICC6	Active Clock Stop Current (-40°C to +85°C)	CS# = VSS, RESET# = VCC, VCC = VCC max	–	5	8	mA
ICC7	VCC Current during power up*1	CS# = VCC, VCC = VCC max, VCC = VCCQ = 2.0V	–	–	35	mA
IDPD	Deep Power Down Current (85°C)	CS# = VCC, VCC = 2.0V	–	–	10	µA

Parameter	Description	Test Conditions		Min	Typ*1	Max	Unit
ICC4	VCC Standby Current (-40°C to +85°C)	CS# = VCC, VCC = 2.0V	Full Array	–	80	220	µA
			Bottom 1/2 Array	–	–	200	
			Bottom 1/4 Array	–	–	180	
			Bottom 1/8 Array	–	–	170	
			Top 1/2 Array	–	–	200	
			Top 1/4 Array	–	–	180	
			Top 1/8 Array	–	–	170	
IHS	Hybrid Sleep Current (-40°C to +85°C)	CS# = VCC, VCC = 2.0V	Full Array	–	25	200	µA
			Bottom 1/2 Array	–	–	170	
			Bottom 1/4 Array	–	–	150	
			Bottom 1/8 Array	–	–	140	
			Top 1/2 Array	–	–	170	
			Top 1/4 Array	–	–	150	
			Top 1/8 Array	–	–	140	

Notes:

1. Typical values are referring to the maximum root mean square value measured @ TCASE=25°C and for reference only, not tested in mass production process.
2. RESET# Low initiates exits from DPD state and initiates the draw of ICC5 reset current, making ILI during Reset# Low insignificant.

11.3.4 Power-Up Initialization

HyperRAM products include an on-chip voltage sensor used to launch the power-up initialization process. VCC and VCCQ must be applied simultaneously. When the power supply reaches a stable level at or above VCC (min), the device will require t_{VCS} time to complete its self-initialization process.

The device must not be selected during power-up. CS# must follow the voltage applied on VCCQ until VCC (min) is reached during power-up, and then CS# must remain high for a further delay of t_{VCS}. A simple pull-up resistor from VCCQ to Chip Select (CS#) can be used to insure safe and proper power-up.

If RESET# is Low during power up, the device delays start of the t_{VCS} period until RESET# is High. The t_{VCS} period is used primarily to perform refresh operations on the DRAM array to initialize it.

When initialization is complete, the device is ready for normal operation.

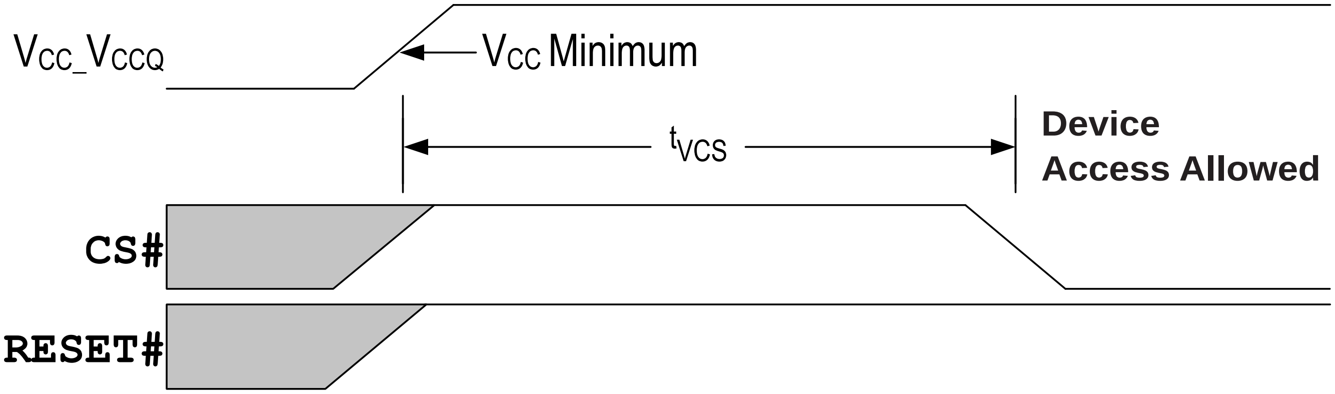


Figure 18 - Power-up with RESET# High

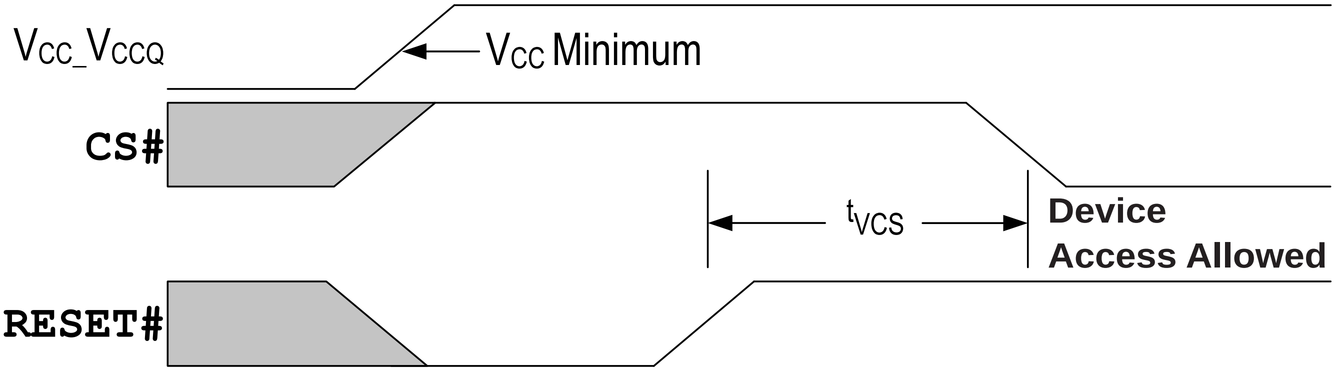


Figure 19 - Power-up with RESET# Low

Table 14 - Power Up and Reset Parameters

Parameter	Description	Min	Max	Unit
VCC	VCC Power Supply	1.7	2.0	V
t_{VCS}	VCC and VCCQ ≥ minimum and RESET# High to first access	–	150	µS

Notes:

1. Bus transactions (read and write) are not allowed during the power-up reset time (t_{VCS}).
2. VCCQ must be the same voltage as VCC.
3. VCC ramp rate may be non-linear.

11.3.5 Power-Down

HyperRAM devices are considered to be powered-off when the array power supplies (VCC) drops below the VCC Lock-Out voltage (VLKO). During a power supply transition down to the VSS level, VCCQ should remain less than or equal to VCC. At the VLKO level, the HyperRAM device will have lost configuration or array data.

VCC must always be greater than or equal to VCCQ (VCC ≥ VCCQ).

During Power-Down or voltage drops below VLKO, the array power supply voltages must also drop below VCC Reset (VRST) for a Power Down period (t_{PD}) for the part to initialize correctly when the power supply again rises to VCC minimum. See Figure 20 - Power Down or Voltage Drop.

If during a voltage drop the VCC stays above VLKO the part will stay initialized and will work correctly when VCC is again above VCC minimum. If VCC does not go below and remain below VRST for greater than t_{PD}, then there is no assurance that the POR process will be performed. In this case, a hardware reset will be required ensure the HyperBus device is properly initialized.

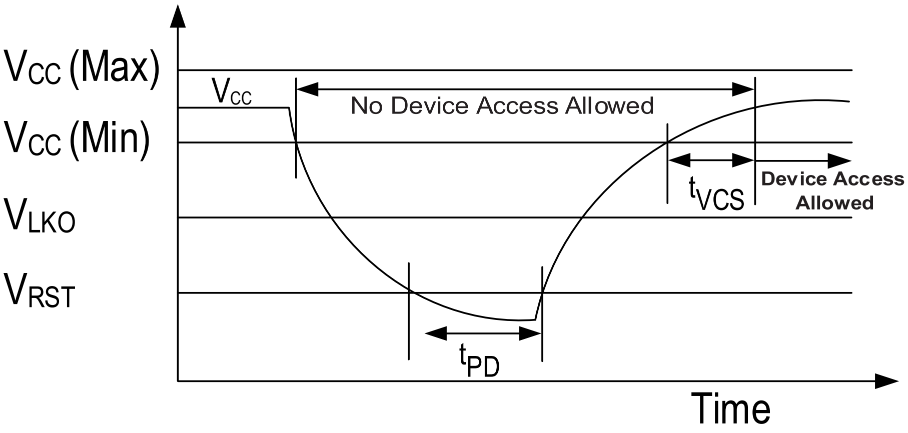


Figure 20 - Power Down or Voltage Drop

The following section describes HyperRAM device dependent aspects of power down specifications.

Table 15 - Power-Down Voltage and Timing

Parameter	Description	Min	Max	Unit
VCC	VCC Power Supply	1.7	2.0	V
VLKO	VCC Lock-out below which re-initialization is required	1.5	–	V
VRST	VCC Low Voltage needed to ensure initialization will occur	0.7	–	V
t_{PD}	Duration of VCC ≤ VRST	50	–	µS

Note: VCC ramp rate can be non-linear.

11.3.6 Hardware Reset

The RESET# input provides a hardware method of returning the device to the standby state.

During t_{RPH} the device will draw I_{CC5} current. If RESET# continues to be held Low beyond t_{RPH}, the device draws CMOS standby current (I_{CC4}). While RESET# is Low (during t_{RP}), and during t_{RPH}, bus transactions are not allowed.

A hardware reset will:

- Cause the configuration registers to return to their default values
- Halt self-refresh operation while RESET# is low - memory array data is considered as invalid
- Force the device to exit the Hybrid Sleep state
- Force the device to exit the Deep Power Down state

After RESET# returns high, the self-refresh operation will resume. Because self-refresh operation is stopped during RESET# Low, and the self-refresh row counter is reset to its default value, some rows may not be refreshed within the required array refresh interval per Table 12 - Array Refresh Interval per Temperature on page 25. This may result in the loss of DRAM array data during or immediately following a hardware reset. The host system should assume DRAM array data is lost after hardware reset and reload any required data.

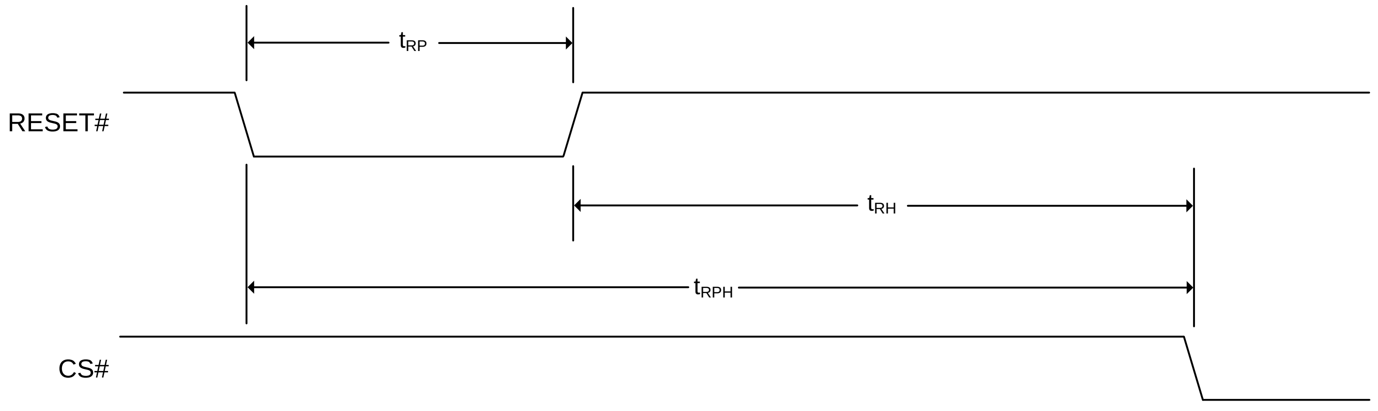


Figure 21 - Hardware Reset Timing Diagram

Table 16 - Power Up and Reset Parameters

Parameter	Description	Min	Max	Unit
t_{RP}	RESET# Pulse Width	200	–	nS
t_{RH}	Time between RESET# (High) and CS# (Low)	200	–	nS
t_{RPH}	RESET# Low to CS# Low	400	–	nS

Note: The RESET# pin is 4V tolerant.

11.3.7 Capacitance Characteristics

Table 17 - Capacitive Characteristics

Parameter	Description	Min	Max	Unit
C_I	Input Capacitance (CK, CK#, CS#)		3.0	pF
C_{ID}	Delta Input Capacitance (CK, CK#)		0.25	pF
C_O	Output Capacitance (RWDS)		3.0	pF
C_{IO}	IO Capacitance (DQx)		3.0	pF
C_{IOD}	IO Capacitance Delta (DQx)		0.25	pF

Notes:

1. These values are guaranteed by design and are tested on a sample basis only.
2. These values are applies to die device only (does not include package capacitance).
3. Contact capacitance is measured according to JEP147 procedure for measuring capacitance using a vector network analyzer. V_{CC}, V_{CCQ} are applied and all other signals (except the signal under test) floating. DQ's should be in the high impedance state.
4. The capacitance values for the CK, CK#, RWDS and DQx signals must have similar capacitance values to allow for signal propagation time matching in the system. The capacitance value for CS# is not as critical because there are no critical timings between CS# going active (Low) and data being presented on the DQs bus.

11.4 Input Signal Overshoot

During DC conditions, input or I/O signals should remain equal to or between V_{SS} and V_{CC}. During voltage transitions, inputs or I/Os may negative overshoot V_{SS} to -1.0V or positive overshoot to V_{CC} +1.0V, for periods up to 20 nS.

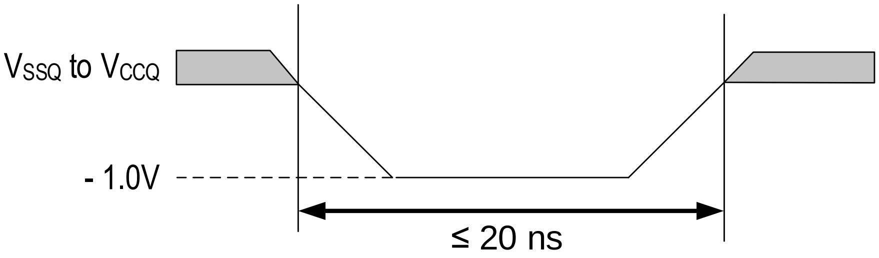


Figure 22 - Maximum Negative Overshoot Waveform

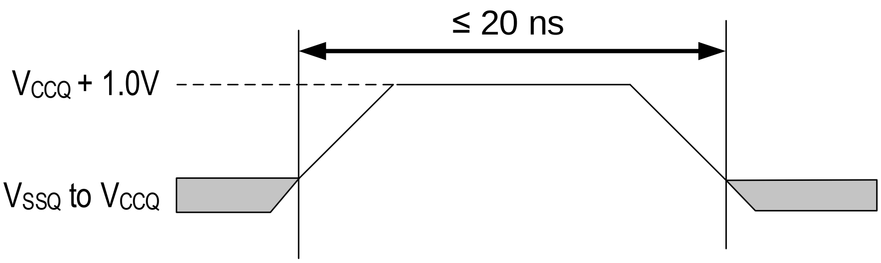
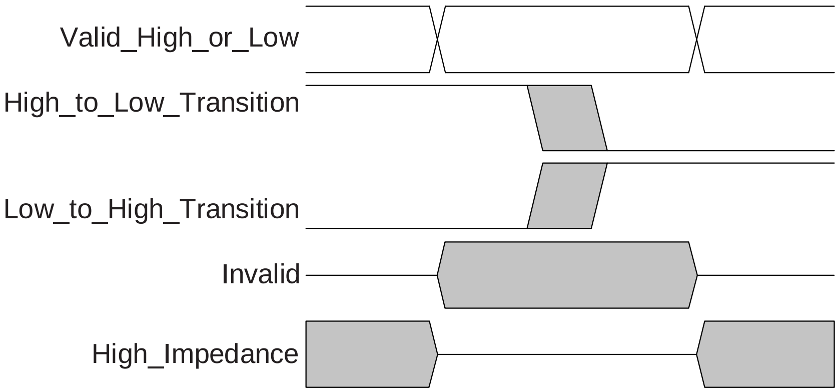


Figure 23 - Maximum Positive Overshoot Waveform

12. TIMING SPECIFICATIONS

The following section describes HyperRAM device dependent aspects of timing specifications.

12.1 Key to Switching Waveforms


Valid_High_or_Low
High_to_Low_Transition
Low_to_High_Transition
Invalid
High_Impedance

12.2 AC Test Conditions

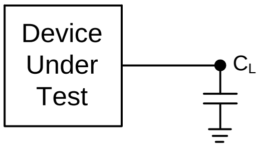

Device Under Test
CL

Figure 24 - Test load reference

Table 18 - Test Specification

Description	All	Unit	Notes
Output Load Capacitance, CL	15	pF	
Minimum Input Rise and Fall Slew Rates	1.13	V/nS	1
Input Pulse Levels	0-VCCQ	V	
Input timing measurement reference levels	VCCQ/2	V	2
Output timing measurement reference levels	VCCQ/2	V	2

Notes:

1. All AC timings assume this input slew rate.
2. Input and output timing is referenced to VCCQ/2 for single ended clock or RWDS or referenced to the crossing of CK/CK# for the differential clock pair.

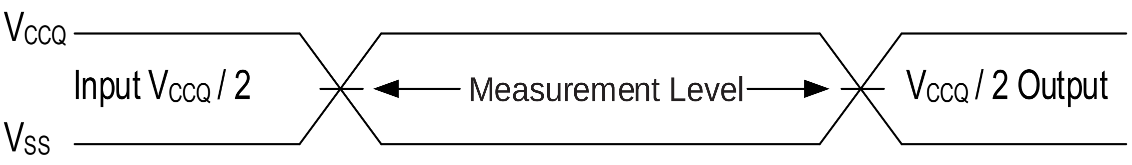

VCCQ
Input VCCQ / 2
Measurement Level
VCCQ / 2 Output
VSS

Figure 25 - Input Waveforms and Measurement Levels

12.3 AC Characteristics

12.3.1 Read Transactions

Table 19 - HyperRAM Specific Read Timing Parameters

Description	Parameter	200 MHz		Unit
		Min	Max	
Chip Select High Between Transactions	t_{CSHI}	6	–	nS
HyperRAM Read-Write Recovery Time	t_{RWR}	35	–	nS
Chip Select Setup to next CK Rising Edge	t_{CSS}	4	–	nS
Data Strobe Valid	t_{DSV}	–	5	nS
Input Setup	t_{IS}	0.5	–	nS
Input Hold	t_{IH}	0.5	–	nS
HyperRAM Read Initial Access Time	t_{ACC}	35	–	nS
Clock to DQs Low Z	t_{DQLZ}	0	–	nS
CK transition to DQ Valid	t_{CKD}	1	5	nS
CK transition to DQ Invalid	t_{CKDI}	0	4.2	nS
Data Valid	t_{DV}	1.45	–	nS
CK transition to RWDS Low @CA phase @Read	t_{CKDSR}	1	5.5	nS
CK transition to RWDS Valid	t_{CKDS}	–	5	nS
RWDS transition to DQ Valid	t_{DSS}	-0.4	+0.4	nS
RWDS transition to DQ Invalid	t_{DSH}	-0.4	+0.4	nS
Chip Select Hold After CK Falling Edge	t_{CSH}	0	–	nS
Chip Select Inactive to RWDS High-Z	t_{DSZ}	–	5	nS
Chip Select Inactive to DQ High-Z	t_{OZ}	–	5	nS
Refresh Time	t_{RFH}	35	–	nS

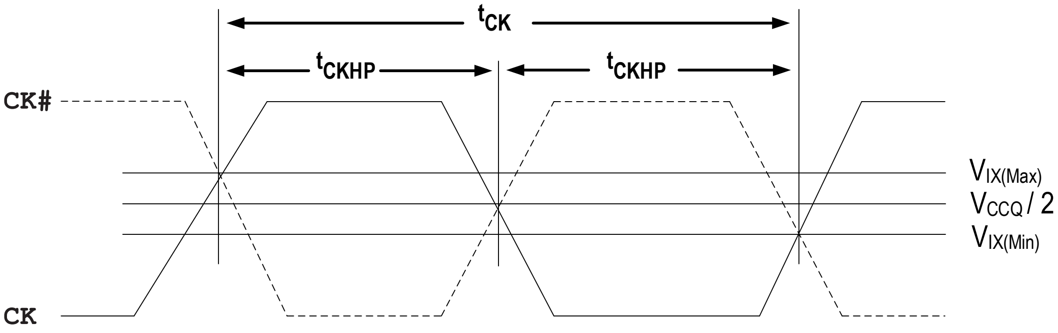


Figure 26 - Clock Characteristics

Table 20 - Clock Timings

Description	**Parameter**	**200 MHz**		**Unit**
		Min	**Max**	
CK Period	t_{CK}	5	–	nS
CK Half Period - Duty Cycle	t_{CKHP}	0.45	0.55	t_{CK}
CK Half Period at Frequency Min = 0.45 t_{CK} Min Max = 0.55 t_{CK} Min	t_{CKHP}	2.25	2.75	nS

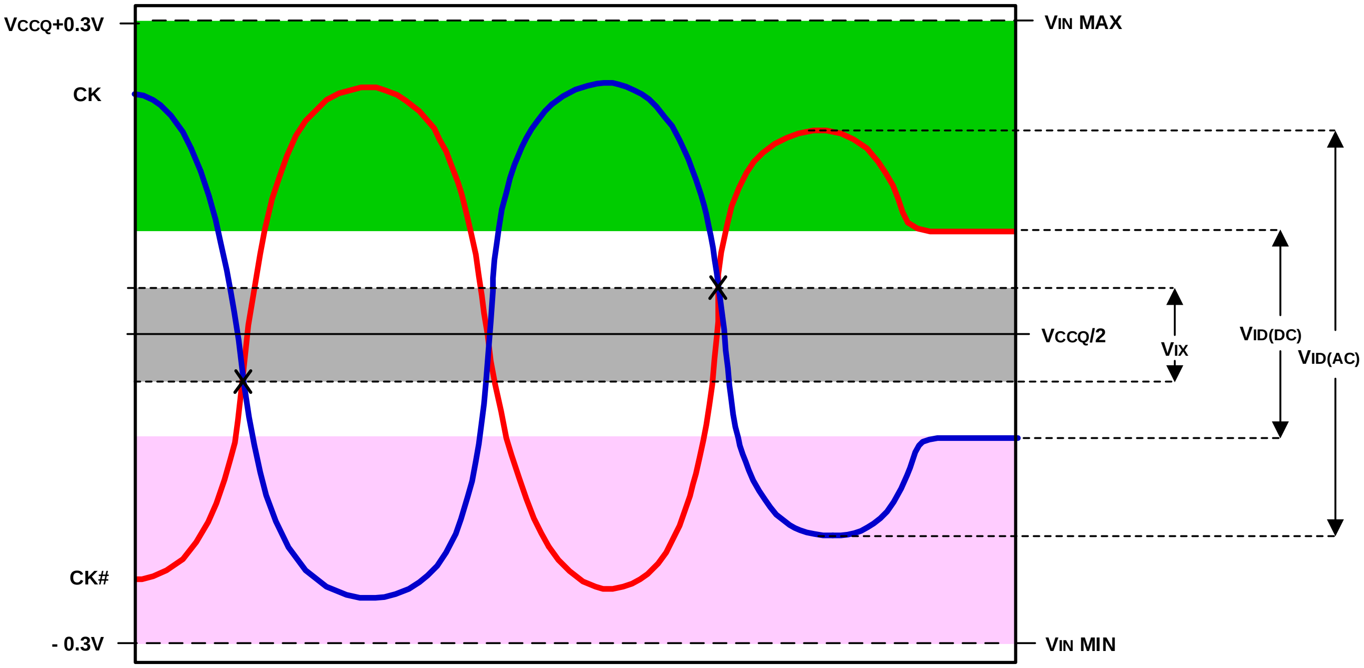
Notes:

1. Clock jitter of ±5% is permitted.
2. Minimum Frequency (Maximum t_{CK}) is dependent upon maximum CS# Low time (t_{CSM}), initial Latency and Burst Length.
3. All parts list in order information table (section 2) will not guarantee to meet functional and AC specification if the t_{CK} and t_{CKHP} out of range mentioned in above table.

Table 21 - Clock AC/DC Electrical Characteristics

Description	Parameter	Min	Max	Unit
DC Input Voltage	VIN	-0.3	VCCQ + 0.3	V
DC Input Differential Voltage	VID(DC)	VCCQ x 0.4	VCCQ + 0.6	V
AC Input Differential Voltage	VID(AC)	VCCQ x 0.6	VCCQ + 0.6	V
AC Differential Crossing Voltage	VIX	VCCQ x 0.4	VCCQ x 0.6	V

Differential Clock Input Levels



Notes:

1. CK and CK# input slew rate must be ≥1V/nS (2V/nS if measured differentially).
2. VID(DC) is the magnitude of the difference between the input level on CK and the input level on CK# when the CK and CK# is stable at a certain voltage level.
3. VID(AC) is the magnitude of the difference between the input level on CK and the input level on CK# when the CK and CK# is transient within a range defined for VIN.
4. The value of VIX is expected to equal VCCQ/2 of the transmitting device and must track variations in the DC level of VCCQ.

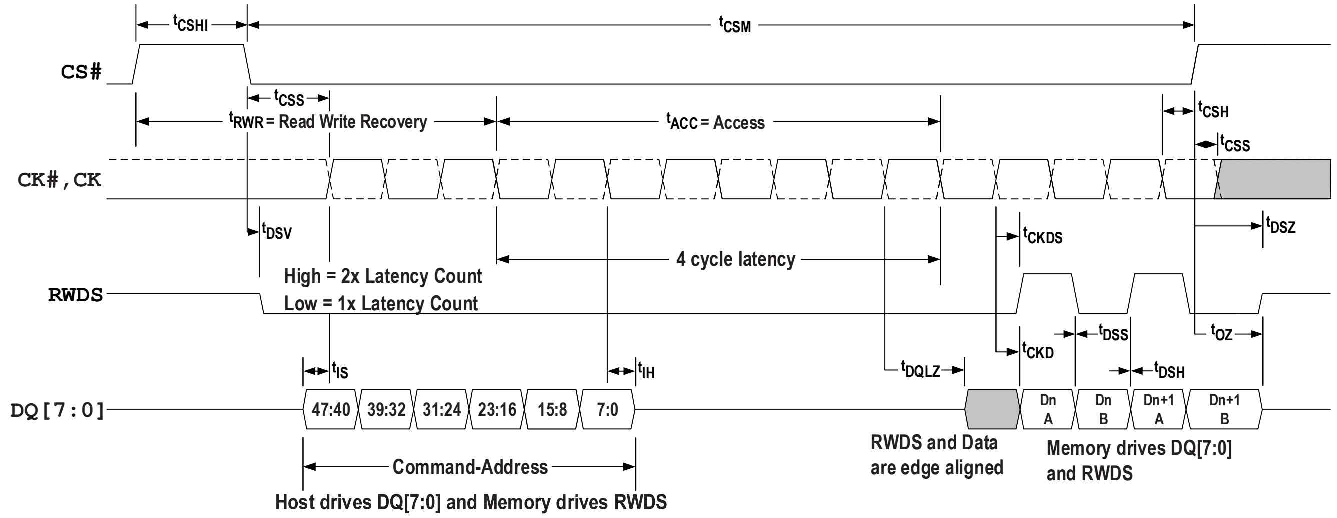

tCSHI
tCSM
CS#
tCSS
tRWR = Read Write Recovery
tACC = Access
tCSH
tCSS
CK#,CK
tDSV
tCKDS
tDSZ
4 cycle latency
High = 2x Latency Count
Low = 1x Latency Count
RWDS
tCKD
tDSS
tOZ
tIS
tIH
tDQLZ
tDSH
DQ[7:0]
47:40
39:32
31:24
23:16
15:8
7:0
Dn A
Dn B
Dn+1 A
Dn+1 B
RWDS and Data are edge aligned
Memory drives DQ[7:0] and RWDS
Command-Address
Host drives DQ[7:0] and Memory drives RWDS

Figure 27 - Read Timing Diagram — No Additional Latency Required

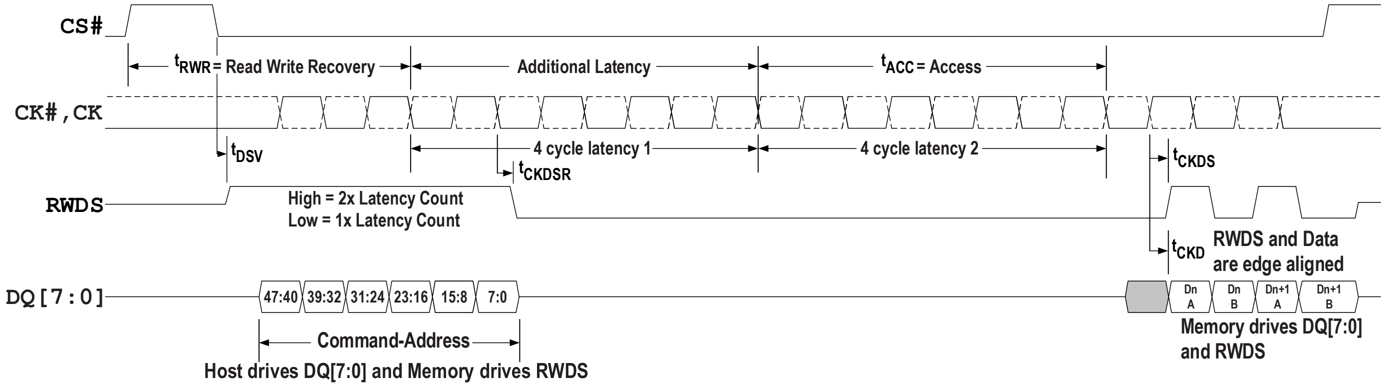
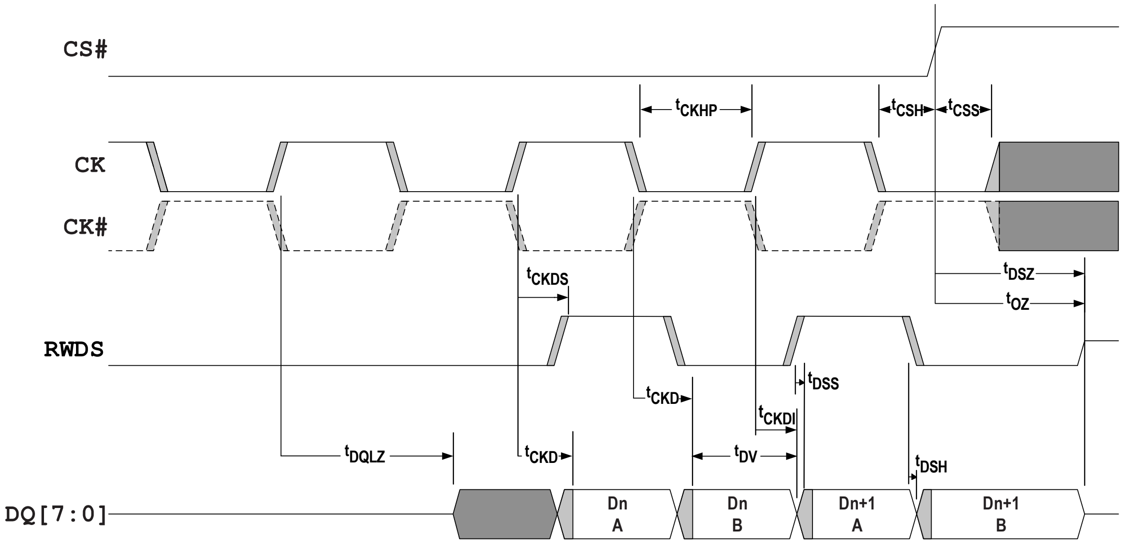

CS#
tRWR = Read Write Recovery
Additional Latency
tACC = Access
CK#,CK
tDSV
4 cycle latency 1
4 cycle latency 2
tCKDSR
tCKDS
RWDS
High = 2x Latency Count
Low = 1x Latency Count
tCKD
RWDS and Data are edge aligned
DQ[7:0]
47:40
39:32
31:24
23:16
15:8
7:0
Dn A
Dn B
Dn+1 A
Dn+1 B
Memory drives DQ[7:0] and RWDS
Command-Address
Host drives DQ[7:0] and Memory drives RWDS

Figure 28 - Read Timing Diagram — With Additional Latency

Notes:

1. Timing parameters applicable to HyperBus interfaces.
2. Transactions must be initiated with CK = Low and CK# = High.
3. CS# must return High before a new transaction is initiated.
4. The memory drives RWDS during the entire Read transaction.
5. Transactions without additional latency count have RWDS Low during CA cycles. Transactions with additional latency count have RWDS High during CA cycles and RWDS returns low at t_{CKDSR}. All other timing relationships are the same for both figures although they are not shown in the second figure. A four cycle latency is used for illustration purposes only. The required latency count is device and clock frequency dependent.
6. These parameters are required by HyperRAM.



RWDS and Data are edge aligned and driven by the memory

Figure 29 - Data Valid Timing

Notes:

1. This figure shows a closer view of the data transfer portion of read transaction diagrams to more clearly show the Data Valid period as affected by clock jitter and clock to output delay uncertainty.
2. The tCKD and tCKDI timing parameters define the beginning and end position of the data valid period.
3. The tDSS and tDSH timing parameters define how early or late RWDS may transition relative to the transition of data. This is the potential skew between the clock to data delay tCKD, and clock to data strobe delay tCKDS. Aside from this skew, the tCKD, tCKDI, and tCKDS values track together (vary by the same ratio) because RWDS and Data are outputs from the same device under the same voltage and temperature conditions.

12.3.2 Write Transactions

Table 22 - Write Timing Parameters

Description	Parameter	200 MHz		Unit
		Min	Max	
Read-Write Recovery Time	t_{RWR}	35	–	nS
Access Time	t_{ACC}	35	–	nS
Refresh Time	t_{RFH}	35	–	nS
Chip Select Maximum Low Time (TCASE < 85°C)	t_{CSM}	–	4	µS
RWDS Data Mask Valid	t_{DMV}	0	–	µS

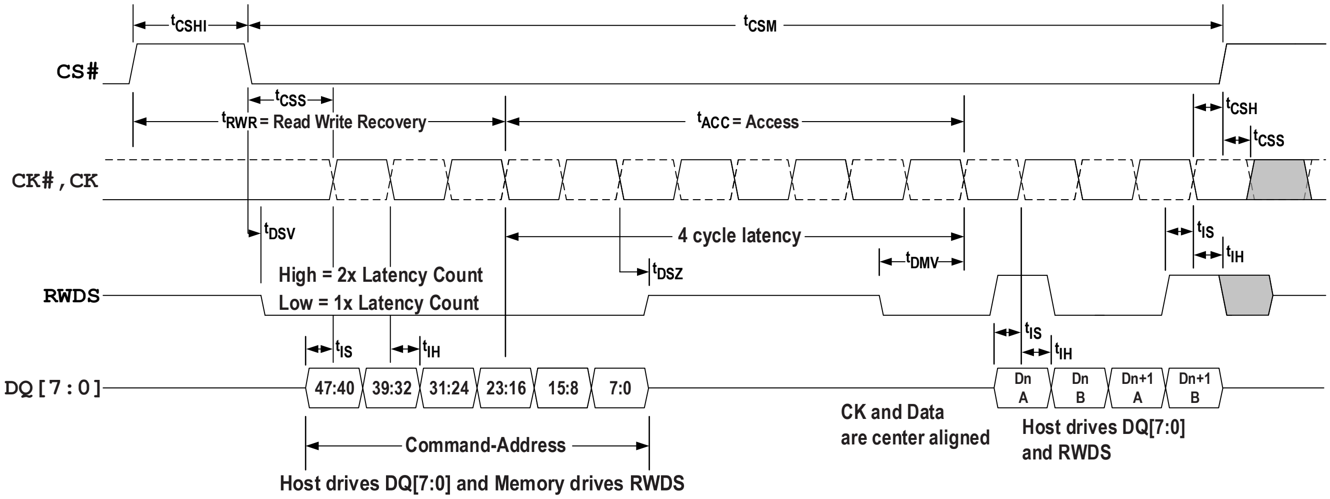

t_{CSHI}
t_{CSM}
CS#
t_{CSS}
t_{RWR} = Read Write Recovery
t_{ACC} = Access
t_{CSH}
t_{CSS}
CK#,CK
t_{DSV}
4 cycle latency
t_{IS}
t_{IH}
t_{DSZ}
t_{DMV}
High = 2x Latency Count
Low = 1x Latency Count
RWDS
t_{IS}
t_{IH}
t_{IS}
t_{IH}
DQ[7:0]
47:40
39:32
31:24
23:16
15:8
7:0
Dn A
Dn B
Dn+1 A
Dn+1 B
CK and Data are center aligned
Host drives DQ[7:0] and RWDS
Command-Address
Host drives DQ[7:0] and Memory drives RWDS

Figure 30 - Write Timing Diagram — No Additional Latency

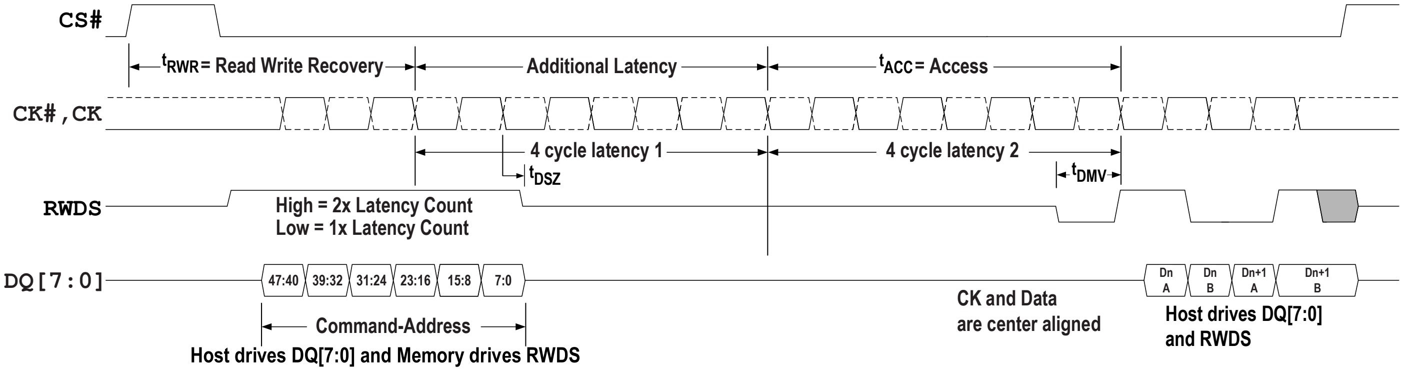

CS#
t_{RWR} = Read Write Recovery
Additional Latency
t_{ACC} = Access
CK#,CK
4 cycle latency 1
4 cycle latency 2
t_{DSZ}
t_{DMV}
RWDS
High = 2x Latency Count
Low = 1x Latency Count
DQ[7:0]
47:40
39:32
31:24
23:16
15:8
7:0
Dn A
Dn B
Dn+1 A
Dn+1 B
Command-Address
Host drives DQ[7:0] and Memory drives RWDS
CK and Data are center aligned
Host drives DQ[7:0] and RWDS

Figure 31 - Write Timing Diagram — With Additional Latency

Notes:

1. Timing parameters applicable to HyperBus interfaces.
2. Transactions must be initiated with CK=Low and CK#=High. CS# must return High before a new transaction is initiated.
3. During write transactions with latency, RWDS is used as an additional latency indicator initially and is then used as a data mask during data transfer.
4. Transactions without additional latency count have RWDS Low during CA cycles and RWDS returns Hi-Z at t_{DSZ}. Transactions with additional latency count have RWDS High during CA cycles and RWDS returns Hi-Z at t_{DSZ}. All other timing relationships are the same for both figures although they are not shown in the second figure. A four cycle latency is used for illustration purposes only. The required latency count is device and clock frequency dependent.
5. At the end of Command-Address cycles the memory stops driving RWDS to allow the host HyperBus master to begin driving RWDS. The master must drive RWDS to a valid Low before the end of the initial latency to provide a data mask preamble period to the slave. This can be done during the last cycle of the initial latency.
6. The write transaction shown demonstrates the Dn A byte and the Dn+1 B byte being masked. Only Dn B byte and Dn+1 A byte are modified in the array. Dn A byte and Dn+1 B byte remain unchanged.

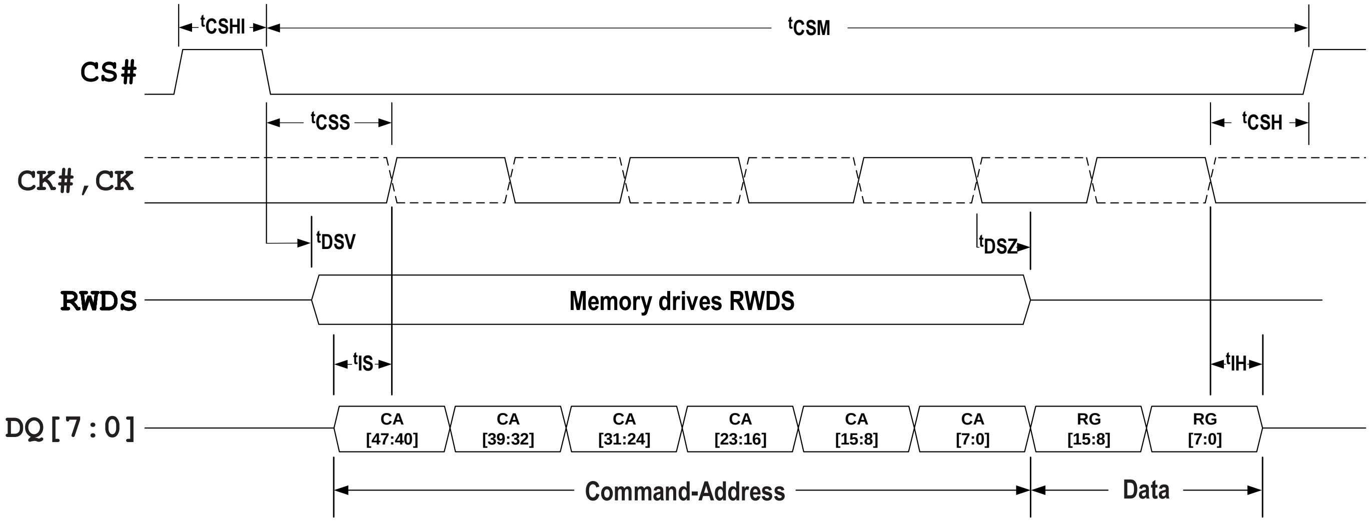


Figure 32 - Write Operation without Initial Latency (Register Write)

Notes:

1. Transactions must be initiated with CK=Low and CK#=High. CS# must return High before a new transaction is initiated.
2. Writes without Initial Latency, do not have a turnaround period for RWDS. The slave device will always drive RWDS during the Command-Address period to indicate whether extended latency is required for a transaction that has initial latency. However, the RWDS is driven before the slave device has received the first byte of CA, that is, before the slave knows whether the transaction is a read or write, to memory space or register space. In the case of a write without Initial Latency, the RWDS state during the CA period does not affect the Latency of Register Write. Since master write data immediately follows the Command-Address period in this case, the slave may continue to drive RWDS Low or may take RWDS to High-Z during write data transfer. The master must not drive RWDS during Register Write. Register Write do not use RWDS as a data mask function. All bytes of write data are written (full word writes).

12.3.3 Hybrid Sleep Timings

Table 23 - Hybrid Sleep Timing Parameters

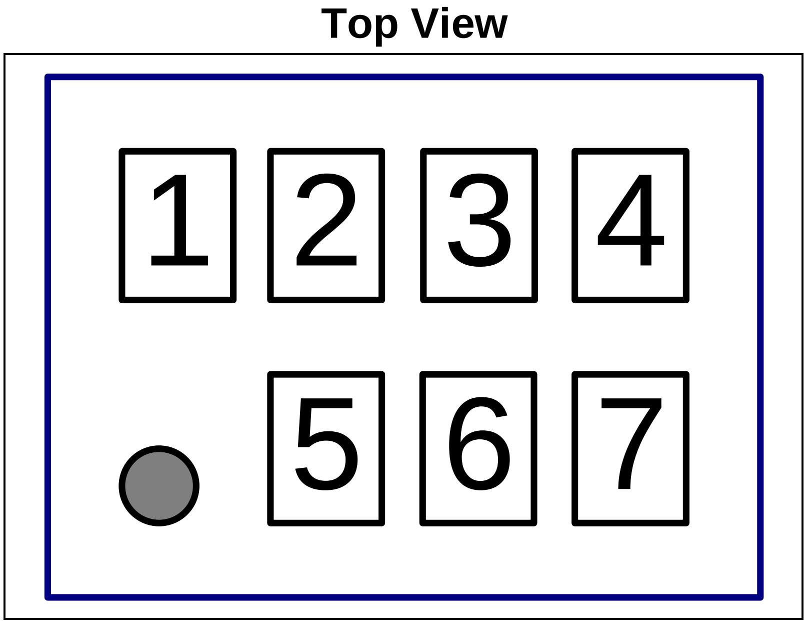
Description	Parameter	Min	Max	Unit
Hybrid Sleep CR1[5]=1 register write to Hybrid Sleep power level	t_{HSIN}	–	3	µS
CS# Pulse Width to Exit Hybrid Sleep	t_{CSHS}	60	3000	nS
CS# Exit Hybrid Sleep to Standby wakeup time	t_{EXTHS}	–	100	µS

12.3.4 Deep Power down Timings

Table 24 - Deep Power down Timing Parameters

Description	Parameter	Min	Max	Unit
Deep Power Down CR0[15]=0 register write to DPD power level	t_{DPDIN}	–	3	µS
CS# Pulse Width to Exit DPD	t_{CSDPD}	200	3000	nS
CS# Exit Deep Power Down to Standby wakeup time	t_{EXTDPD}	–	150	µS

13. WLCSP 15 BALL PACKAGE MARKING COMPOSITION



- **Digit 1: Part number code**

Part number code for part number

Code	Part number
1	-
2	-
3	W956D8MWSX5I
4	-
5	-
6	-

- **Digit 2, 3, 4: Serial number**

- **Digit 5: Year code**

Year code for year (For year 2020 to 2029)

Code	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**
Year	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029

- **Digit 6, 7: Week code**

Week code for week (Week by calendar year)

Code 6, 7	**01**	**02**	**03**	**……**	**31**	**32**	**……**	**53**	**54**
Week	1st week	2nd week	3rd week	……	31th week	32th week	……	53th week	54th week

14. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A01-001	Nov. 05, 2020	All	Initial formal datasheet
A01-002	Apr. 14, 2021	44	Update WLCSP 15 minimum and maximum dimension spec of length width
A01-003	Sep. 02, 2021	36	Remove DDR Input Timing Reference Levels for tIS and tIH figure
A01-004	Nov. 24, 2021	44	Add WLCSP 15 ball package marking composition information
A01-005	Mar. 07, 2022	44	Change W956D8MWSX5I part number code of section 3.2 WLCSP 15 Ball Package Marking Composition, Part number code for part number table (Digit 1: Part number code from 1 to 3)
A01-006	Mar. 14, 2023	43	Remove package outline drawing figure and dimensions spec portion and move it to another separated W956D8MW 64Mb HyperRAM WLCSP 15 package information document

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