NuMicro® Family
Arm® 32-bit Cortex®-M4 Microcontroller

M471V/M471K Series
Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

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1 GENERAL DESCRIPTION

The NuMicro® M471V/M471K series is a 32-bit microcontroller based on Arm Cortex-M4F core, with DSP instruction set and single-precision floating-point unit (FPU), targeted for smart home appliance applications. For the growing requirement of the safety functions on the home appliance, the M471V/M471K series provides certified Software Test Library (STL) and an application note for IEC60730-1 Class B Annex H. This certified STL can significantly reduce the development time and efforts to pass IEC60730-1 Class B certification for home appliances. The M471V/M471K series runs up to 120 MHz, and features 2.5V to 5.5V wide operating voltage, -40°C to 105°C wide operating temperature, a variety of packages with wide pin pitch, and excellent high immunity characteristics by ESD HBM 8 KV and EFT 4.4 KV, which greatly meet the rigid requirements for stability, reliability and safety of home appliance systems.

As the new smart function added on home appliances, the M471V/M471K series provides up to 512 KB dual-bank of Flash memory for code storage, 64 KB SRAM for run time operation and 32 KB independent Data Flash for parameters. The dual bank design of 512 KB Flash memory supports the Firmware update through the Over-The-Air (FOTA) process. Additionally, in response to the code security requirements, the M471V/M471K series supports Execute-Only Memory (XOM) function to protect confidential program code information from stealing in the run-time. Finally, the 32 KB independent data Flash provides a 256 Bytes page erasing unit to make the parameter data update and access more efficiently. In order to reduce the data access overhead of CPU core to peripherals, a peripheral direct memory access (PDMA) is provided.

The M471V/M471K series supports plenty of peripherals, including a Customize IR receiver (CIR) for remote controller, up to 24 channels of 16-bit PWM, 6 sets of UART, 2 sets of SPI/I²S, 2 sets of I²C, and a real-time clock (RTC).

The M471V/M471K series also provides rich analog peripherals including 2 sets of analog comparators, up to 24 channels of 12-bit SAR ADC, and 1 channel of 8-bit DAC. The M471V/M471K series also integrates a pseudo random number generator (PRNG) to support the requirement for encryption and decryption of smart home appliances.

For the development, Nuvoton provides the NuMaker-M471KI evaluation board, and Nuvoton Nu-Link debugger. The 3rd Party IDE such as Keil MDK, IAR EWARM, Eclippse IDE with GNU GCC compilers are also supported.

Product Line	Core (MHz)	PDMA	CRC	Timer (32-bit)	PWM	UART	I²C	QSPI/ SPI	ADC	ACMP	DAC	CIR	PRNG
M471V/M471K Series	120	√	√	4	24	6	2	SPI x2	24	2	1	√	√

Table 1-1 NuMicro® M471V/M471K Series Key Features Support Table

This series supports two package choices which are designed for home appliance PCB demands.

- LQFP100: 14 mm x 14 mm, pin pitch 0.5 mm
- LQFP128: 14 mm x 14 mm, pin pitch 0.4 mm

The NuMicro® M471V/M471K series is suitable for a wide range of applications such as:

- Washing Machine
- Refrigerator
- Air conditioner
- Air Purifier
- Other home appliances

2 FEATURES

2.1 NuMicro® M471V/M471K Features

Core and System	
Arm® Cortex®-M4	• Arm® Cortex®-M4 processor, running up to 120 MHz • Built-in Memory Protection Unit (MPU) • Built-in Nested Vectored Interrupt Controller (NVIC) • Hardware IEEE 754 compliant Floating-point Unit (FPU) • DSP extension with hardware divider and single-cycle 32-bit hardware multiplier • 24-bit system tick timer • Programmble and maskable interrupt • Low Power Sleep mode by WFI and WFE instructions
Brown-out Detector (BOD)	• Four-level BOD with brown-out interrupt and reset option (4.4V/3.7V/2.7V/2.4V)
Low Voltage Reset (LVR)	• LVR with 2.35V threshold voltage level
Security	• 96-bit Unique ID (UID). • 128-bit Unique Customer ID (UCID).
Memories	
Flash	• Two bank 512 KB on-chip Application ROM (APROM) • Supports FOTA function • 4 KB on-chip Flash for user-defined loader (LDROM) • 32 Kbytes data Flash which is rewritable in parallel with instruction execution • All on-chip Flash expect data Flash supporting 2048-byte page erase • Data Flash supporting 256-byte page erase • Fast Flash programming verification with CRC • On-chip Flash programming with In-Chip Programming (ICP), In-System Programming (ISP) and In-Application Programming (IAP) capabilities • Configurable boot up sources user-defined loader (LDROM) or Application ROM (APROM) • 2-wired ICP Flash updating through SWD interface • 32-bit/64-bit and multi-word Flash programming function
SRAM	• Up to 64 KB on-chip SRAM includes:

	• Byte-, half-word- and word-access • 32 KB with hardware parity check • Supports PDMA operation
Cyclic Redundancy Calculation (CRC)	• Supports CRC-CCITT, CRC-8, CRC-16 and CRC-32 polynomials • Programmable initial value and seed value • Programmable order reverse setting and one's complement setting for input data and CRC checksum • 8-bit, 16-bit, and 32-bit data width • 8-bit write mode with 1-AHB clock cycle operation • 16-bit write mode with 2-AHB clock cycle operation • 32-bit write mode with 4-AHB clock cycle operation • Uses PDMA to write data with performing CRC operation
Peripheral DMA (PDMA)	• Six independent and configurable channels for automatic data transfer between memories and peripherals • Basic and Scatter-Gather transfer modes • Each channel supports circular buffer management using Scatter-Gather Transfer mode • Fixed-priority and Round-robin priorities modes • Single and burst transfer types • Byte-, half-word- and word tranfer unit with count up to 65536 • Incremental or fixed source and destination address
Pseudo Random Number Generator (PRNG)	• Supports 64 bits, 128 bits, 192 bits, and 256 bits random number generation.
Clocks	
External Clock Source	• 4~24 MHz High-speed eXternal crystal oscillator (HXT) for precise timing operation • 32.768 kHz Low-speed eXternal crystal oscillator (LXT) for RTC function and low-power system operation • Supports clock failure detection for external crystal oscillators and exception generatation (NMI)
Internal Clock Source	• 38 kHz Low-speed Internal RC oscillator (LIRC) for watchdog timer and wakeup operation • 48 MHz High-speed Internal RC oscillator (HIRC) trimmed to 1% accuracy at -20 to 85°C • Up to 120 MHz on-chip PLL, sourced from HIRC or HXT, allowing CPU operation up to the maximum CPU frequency without the need for a high-frequency crystal
Real-Time Clock (RTC)	• The RTC clock source is from Low-speed external crystal

	• Able to wake up CPU from any reduced power mode • Supports ±5 ppm within 5 seconds software clock accuracy compensation • Supports Alarm registers (second, minute, hour, day, month, year) • Supports RTC Time Tick and Alarm Match interrupt • Automatic leap year recognition • Supports 1 Hz clock output for calibration
Timers	
32-bit Timer	**TIMER** • 4 sets of 32-bit timers with 24-bit up counters and 8-bit prescale counters • Independent clock source for each timer • One-shot, Periodic, Toggle and Continuous Counting operation modes • Event counting function to count the event from external pin • Input capture function to capture or reset counter value • External capture pin event for interval measurement • External capture pin event to reset 24-bit up counter • Chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated • Timer interrupt flag or external capture interrupt flag to trigger BPWM, EPWM, EADC, DAC and PDMA • Internal capture triggered source from ACMP output • Inter-Timer trigger capture mode **PWM** • 16-bit compare register and period register • Double buffer for period register and compare register • Supports inverse in PWM output • PWM interrupt wake-up from system Power-down mode
Enhanced PWM (EPWM)	• 16-bit counters with 12-bit clock presacle supporting 12 PWM output channels • Up to 12 independent input capture channels with 16-bit resolution counter • Supports dead time with maximum divided 12-bit prescale • Up, down or up-down PWM counter type • Supports complementary mode for 3 complementary paired PWM output channels • Synchronous function for phase control • Counter synchronous start function • Brake function with auto recovery mechanism • Mask function and tri-state output for each PWM channel

	• Trigger EADC or DAC to start conversion immediately • Trigger EADC to start conversion after a short delay • Hardware short-circuit output check
Basic PWM (BPWM)	• 16-bit counters with 12-bit clock presacle supporting 12 PWM output channels • Up to 12 independent input capture channels with 16-bit resolution counter • Up, down or up-down PWM counter type • Counter synchronous start function • Complementary mode for 6 complementary paired PWM output channels • Mask function and tri-state output for each PWM channel • Able to trigger EADC to start conversion
Watchdog	• 18-bit free running up counter for WDT time-out interval • Supports multiple clock sources from LIRC (default selection), HCLK/2048 and LXT with 8 selectable time-out period • Able to wake up system from Power-down or Idle mode • Time-out event to trigger interrupt or reset system • Supports four WDT reset delay periods, including 1026, 130, 18 or 3 WDT_CLK reset delay period • Configured to force WDT enabled on chip power-on or reset
Window Watchdog	• Clock sourced from HCLK/2048 or LIRC; the window set by 6-bit counter with 11-bit prescale • Suspended in Idle/Power-down mode
Analog Interfaces	
Enhanced Analog-to-Digital Converter (EADC)	• One 12-bit, 24-ch 1.895 MSPS SAR EADC with up to 24 single-ended input channels or 1 differential input pair; 10-bit accuracy is guaranteed • Three internal channels for band-gap VBG input, Temperature sensor input and DAC input • Supports external V_{REF} pin or internal reference voltage • Analog-to-Digital conversion can be triggered by software enable, external pin, Timer 0~3 overflow pulse trigger or PWM trigger • Configurable EADC sampling time • Double data buffers for sample module 0~3 • Supports PDMA operation
Digital-to-Analog Converter (DAC)	• One 8-bit, 200 KSPS voltage type DAC without buffer • Reference voltage can be switched from AV_{DD}, V_{REF} pin and Internal reference voltage • The trigger of the DAC conversion can be done by the software,

	external triggers or timer0 to timer3, EPWM0 • Available for monitoring by the ACMP • PDMA operation
Analog Comparator (ACMP)	• Two Analog Comparators • Supports four multiplexed I/O pins at positive input • Supports one I/O pin, band-gap voltage, DAC voltage output, internal voltage reference, and 16-level voltage divider from AV_{DD} or V_{REF} at negative input • Supports wake up from Power-down by interrput • Supports triggers for brake events and cycle-by-cycle control for PWM • Supports window compare mode and window latch mode • Supports programmable hysteresis window: 20 mV and 40 mV

Internal reference voltage	• One Internal reference voltage with 2.048V, 2.560V, 3.072V, 4.096V
	• Can be configured to supply a reference voltage to the following:
	  • ADC reference Voltage
	  • DAC reference Voltage
	  • Comparator negative input

Temperature sensor	• One built-in temperature sensor with 1°C resolution
Communication Interfaces	
Low-power UART	• Six Low-power UARTs with up to 2 MHz baud rate • Auto-Baud Rate measurement and baud rate compensation function • Supports low power UART (LPUART): baud rate clock from LXT(32.768 kHz) with 9600bps in Power-down mode even system clock is stopped • UART0/UART1 supporting 16-byte FIFOs with programmable level trigger • UART2/UART3/UART4/UART5 supporting 1-byte FIFOs with programmable level trigger • Auto flow control (nCTS and nRTS) • Supports IrDA (SIR) function on UART0/UART1 • Supports LIN function on UART0/UART1 • Supports RS-485 9-bit mode and direction control • Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function in idle mode • Supports hardware or software enabled to program nRTS pin to control RS-485 transmission direction

	• Supports wake-up function • 8-bit receiver FIFO time-out detection function • Supports break error, frame error, parity error and receive/transmit FIFO overflow detection function • PDMA operation
I²C	• Two sets of I²C devices with Master/Slave mode • Supports Standard mode (100 kbps), Fast mode (400 kbps), Fast mode plus (1 Mbps) • Programmable clocks allowing for versatile rate control • Supports multiple address recognition (four slave address with mask option) • Supports SMBus and PMBus • Supports multi-address power-down wake-up function • PDMA operation
SPI/I²S	• Two SPI/I²S controllers with Master/Slave mode • SPI/I²S provides separate 4-level of 32-bit (or 8-level of 16-bit) transmit and receive FIFO buffers **SPI** • Up to 24 MHz in Master mode • Configurable bit length of a transfer word from 8 to 32-bit • MSB first or LSB first transfer sequence • Byte reorder function • Supports Byte or Word Suspend mode • Supports one data channel half-duplex transfer • Supports receive-only mode **I²S** • Supports mono and stereo audio data with 8-, 16-, 24- and 32-bit audio data sizes • Supports PCM mode A, PCM mode B, I²S and MSB justified data format • PDMA operation
Customize IR Receiver (CIR)	• 1 channel • Four pattern matching (header, data 0, data 1, and special data detection) • 8-byte receive buffer per unit
GPIO	• Supports four I/O modes: Quasi bi-direction, Push-Pull output, Open-Drain output and Input only with high impendence mode • Selectable TTL/Schmitt trigger input • Configured as interrupt source with edge/level trigger setting • Supports independent pull-up control

- Supports high driver and high sink current I/O
- Supports software selectable slew rate control

3 PARTS INFORMATION

3.1 Package Type

Part No.	LQFP100	LQFP128
M471V/M471K	M471VI8AE M471VG7AE	M471KI8AE

3.2 NuMicro® M471V/M471K Selection Guide

PART NUMBER		M471		
		VG7AE	VI8AE	KI8AE
Flash (KB)		256 (dual bank)	512 (dual bank)	512 (dual bank)
SRAM (KB)		48 (32 KB hardware parity check)	64 (32 KB hardware parity check)	64 (32 KB hardware parity check)
Data Flash (KB)		32		
LDROM (KB)		4		
XOM (regions)		4		
System Frequency (MHz)		120		
I/O		91		119
32-bit Timer		4		
Customize IR Receiver		√		
Connectivity	UART	6		
	SPI/I²S	2		
	I²C	2		
16-bit EPWM		12		
16-bit BPWM		12		
PMDA		6-ch		
RTC		√		
12-bit ADC		23		24
8-bit DAC		1		
Analog Comparator		2		
PRNG		√		
Package		LQFP 100 (14x14mm)		LQFP 128 (14x14mm)

3.3 NuMicro® M471V/M471K Naming Rule

M4	71	K	I	8	A	E
Core	**Series**	**Package**	**Flash Size**	**SRAM Size**	**Revision**	**Temperature**
Cortex®-M4F	71: Base	V: LQFP100 (14x14 mm) K: LQFP128 (14x14 mm)	G: 256 KB I: 512 KB	7: 48 KB 8: 64 KB		E:-40˚C ~ 105˚C

4 PIN CONFIGURATION

Users can find pin configuaration information in the Multi-function Pin Diagram section or by using NuTool - PinConfig. The NuTool - PinConfig contains all Nuvoton NuMicro® Family chip series with all part number, and helps users configure GPIO multi-function correctly and handily.

4.1 Pin Configuration

4.1.1 Pin Diagram

4.1.1.1 LQFP100 Pin Diagram

Corresponding Part Number: M471VI8AE, M471VG7AE

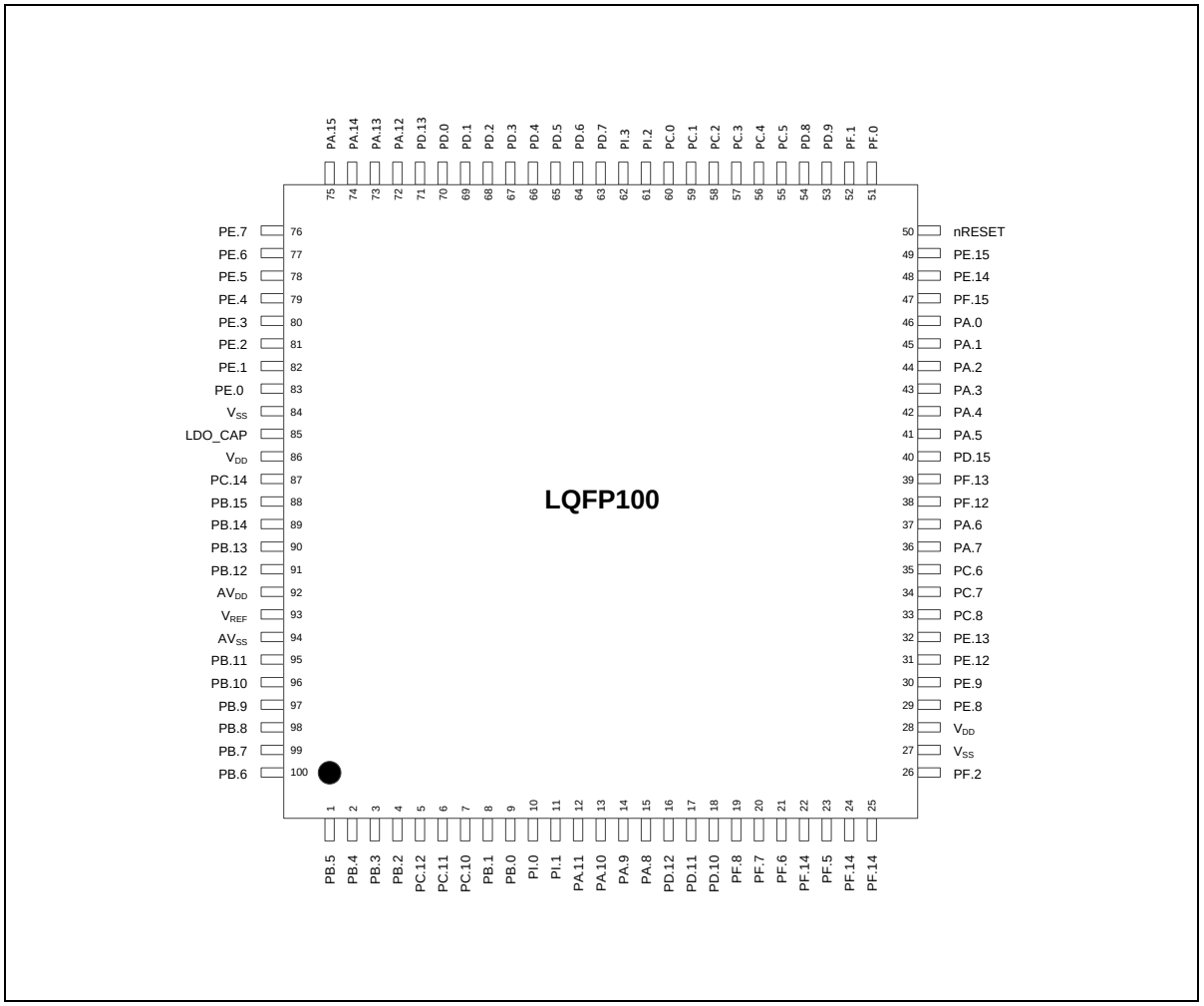


Figure 4.1-1 LQFP 100-pin Diagram

4.1.1.2 LQFP128 Pin Diagram

Corresponding Part Number: M471KI8AE

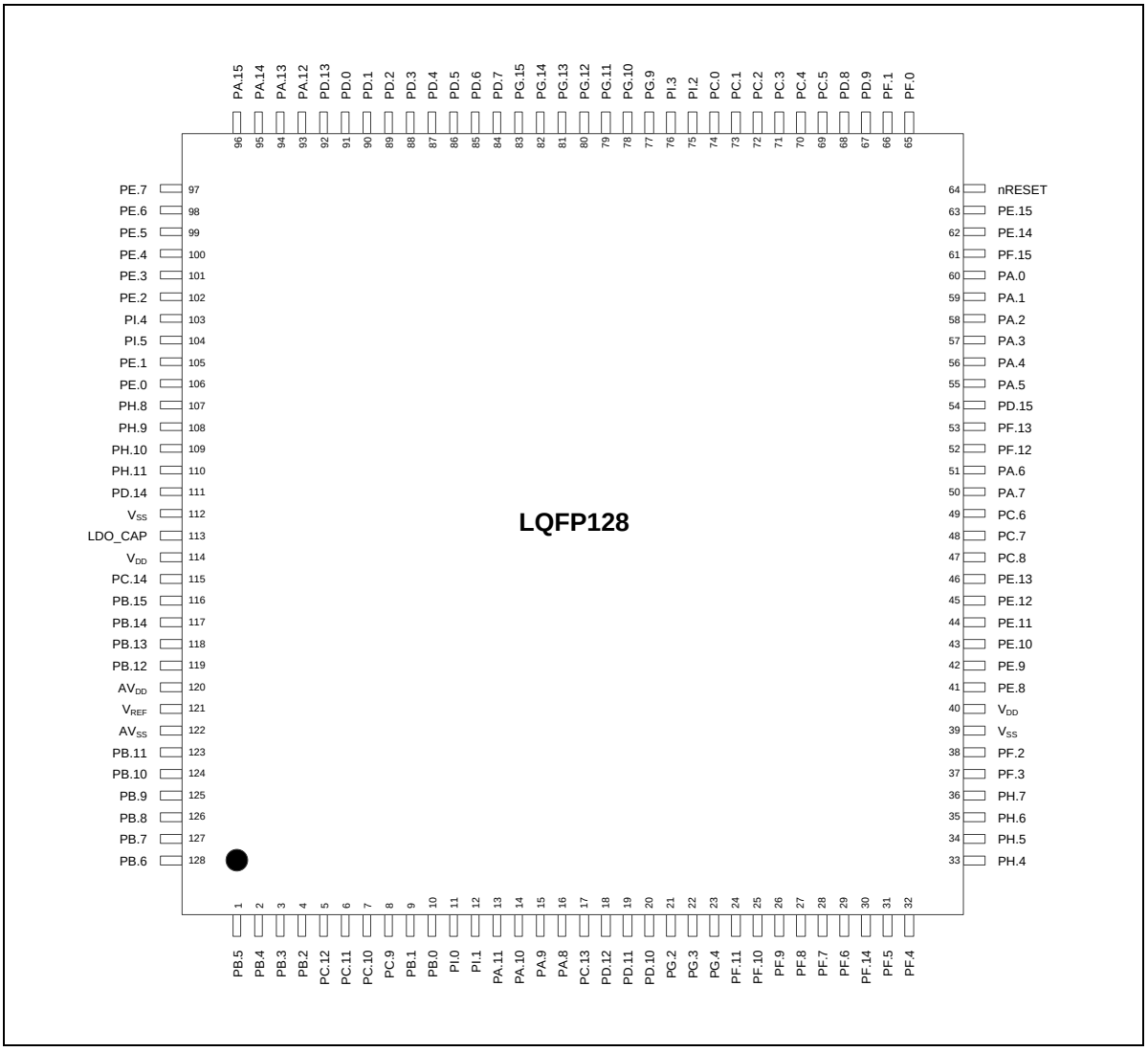


Figure 4.1-2 LQFP 128-pin Diagram

4.1.2 Multi-function Pin Diagram

4.1.2.1 LQFP-100 Pin Multi-function Pin Diagram

Corresponding Part Number: M471VI8AE, M471VG7AE

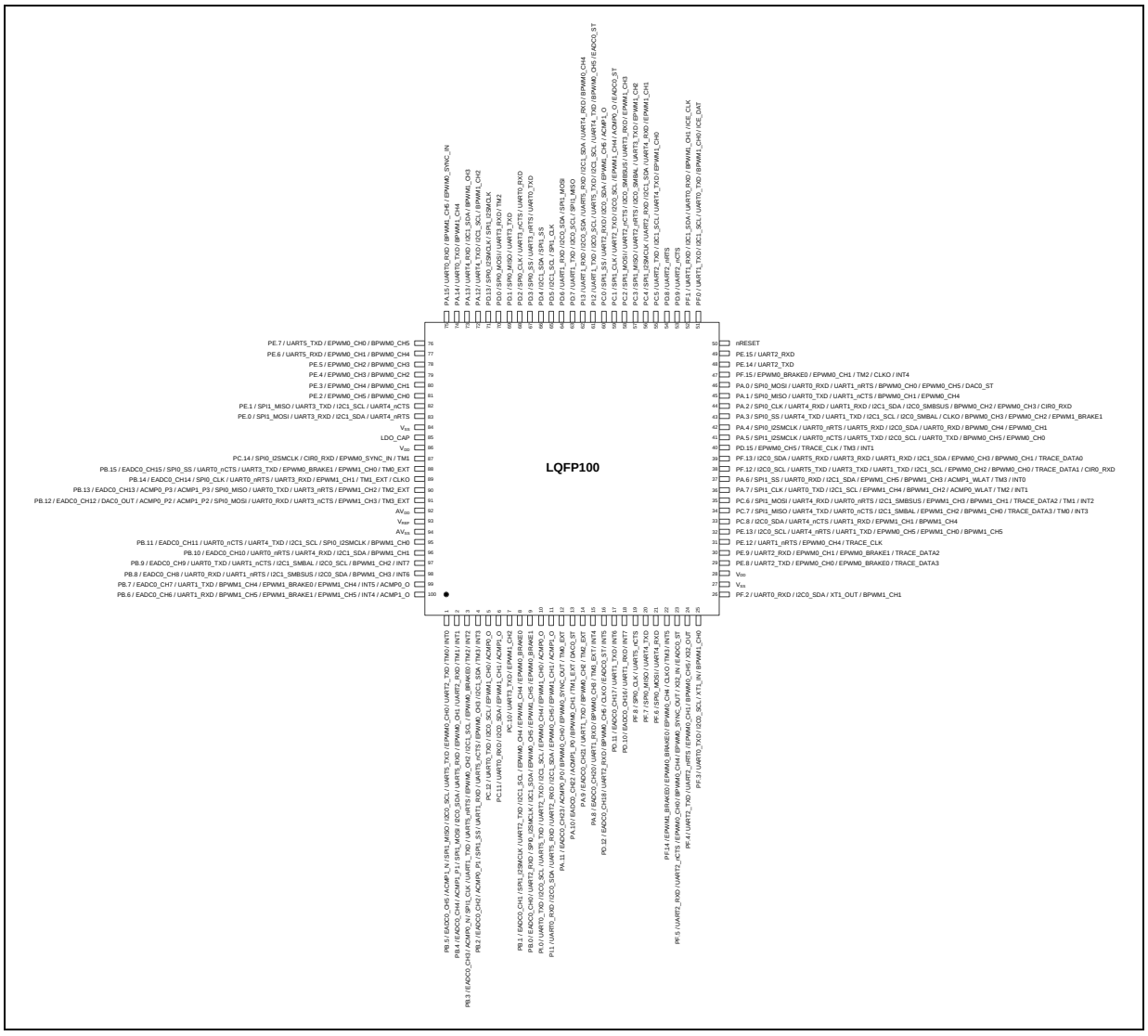


Figure 4.1-3 LQFP 100-pin Multi-function Pin Diagram

4.1.2.2 LQFP-128 Pin Multi-function Pin Diagram

Corresponding Part Number: M471KI8AE

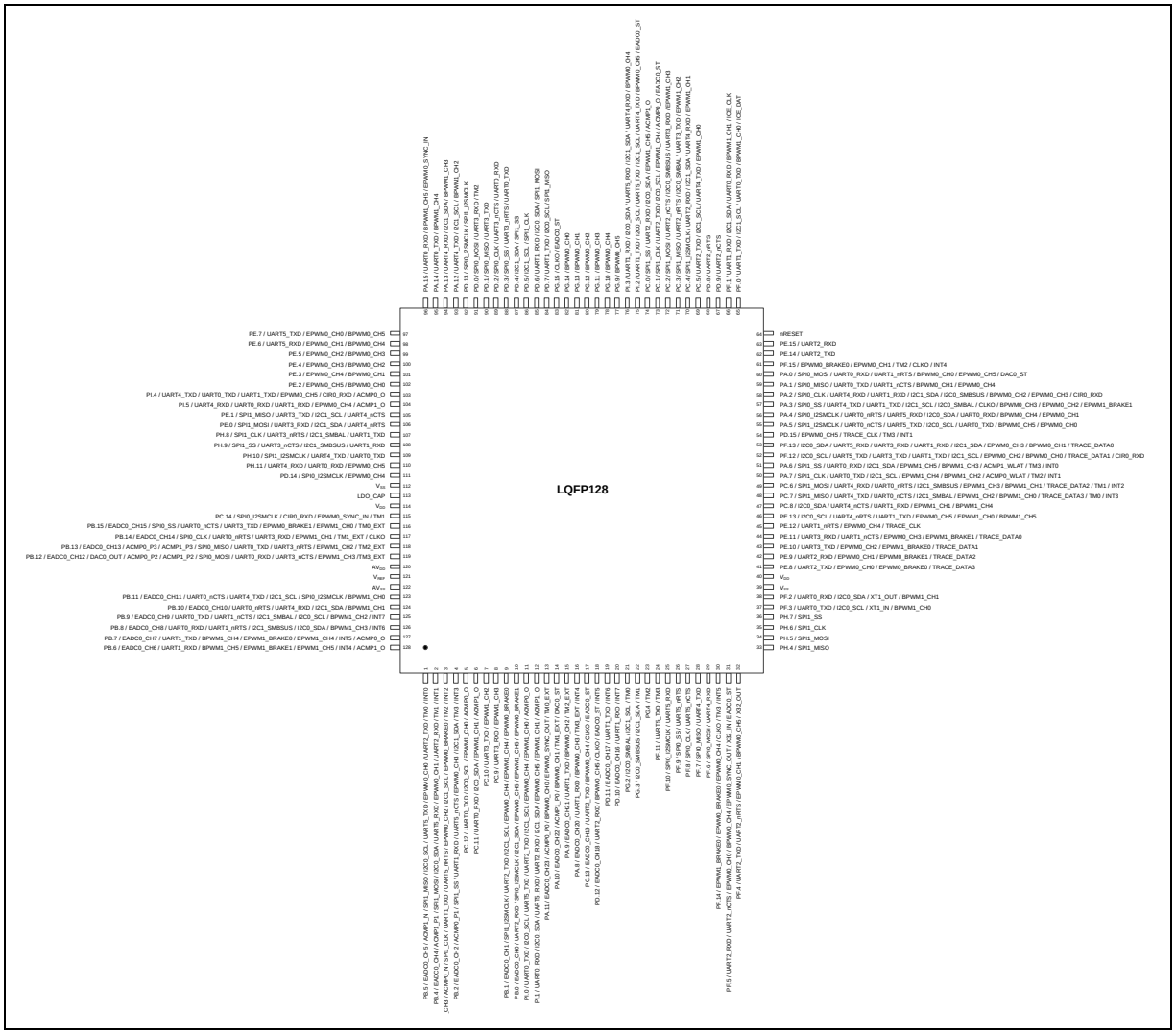


Figure 4.1-4 LQFP 128-pin Multi-function Pin Diagram

4.2 Pin Mapping

Different part number with same package might has different function. Please refer to the selection guide in section 3.2, Pin Configuration in section 4.1 or NuTool - PinConfig.

Corresponding Part Number: M471VI8AE, M471VG7AE, M471KI8AE

	M471	
Pin Name	100 Pin	128 Pin
PB.5	1	1
PB.4	2	2
PB.3	3	3
PB.2	4	4
PC.12	5	5
PC.11	6	6
PC.10	7	7
PC.9		8
PB.1	8	9
PB.0	9	10
PI.0	10	11
PI.1	11	12
PA.11	12	13
PA.10	13	14
PA.9	14	15
PA.8	15	16
PC.13		17
PD.12	16	18
PD.11	17	19
PD.10	18	20
PG.2		21
PG.3		22
PG.4		23
PF.11		24
PF.10		25
PF.9		26
PF.8	19	27
PF.7	20	28
PF.6	21	29

PF.14	22	30
PF.5	23	31
PF.4	24	32
PH.4		33
PH.5		34
PH.6		35
PH.7		36
PF.3	25	37
PF.2	26	38
V_{SS}	27	39
V_{DD}	28	40
PE.8	29	41
PE.9	30	42
PE.10		43
PE.11		44
PE.12	31	45
PE.13	32	46
PC.8	33	47
PC.7	34	48
PC.6	35	49
PA.7	36	50
PA.6	37	51
PF.12	38	52
PF.13	39	53
PD.15	40	54
PA.5	41	55
PA.4	42	56
PA.3	43	57
PA.2	44	58
PA.1	45	59
PA.0	46	60
PF.15	47	61
PE.14	48	62
PE.15	49	63
nRESET	50	64

PF.0	51	65
PF.1	52	66
PD.9	53	67
PD.8	54	68
PC.5	55	69
PC.4	56	70
PC.3	57	71
PC.2	58	72
PC.1	59	73
PC.0	60	74
PI.2	61	75
PI.3	62	76
PG.9		77
PG.10		78
PG.11		79
PG.12		80
PG.13		81
PG.14		82
PG.15		83
PD.7	63	84
PD.6	64	85
PD.5	65	86
PD.4	66	87
PD.3	67	88
PD.2	68	89
PD.1	69	90
PD.0	70	91
PD.13	71	92
PA.12	72	93
PA.13	73	94
PA.14	74	95
PA.15	75	96
PE.7	76	97
PE.6	77	98
PE.5	78	99

PE.4	79	100
PE.3	80	101
PE.2	81	102
PI.4		103
PI.5		104
PE.1	82	105
PE.0	83	106
PH.8		107
PH.9		108
PH.10		109
PH.11		110
PD.14		111
V_{SS}	84	112
LDO_CAP	85	113
V_{DD}	86	114
PC.14	87	115
PB.15	88	116
PB.14	89	117
PB.13	90	118
PB.12	91	119
AV_{DD}	92	120
V_{REF}	93	121
AV_{SS}	94	122
PB.11	95	123
PB.10	96	124
PB.9	97	125
PB.8	98	126
PB.7	99	127
PB.6	100	128

4.3 Pin Functional Description

Corresponding Part Number: M471VI8AE, M471VG7AE, M471KI8AE

4.3.1 Multi-function Summary Table

Group	Pin Name	GPIO	MFP	Type	Description
ACMP0	ACMP0_N	PB.3	MFP1	A	Analog comparator 0 negative input pin.
	ACMP0_O	PC.12	MFP14	O	Analog comparator 0 output pin.
		PI.0	MFP14	O	
		PC.1	MFP14	O	
		PI.4	MFP15	O	
		PB.7	MFP15	O	
	ACMP0_P0	PA.11	MFP1	A	Analog comparator 0 positive input 0 pin.
	ACMP0_P1	PB.2	MFP1	A	Analog comparator 0 positive input 1 pin.
	ACMP0_P2	PB.12	MFP1	A	Analog comparator 0 positive input 2 pin.
	ACMP0_P3	PB.13	MFP1	A	Analog comparator 0 positive input 3 pin.
	ACMP0_WLAT	PA.7	MFP13	I	Analog comparator 0 window latch input pin
ACMP1	ACMP1_N	PB.5	MFP1	A	Analog comparator 1 negative input pin.
	ACMP1_O	PC.11	MFP14	O	Analog comparator 1 output pin.
		PI.1	MFP14	O	
		PC.0	MFP14	O	
		PI.5	MFP15	O	
		PB.6	MFP15	O	
	ACMP1_P0	PA.10	MFP1	A	Analog comparator 1 positive input 0 pin.
	ACMP1_P1	PB.4	MFP1	A	Analog comparator 1 positive input 1 pin.
	ACMP1_P2	PB.12	MFP1	A	Analog comparator 1 positive input 2 pin.
	ACMP1_P3	PB.13	MFP1	A	Analog comparator 1 positive input 3 pin.
	ACMP1_WLAT	PA.6	MFP13	I	Analog comparator 1 window latch input pin
BPWM0	BPWM0_CH0	PA.11	MFP9	I/O	BPWM0 channel 0 output/capture input.
		PF.12	MFP11	I/O	
		PA.0	MFP12	I/O	
		PG.14	MFP12	I/O	
		PE.2	MFP13	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
	BPWM0_CH1	PA.10	MFP9	I/O	BPWM0 channel 1 output/capture input.
		PF.13	MFP11	I/O	
		PA.1	MFP12	I/O	
		PG.13	MFP12	I/O	
		PE.3	MFP13	I/O	
	BPWM0_CH2	PA.9	MFP9	I/O	BPWM0 channel 2 output/capture input.
		PA.2	MFP12	I/O	
		PG.12	MFP12	I/O	
		PE.4	MFP13	I/O	
	BPWM0_CH3	PA.8	MFP9	I/O	BPWM0 channel 3 output/capture input.
		PA.3	MFP12	I/O	
		PG.11	MFP12	I/O	
		PE.5	MFP13	I/O	
	BPWM0_CH4	PC.13	MFP9	I/O	BPWM0 channel 4 output/capture input.
		PF.5	MFP8	I/O	
		PA.4	MFP12	I/O	
		PI.3	MFP12	I/O	
		PG.10	MFP12	I/O	
		PE.6	MFP13	I/O	
	BPWM0_CH5	PD.12	MFP9	I/O	BPWM0 channel 5 output/capture input.
		PF.4	MFP8	I/O	
		PA.5	MFP12	I/O	
		PI.2	MFP12	I/O	
		PG.9	MFP12	I/O	
		PE.7	MFP13	I/O	
BPWM1	BPWM1_CH0	PF.3	MFP11	I/O	BPWM1 channel 0 output/capture input.
		PC.7	MFP12	I/O	
		PF.0	MFP12	I/O	
		PB.11	MFP10	I/O	
	BPWM1_CH1	PF.2	MFP11	I/O	BPWM1 channel 1 output/capture input.
		PC.6	MFP12	I/O	
		PF.1	MFP12	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
		PB.10	MFP10	I/O	
	BPWM1_CH2	PA.7	MFP12	I/O	BPWM1 channel 2 output/capture input.
		PA.12	MFP11	I/O	
		PB.9	MFP10	I/O	
	BPWM1_CH3	PA.6	MFP12	I/O	BPWM1 channel 3 output/capture input.
		PA.13	MFP11	I/O	
		PB.8	MFP10	I/O	
	BPWM1_CH4	PC.8	MFP12	I/O	BPWM1 channel 4 output/capture input.
		PA.14	MFP11	I/O	
		PB.7	MFP10	I/O	
	BPWM1_CH5	PE.13	MFP12	I/O	BPWM1 channel 5 output/capture input.
		PA.15	MFP11	I/O	
		PB.6	MFP10	I/O	
CIR0	CIR0_RXD	PF.12	MFP15	I	CIR0 data receiver input pin.
		PA.2	MFP15	I	
		PI.4	MFP14	I	
		PC.14	MFP10	I	
CLKO	CLKO	PC.13	MFP13	O	Clock Out
		PD.12	MFP13	O	
		PF.14	MFP13	O	
		PA.3	MFP11	O	
		PF.15	MFP14	O	
		PG.15	MFP14	O	
		PB.14	MFP14	O	
DAC0	DAC0_OUT	PB.12	MFP1	A	DAC0 channel analog output.
	DAC0_ST	PA.10	MFP14	I	DAC0 external trigger input.
		PA.0	MFP15	I	
EADC0	EADC0_CH0	PB.0	MFP1	A	EADC0 channel 0 analog input.
	EADC0_CH1	PB.1	MFP1	A	EADC0 channel 1 analog input.
	EADC0_CH2	PB.2	MFP1	A	EADC0 channel 2 analog input.
	EADC0_CH3	PB.3	MFP1	A	EADC0 channel 3 analog input.
	EADC0_CH4	PB.4	MFP1	A	EADC0 channel 4 analog input.

Group	Pin Name	GPIO	MFP	Type	Description
	EADC0_CH5	PB.5	MFP1	A	EADC0 channel 5 analog input.
	EADC0_CH6	PB.6	MFP1	A	EADC0 channel 6 analog input.
	EADC0_CH7	PB.7	MFP1	A	EADC0 channel 7 analog input.
	EADC0_CH8	PB.8	MFP1	A	EADC0 channel 8 analog input.
	EADC0_CH9	PB.9	MFP1	A	EADC0 channel 9 analog input.
	EADC0_CH10	PB.10	MFP1	A	EADC0 channel 10 analog input.
	EADC0_CH11	PB.11	MFP1	A	EADC0 channel 11 analog input.
	EADC0_CH12	PB.12	MFP1	A	EADC0 channel 12 analog input.
	EADC0_CH13	PB.13	MFP1	A	EADC0 channel 13 analog input.
	EADC0_CH14	PB.14	MFP1	A	EADC0 channel 14 analog input.
	EADC0_CH15	PB.15	MFP1	A	EADC0 channel 15 analog input.
	EADC0_CH16	PD.10	MFP1	A	EADC0 channel 16 analog input.
	EADC0_CH17	PD.11	MFP1	A	EADC0 channel 17 analog input.
	EADC0_CH18	PD.12	MFP1	A	EADC0 channel 18 analog input.
	EADC0_CH19	PC.13	MFP1	A	EADC0 channel 19 analog input.
	EADC0_CH20	PA.8	MFP1	A	EADC0 channel 20 analog input.
	EADC0_CH21	PA.9	MFP1	A	EADC0 channel 21 analog input.
	EADC0_CH22	PA.10	MFP1	A	EADC0 channel 22 analog input.
	EADC0_CH23	PA.11	MFP1	A	EADC0 channel 23 analog input.
	EADC0_ST	PC.13	MFP14	I	EADC0 external trigger input.
		PD.12	MFP14	I	
		PF.5	MFP11	I	
		PC.1	MFP15	I	
		PI.2	MFP15	I	
		PG.15	MFP15	I	
EPWM0	EPWM0_BRAKE0	PB.3	MFP13	I	EPWM0 Brake 0 input pin.
		PB.1	MFP13	I	
		PF.14	MFP10	I	
		PE.8	MFP11	I	
		PF.15	MFP11	I	
	EPWM0_BRAKE1	PB.0	MFP13	I	EPWM0 Brake 1 input pin.
		PE.9	MFP11	I	

Group	Pin Name	GPIO	MFP	Type	Description
		PB.15	MFP10	I	
	EPWM0_CH0	PB.5	MFP11	I/O	EPWM0 channel 0 output/capture input.
		PF.5	MFP7	I/O	
		PE.8	MFP10	I/O	
		PA.5	MFP13	I/O	
		PE.7	MFP12	I/O	
	EPWM0_CH1	PB.4	MFP11	I/O	EPWM0 channel 1 output/capture input.
		PF.4	MFP7	I/O	
		PE.9	MFP10	I/O	
		PA.4	MFP13	I/O	
		PF.15	MFP12	I/O	
		PE.6	MFP12	I/O	
	EPWM0_CH2	PB.3	MFP11	I/O	EPWM0 channel 2 output/capture input.
		PE.10	MFP10	I/O	
		PF.12	MFP10	I/O	
		PA.3	MFP13	I/O	
		PE.5	MFP12	I/O	
	EPWM0_CH3	PB.2	MFP11	I/O	EPWM0 channel 3 output/capture input.
		PE.11	MFP10	I/O	
		PF.13	MFP10	I/O	
		PA.2	MFP13	I/O	
		PE.4	MFP12	I/O	
	EPWM0_CH4	PB.1	MFP11	I/O	EPWM0 channel 4 output/capture input.
		PI.0	MFP11	I/O	
		PF.14	MFP12	I/O	
		PE.12	MFP10	I/O	
		PA.1	MFP13	I/O	
		PE.3	MFP12	I/O	
		PI.5	MFP11	I/O	
		PD.14	MFP11	I/O	
	EPWM0_CH5	PB.0	MFP11	I/O	EPWM0 channel 5 output/capture input.
		PI.1	MFP11	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
		PE.13	MFP10	I/O	
		PD.15	MFP12	I/O	
		PA.0	MFP13	I/O	
		PE.2	MFP12	I/O	
		PI.4	MFP11	I/O	
		PH.11	MFP11	I/O	
	EPWM0_SYNC_IN	PA.15	MFP12	I	EPWM0 counter synchronous trigger input pin.
		PC.14	MFP11	I	
	EPWM0_SYNC_OUT	PA.11	MFP10	O	EPWM0 counter synchronous trigger output pin.
		PF.5	MFP9	O	
EPWM1	EPWM1_BRAKE0	PF.14	MFP9	I	EPWM1 Brake 0 input pin.
		PE.10	MFP11	I	
		PB.7	MFP11	I	
	EPWM1_BRAKE1	PE.11	MFP11	I	EPWM1 Brake 1 input pin.
		PA.3	MFP15	I	
		PB.6	MFP11	I	
	EPWM1_CH0	PC.12	MFP12	I/O	EPWM1 channel 0 output/capture input.
		PI.0	MFP12	I/O	
		PE.13	MFP11	I/O	
		PC.5	MFP12	I/O	
		PB.15	MFP11	I/O	
	EPWM1_CH1	PC.11	MFP12	I/O	EPWM1 channel 1 output/capture input.
		PI.1	MFP12	I/O	
		PC.8	MFP11	I/O	
		PC.4	MFP12	I/O	
		PB.14	MFP11	I/O	
	EPWM1_CH2	PC.10	MFP12	I/O	EPWM1 channel 2 output/capture input.
		PC.7	MFP11	I/O	
		PC.3	MFP12	I/O	
		PB.13	MFP11	I/O	
	EPWM1_CH3	PC.9	MFP12	I/O	EPWM1 channel 3 output/capture input.
		PC.6	MFP11	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
		PC.2	MFP12	I/O	
		PB.12	MFP11	I/O	
	EPWM1_CH4	PB.1	MFP12	I/O	EPWM1 channel 4 output/capture input.
		PA.7	MFP11	I/O	
		PC.1	MFP12	I/O	
		PB.7	MFP12	I/O	
	EPWM1_CH5	PB.0	MFP12	I/O	EPWM1 channel 5 output/capture input.
		PA.6	MFP11	I/O	
		PC.0	MFP12	I/O	
		PB.6	MFP12	I/O	
I2C0	I2C0_SCL	PB.5	MFP6	I/O	I^2C0 clock pin.
		PC.12	MFP4	I/O	
		PI.0	MFP4	I/O	
		PF.3	MFP4	I/O	
		PE.13	MFP4	I/O	
		PF.12	MFP4	I/O	
		PA.5	MFP9	I/O	
		PC.1	MFP9	I/O	
		PI.2	MFP4	I/O	
		PD.7	MFP4	I/O	
		PB.9	MFP9	I/O	
	I2C0_SDA	PB.4	MFP6	I/O	I^2C0 data input/output pin.
		PC.11	MFP4	I/O	
		PI.1	MFP4	I/O	
		PF.2	MFP4	I/O	
		PC.8	MFP4	I/O	
		PF.13	MFP4	I/O	
		PA.4	MFP9	I/O	
		PC.0	MFP9	I/O	
		PI.3	MFP4	I/O	
		PD.6	MFP4	I/O	
		PB.8	MFP9	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
	I2C0_SMBAL	PG.2	MFP4	O	I²C0 SMBus SMBALTER pin
		PA.3	MFP10	O	
		PC.3	MFP9	O	
	I2C0_SMBSUS	PG.3	MFP4	O	I²C0 SMBus SMBSUS pin (PMBus CONTROL pin)
		PA.2	MFP10	O	
		PC.2	MFP9	O	
I2C1	I2C1_SCL	PB.3	MFP12	I/O	I²C1 clock pin.
		PB.1	MFP9	I/O	
		PI.0	MFP9	I/O	
		PG.2	MFP5	I/O	
		PA.7	MFP8	I/O	
		PF.12	MFP9	I/O	
		PA.3	MFP9	I/O	
		PF.0	MFP3	I/O	
		PC.5	MFP9	I/O	
		PI.2	MFP9	I/O	
		PD.5	MFP4	I/O	
		PA.12	MFP4	I/O	
		PE.1	MFP8	I/O	
		PB.11	MFP7	I/O	
	I2C1_SDA	PB.2	MFP12	I/O	I²C1 data input/output pin.
		PB.0	MFP9	I/O	
		PI.1	MFP9	I/O	
		PG.3	MFP5	I/O	
		PA.6	MFP8	I/O	
		PF.13	MFP9	I/O	
		PA.2	MFP9	I/O	
		PF.1	MFP3	I/O	
		PC.4	MFP9	I/O	
		PI.3	MFP9	I/O	
		PD.4	MFP4	I/O	
		PA.13	MFP4	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
		PE.0	MFP8	I/O	
		PB.10	MFP7	I/O	
	I2C1_SMBAL	PC.7	MFP8	O	I^2C1 SMBus SMBALTER pin
		PH.8	MFP8	O	
		PB.9	MFP7	O	
	I2C1_SMBSUS	PC.6	MFP8	O	I^2C1 SMBus SMBSUS pin (PMBus CONTROL pin)
		PH.9	MFP8	O	
		PB.8	MFP7	O	
ICE	ICE_CLK	PF.1	MFP14	I	Serial wired debugger clock pin. Note: It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
	ICE_DAT	PF.0	MFP14	I/O	Serial wired debugger data pin. Note: It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
INT0	INT0	PB.5	MFP15	I	External interrupt 0 input pin.
		PA.6	MFP15	I	
INT1	INT1	PB.4	MFP15	I	External interrupt 1 input pin.
		PA.7	MFP15	I	
		PD.15	MFP15	I	
INT2	INT2	PB.3	MFP15	I	External interrupt 2 input pin.
		PC.6	MFP15	I	
INT3	INT3	PB.2	MFP15	I	External interrupt 3 input pin.
		PC.7	MFP15	I	
INT4	INT4	PA.8	MFP15	I	External interrupt 4 input pin.
		PF.15	MFP15	I	
		PB.6	MFP13	I	
INT5	INT5	PD.12	MFP15	I	External interrupt 5 input pin.
		PF.14	MFP15	I	
		PB.7	MFP13	I	
INT6	INT6	PD.11	MFP15	I	External interrupt 6 input pin.
		PB.8	MFP13	I	
INT7	INT7	PD.10	MFP15	I	External interrupt 7 input pin.
		PB.9	MFP13	I	

Group	Pin Name	GPIO	MFP	Type	Description
SPI0	SPI0_CLK	PF.8	MFP5	I/O	SPI0 serial clock pin.
		PA.2	MFP4	I/O	
		PD.2	MFP4	I/O	
		PB.14	MFP4	I/O	
	SPI0_I2SMCLK	PB.0	MFP8	I/O	SPI0 I²S master clock output pin
		PF.10	MFP5	I/O	
		PA.4	MFP4	I/O	
		PD.13	MFP4	I/O	
		PD.14	MFP5	I/O	
		PC.14	MFP4	I/O	
		PB.11	MFP9	I/O	
	SPI0_MISO	PF.7	MFP5	I/O	SPI0 MISO (Master In, Slave Out) pin.
		PA.1	MFP4	I/O	
		PD.1	MFP4	I/O	
		PB.13	MFP4	I/O	
	SPI0_MOSI	PF.6	MFP5	I/O	SPI0 MOSI (Master Out, Slave In) pin.
		PA.0	MFP4	I/O	
		PD.0	MFP4	I/O	
		PB.12	MFP4	I/O	
	SPI0_SS	PF.9	MFP5	I/O	SPI0 slave select pin.
		PA.3	MFP4	I/O	
		PD.3	MFP4	I/O	
		PB.15	MFP4	I/O	
SPI1	SPI1_CLK	PB.3	MFP5	I/O	SPI1 serial clock pin.
		PH.6	MFP3	I/O	
		PA.7	MFP4	I/O	
		PC.1	MFP7	I/O	
		PD.5	MFP5	I/O	
		PH.8	MFP6	I/O	
	SPI1_I2SMCLK	PB.1	MFP5	I/O	SPI1 I²S master clock output pin
		PA.5	MFP4	I/O	
		PC.4	MFP7	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
		PD.13	MFP5	I/O	
		PH.10	MFP6	I/O	
	SPI1_MISO	PB.5	MFP5	I/O	SPI1 MISO (Master In, Slave Out) pin.
		PH.4	MFP3	I/O	
		PC.7	MFP4	I/O	
		PC.3	MFP7	I/O	
		PD.7	MFP5	I/O	
		PE.1	MFP6	I/O	
	SPI1_MOSI	PB.4	MFP5	I/O	SPI1 MOSI (Master Out, Slave In) pin.
		PH.5	MFP3	I/O	
		PC.6	MFP4	I/O	
		PC.2	MFP7	I/O	
		PD.6	MFP5	I/O	
		PE.0	MFP6	I/O	
	SPI1_SS	PB.2	MFP5	I/O	SPI1 slave select pin.
		PH.7	MFP3	I/O	
		PA.6	MFP4	I/O	
		PC.0	MFP7	I/O	
		PD.4	MFP5	I/O	
		PH.9	MFP6	I/O	
TM0	TM0	PB.5	MFP14	I/O	Timer0 event counter input/toggle output pin.
		PG.2	MFP13	I/O	
		PC.7	MFP14	I/O	
	TM0_EXT	PA.11	MFP13	I/O	Timer0 external capture input/toggle output pin.
		PB.15	MFP13	I/O	
TM1	TM1	PB.4	MFP14	I/O	Timer1 event counter input/toggle output pin.
		PG.3	MFP13	I/O	
		PC.6	MFP14	I/O	
		PC.14	MFP13	I/O	
	TM1_EXT	PA.10	MFP13	I/O	Timer1 external capture input/toggle output pin.
		PB.14	MFP13	I/O	
TM2	TM2	PB.3	MFP14	I/O	Timer2 event counter input/toggle output

Group	Pin Name	GPIO	MFP	Type	Description
		PG.4	MFP13	I/O	pin.
		PA.7	MFP14	I/O	
		PF.15	MFP13	I/O	
		PD.0	MFP14	I/O	
	TM2_EXT	PA.9	MFP13	I/O	Timer2 external capture input/toggle output pin.
		PB.13	MFP13	I/O	
TM3	TM3	PB.2	MFP14	I/O	Timer3 event counter input/toggle output pin.
		PF.11	MFP13	I/O	
		PF.14	MFP14	I/O	
		PA.6	MFP14	I/O	
		PD.15	MFP14	I/O	
	TM3_EXT	PA.8	MFP13	I/O	Timer3 external capture input/toggle output pin.
		PB.12	MFP13	I/O	
TRACE	TRACE_CLK	PE.12	MFP14	O	ETM Trace Clock output pin
		PD.15	MFP13	O	
	TRACE_DATA0	PE.11	MFP14	O	ETM Trace Data 0 output pin
		PF.13	MFP13	O	
	TRACE_DATA1	PE.10	MFP14	O	ETM Trace Data 1 output pin
		PF.12	MFP13	O	
	TRACE_DATA2	PE.9	MFP14	O	ETM Trace Data 2 output pin
		PC.6	MFP13	O	
	TRACE_DATA3	PE.8	MFP14	O	ETM Trace Data 3 output pin
		PC.7	MFP13	O	
UART0	UART0_RXD	PC.11	MFP3	I	UART0 data receiver input pin.
		PI.1	MFP3	I	
		PF.2	MFP3	I	
		PA.6	MFP7	I	
		PA.4	MFP11	I	
		PA.0	MFP7	I	
		PF.1	MFP4	I	
		PD.2	MFP9	I	
		PA.15	MFP3	I	

Group	Pin Name	GPIO	MFP	Type	Description
		PI.5	MFP8	I	
		PH.11	MFP8	I	
		PB.12	MFP6	I	
		PB.8	MFP5	I	
	UART0_TXD	PC.12	MFP3	O	UART0 data transmitter output pin.
		PI.0	MFP3	O	
		PF.3	MFP3	O	
		PA.7	MFP7	O	
		PA.5	MFP11	O	
		PA.1	MFP7	O	
		PF.0	MFP4	O	
		PD.3	MFP9	O	
		PA.14	MFP3	O	
		PI.4	MFP8	O	
		PH.10	MFP8	O	
		PB.13	MFP6	O	
		PB.9	MFP5	O	
	UART0_nCTS	PC.7	MFP7	I	UART0 clear to Send input pin.
		PA.5	MFP7	I	
		PB.15	MFP6	I	
		PB.11	MFP5	I	
	UART0_nRTS	PC.6	MFP7	O	UART0 request to Send output pin.
		PA.4	MFP7	O	
		PB.14	MFP6	O	
		PB.10	MFP5	O	
UART1	UART1_RXD	PB.2	MFP6	I	UART1 data receiver input pin.
		PA.8	MFP7	I	
		PD.10	MFP3	I	
		PC.8	MFP8	I	
		PF.13	MFP8	I	
		PA.2	MFP8	I	
		PF.1	MFP2	I	

Group	Pin Name	GPIO	MFP	Type	Description
		PI.3	MFP3	I	
		PD.6	MFP3	I	
		PI.5	MFP10	I	
		PH.9	MFP10	I	
		PB.6	MFP6	I	
	UART1_TXD	PB.3	MFP6	O	UART1 data transmitter output pin.
		PA.9	MFP7	O	
		PD.11	MFP3	O	
		PE.13	MFP8	O	
		PF.12	MFP8	O	
		PA.3	MFP8	O	
		PF.0	MFP2	O	
		PI.2	MFP3	O	
		PD.7	MFP3	O	
		PI.4	MFP10	O	
		PH.8	MFP10	O	
		PB.7	MFP6	O	
	UART1_nCTS	PE.11	MFP8	I	UART1 clear to Send input pin.
		PA.1	MFP8	I	
		PB.9	MFP6	I	
	UART1_nRTS	PE.12	MFP8	O	UART1 request to Send output pin.
		PA.0	MFP8	O	
		PB.8	MFP6	O	
UART2	UART2_RXD	PB.4	MFP12	I	UART2 data receiver input pin.
		PB.0	MFP7	I	
		PI.1	MFP7	I	
		PD.12	MFP7	I	
		PF.5	MFP2	I	
		PE.9	MFP7	I	
		PE.15	MFP3	I	
		PC.4	MFP8	I	
		PC.0	MFP8	I	

Group	Pin Name	GPIO	MFP	Type	Description
	UART2_TXD	PB.5	MFP12	O	UART2 data transmitter output pin.
		PB.1	MFP7	O	
		PI.0	MFP7	O	
		PC.13	MFP7	O	
		PF.4	MFP2	O	
		PE.8	MFP7	O	
		PE.14	MFP3	O	
		PC.5	MFP8	O	
		PC.1	MFP8	O	
	UART2_nCTS	PF.5	MFP4	I	UART2 clear to Send input pin.
		PD.9	MFP4	I	
		PC.2	MFP8	I	
	UART2_nRTS	PF.4	MFP4	O	UART2 request to Send output pin.
		PD.8	MFP4	O	
		PC.3	MFP8	O	
UART3	UART3_RXD	PC.9	MFP7	I	UART3 data receiver input pin.
		PE.11	MFP7	I	
		PF.13	MFP7	I	
		PC.2	MFP11	I	
		PD.0	MFP5	I	
		PE.0	MFP7	I	
		PB.14	MFP7	I	
	UART3_TXD	PC.10	MFP7	O	UART3 data transmitter output pin.
		PE.10	MFP7	O	
		PF.12	MFP7	O	
		PC.3	MFP11	O	
		PD.1	MFP5	O	
		PE.1	MFP7	O	
		PB.15	MFP7	O	
	UART3_nCTS	PD.2	MFP5	I	UART3 clear to Send input pin.
		PH.9	MFP7	I	
		PB.12	MFP7	I	

Group	Pin Name	GPIO	MFP	Type	Description
	UART3_nRTS	PD.3	MFP5	O	UART3 request to Send output pin.
		PH.8	MFP7	O	
		PB.13	MFP7	O	
UART4	UART4_RXD	PF.6	MFP6	I	UART4 data receiver input pin.
		PC.6	MFP5	I	
		PA.2	MFP7	I	
		PC.4	MFP11	I	
		PI.3	MFP11	I	
		PA.13	MFP3	I	
		PI.5	MFP7	I	
		PH.11	MFP7	I	
		PB.10	MFP6	I	
	UART4_TXD	PF.7	MFP6	O	UART4 data transmitter output pin.
		PC.7	MFP5	O	
		PA.3	MFP7	O	
		PC.5	MFP11	O	
		PI.2	MFP11	O	
		PA.12	MFP3	O	
		PI.4	MFP7	O	
		PH.10	MFP7	O	
		PB.11	MFP6	O	
	UART4_nCTS	PC.8	MFP5	I	UART4 clear to Send input pin.
		PE.1	MFP9	I	
	UART4_nRTS	PE.13	MFP5	O	UART4 request to Send output pin.
		PE.0	MFP9	O	
UART5	UART5_RXD	PB.4	MFP7	I	UART5 data receiver input pin.
		PI.1	MFP6	I	
		PF.10	MFP6	I	
		PF.13	MFP6	I	
		PA.4	MFP8	I	
		PI.3	MFP6	I	
		PE.6	MFP8	I	

Group	Pin Name	GPIO	MFP	Type	Description
	UART5_TXD	PB.5	MFP7	O	UART5 data transmitter output pin.
		PI.0	MFP6	O	
		PF.11	MFP6	O	
		PF.12	MFP6	O	
		PA.5	MFP8	O	
		PI.2	MFP6	O	
		PE.7	MFP8	O	
	UART5_nCTS	PB.2	MFP7	I	UART5 clear to Send input pin.
		PF.8	MFP6	I	
	UART5_nRTS	PB.3	MFP7	O	UART5 request to Send output pin.
		PF.9	MFP6	O	
X32	X32_IN	PF.5	MFP10	I	External 32.768 kHz crystal input pin.
	X32_OUT	PF.4	MFP10	O	External 32.768 kHz crystal output pin.
XT1	XT1_IN	PF.3	MFP10	I	External 4~24 MHz (high speed) crystal input pin.
	XT1_OUT	PF.2	MFP10	O	External 4~24 MHz (high speed) crystal output pin.

4.3.2 Multi-function Summary Table Sorted by GPIO

	Pin Name	Type	MFP	Description
PA.0	PA.0	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
	UART0_RXD	I	MFP7	UART0 data receiver input pin.
	UART1_nRTS	O	MFP8	UART1 request to Send output pin.
	BPWM0_CH0	I/O	MFP12	BPWM0 channel 0 output/capture input.
	EPWM0_CH5	I/O	MFP13	EPWM0 channel 5 output/capture input.
	DAC0_ST	I	MFP15	DAC0 external trigger input.
PA.1	PA.1	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
	UART0_TXD	O	MFP7	UART0 data transmitter output pin.
	UART1_nCTS	I	MFP8	UART1 clear to Send input pin.
	BPWM0_CH1	I/O	MFP12	BPWM0 channel 1 output/capture input.
	EPWM0_CH4	I/O	MFP13	EPWM0 channel 4 output/capture input.
PA.2	PA.2	I/O	MFP0	General purpose digital I/O pin.
	SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
	UART4_RXD	I	MFP7	UART4 data receiver input pin.
	UART1_RXD	I	MFP8	UART1 data receiver input pin.
	I2C1_SDA	I/O	MFP9	I^2C1 data input/output pin.
	I2C0_SMBSUS	O	MFP10	I^2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
	BPWM0_CH2	I/O	MFP12	BPWM0 channel 2 output/capture input.
	EPWM0_CH3	I/O	MFP13	EPWM0 channel 3 output/capture input.
	CIR0_RXD	I	MFP15	CIR0 data receiver input pin.
PA.3	PA.3	I/O	MFP0	General purpose digital I/O pin.
	SPI0_SS	I/O	MFP4	SPI0 slave select pin.
	UART4_TXD	O	MFP7	UART4 data transmitter output pin.
	UART1_TXD	O	MFP8	UART1 data transmitter output pin.
	I2C1_SCL	I/O	MFP9	I^2C1 clock pin.
	I2C0_SMBAL	O	MFP10	I^2C0 SMBus SMBALTER pin
	CLKO	O	MFP11	Clock Out
	BPWM0_CH3	I/O	MFP12	BPWM0 channel 3 output/capture input.
	EPWM0_CH2	I/O	MFP13	EPWM0 channel 2 output/capture input.

	Pin Name	Type	MFP	Description
	EPWM1_BRAKE1	I	MFP15	EPWM1 Brake 1 input pin.
PA.4	PA.4	I/O	MFP0	General purpose digital I/O pin.
	SPI0_I2SMCLK	I/O	MFP4	SPI0 I²S master clock output pin
	UART0_nRTS	O	MFP7	UART0 request to Send output pin.
	UART5_RXD	I	MFP8	UART5 data receiver input pin.
	I2C0_SDA	I/O	MFP9	I²C0 data input/output pin.
	UART0_RXD	I	MFP11	UART0 data receiver input pin.
	BPWM0_CH4	I/O	MFP12	BPWM0 channel 4 output/capture input.
	EPWM0_CH1	I/O	MFP13	EPWM0 channel 1 output/capture input.
PA.5	PA.5	I/O	MFP0	General purpose digital I/O pin.
	SPI1_I2SMCLK	I/O	MFP4	SPI1 I²S master clock output pin
	UART0_nCTS	I	MFP7	UART0 clear to Send input pin.
	UART5_TXD	O	MFP8	UART5 data transmitter output pin.
	I2C0_SCL	I/O	MFP9	I²C0 clock pin.
	UART0_TXD	O	MFP11	UART0 data transmitter output pin.
	BPWM0_CH5	I/O	MFP12	BPWM0 channel 5 output/capture input.
	EPWM0_CH0	I/O	MFP13	EPWM0 channel 0 output/capture input.
PA.6	PA.6	I/O	MFP0	General purpose digital I/O pin.
	SPI1_SS	I/O	MFP4	SPI1 slave select pin.
	UART0_RXD	I	MFP7	UART0 data receiver input pin.
	I2C1_SDA	I/O	MFP8	I²C1 data input/output pin.
	EPWM1_CH5	I/O	MFP11	EPWM1 channel 5 output/capture input.
	BPWM1_CH3	I/O	MFP12	BPWM1 channel 3 output/capture input.
	ACMP1_WLAT	I	MFP13	Analog comparator 1 window latch input pin
	TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
	INT0	I	MFP15	External interrupt 0 input pin.
PA.7	PA.7	I/O	MFP0	General purpose digital I/O pin.
	SPI1_CLK	I/O	MFP4	SPI1 serial clock pin.
	UART0_TXD	O	MFP7	UART0 data transmitter output pin.
	I2C1_SCL	I/O	MFP8	I²C1 clock pin.
	EPWM1_CH4	I/O	MFP11	EPWM1 channel 4 output/capture input.
	BPWM1_CH2	I/O	MFP12	BPWM1 channel 2 output/capture input.

	Pin Name	Type	MFP	Description
	ACMP0_WLAT	I	MFP13	Analog comparator 0 window latch input pin
	TM2	I/O	MFP14	Timer2 event counter input/toggle output pin.
	INT1	I	MFP15	External interrupt 1 input pin.
PA.8	PA.8	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH20	A	MFP1	EADC0 channel 20 analog input.
	UART1_RXD	I	MFP7	UART1 data receiver input pin.
	BPWM0_CH3	I/O	MFP9	BPWM0 channel 3 output/capture input.
	TM3_EXT	I/O	MFP13	Timer3 external capture input/toggle output pin.
	INT4	I	MFP15	External interrupt 4 input pin.
PA.9	PA.9	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH21	A	MFP1	EADC0 channel 21 analog input.
	UART1_TXD	O	MFP7	UART1 data transmitter output pin.
	BPWM0_CH2	I/O	MFP9	BPWM0 channel 2 output/capture input.
	TM2_EXT	I/O	MFP13	Timer2 external capture input/toggle output pin.
PA.10	PA.10	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH22	A	MFP1	EADC0 channel 22 analog input.
	ACMP1_P0	A	MFP1	Analog comparator 1 positive input 0 pin.
	BPWM0_CH1	I/O	MFP9	BPWM0 channel 1 output/capture input.
	TM1_EXT	I/O	MFP13	Timer1 external capture input/toggle output pin.
	DAC0_ST	I	MFP14	DAC0 external trigger input.
PA.11	PA.11	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH23	A	MFP1	EADC0 channel 23 analog input.
	ACMP0_P0	A	MFP1	Analog comparator 0 positive input 0 pin.
	BPWM0_CH0	I/O	MFP9	BPWM0 channel 0 output/capture input.
	EPWM0_SYNC_OUT	O	MFP10	EPWM0 counter synchronous trigger output pin.
	TM0_EXT	I/O	MFP13	Timer0 external capture input/toggle output pin.
PA.12	PA.12	I/O	MFP0	General purpose digital I/O pin.
	UART4_TXD	O	MFP3	UART4 data transmitter output pin.
	I2C1_SCL	I/O	MFP4	I^2C1 clock pin.
	BPWM1_CH2	I/O	MFP11	BPWM1 channel 2 output/capture input.
PA.13	PA.13	I/O	MFP0	General purpose digital I/O pin.
	UART4_RXD	I	MFP3	UART4 data receiver input pin.

	Pin Name	Type	MFP	Description
	I2C1_SDA	I/O	MFP4	I²C1 data input/output pin.
	BPWM1_CH3	I/O	MFP11	BPWM1 channel 3 output/capture input.
PA.14	PA.14	I/O	MFP0	General purpose digital I/O pin.
	UART0_TXD	O	MFP3	UART0 data transmitter output pin.
	BPWM1_CH4	I/O	MFP11	BPWM1 channel 4 output/capture input.
PA.15	PA.15	I/O	MFP0	General purpose digital I/O pin.
	UART0_RXD	I	MFP3	UART0 data receiver input pin.
	BPWM1_CH5	I/O	MFP11	BPWM1 channel 5 output/capture input.
	EPWM0_SYNC_IN	I	MFP12	EPWM0 counter synchronous trigger input pin.
PB.0	PB.0	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH0	A	MFP1	EADC0 channel 0 analog input.
	UART2_RXD	I	MFP7	UART2 data receiver input pin.
	SPI0_I2SMCLK	I/O	MFP8	SPI0 I²S master clock output pin
	I2C1_SDA	I/O	MFP9	I²C1 data input/output pin.
	EPWM0_CH5	I/O	MFP11	EPWM0 channel 5 output/capture input.
	EPWM1_CH5	I/O	MFP12	EPWM1 channel 5 output/capture input.
	EPWM0_BRAKE1	I	MFP13	EPWM0 Brake 1 input pin.
PB.1	PB.1	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH1	A	MFP1	EADC0 channel 1 analog input.
	SPI1_I2SMCLK	I/O	MFP5	SPI1 I²S master clock output pin
	UART2_TXD	O	MFP7	UART2 data transmitter output pin.
	I2C1_SCL	I/O	MFP9	I²C1 clock pin.
	EPWM0_CH4	I/O	MFP11	EPWM0 channel 4 output/capture input.
	EPWM1_CH4	I/O	MFP12	EPWM1 channel 4 output/capture input.
	EPWM0_BRAKE0	I	MFP13	EPWM0 Brake 0 input pin.
PB.2	PB.2	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH2	A	MFP1	EADC0 channel 2 analog input.
	ACMP0_P1	A	MFP1	Analog comparator 0 positive input 1 pin.
	SPI1_SS	I/O	MFP5	SPI1 slave select pin.
	UART1_RXD	I	MFP6	UART1 data receiver input pin.
	UART5_nCTS	I	MFP7	UART5 clear to Send input pin.
	EPWM0_CH3	I/O	MFP11	EPWM0 channel 3 output/capture input.

	Pin Name	Type	MFP	Description
	I2C1_SDA	I/O	MFP12	I^2C1 data input/output pin.
	TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
	INT3	I	MFP15	External interrupt 3 input pin.
PB.3	PB.3	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH3	A	MFP1	EADC0 channel 3 analog input.
	ACMP0_N	A	MFP1	Analog comparator 0 negative input pin.
	SPI1_CLK	I/O	MFP5	SPI1 serial clock pin.
	UART1_TXD	O	MFP6	UART1 data transmitter output pin.
	UART5_nRTS	O	MFP7	UART5 request to Send output pin.
	EPWM0_CH2	I/O	MFP11	EPWM0 channel 2 output/capture input.
	I2C1_SCL	I/O	MFP12	I^2C1 clock pin.
	EPWM0_BRAKE0	I	MFP13	EPWM0 Brake 0 input pin.
	TM2	I/O	MFP14	Timer2 event counter input/toggle output pin.
	INT2	I	MFP15	External interrupt 2 input pin.
PB.4	PB.4	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH4	A	MFP1	EADC0 channel 4 analog input.
	ACMP1_P1	A	MFP1	Analog comparator 1 positive input 1 pin.
	SPI1_MOSI	I/O	MFP5	SPI1 MOSI (Master Out, Slave In) pin.
	I2C0_SDA	I/O	MFP6	I^2C0 data input/output pin.
	UART5_RXD	I	MFP7	UART5 data receiver input pin.
	EPWM0_CH1	I/O	MFP11	EPWM0 channel 1 output/capture input.
	UART2_RXD	I	MFP12	UART2 data receiver input pin.
	TM1	I/O	MFP14	Timer1 event counter input/toggle output pin.
	INT1	I	MFP15	External interrupt 1 input pin.
PB.5	PB.5	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH5	A	MFP1	EADC0 channel 5 analog input.
	ACMP1_N	A	MFP1	Analog comparator 1 negative input pin.
	SPI1_MISO	I/O	MFP5	SPI1 MISO (Master In, Slave Out) pin.
	I2C0_SCL	I/O	MFP6	I^2C0 clock pin.
	UART5_TXD	O	MFP7	UART5 data transmitter output pin.
	EPWM0_CH0	I/O	MFP11	EPWM0 channel 0 output/capture input.
	UART2_TXD	O	MFP12	UART2 data transmitter output pin.

	Pin Name	Type	MFP	Description
	TM0	I/O	MFP14	Timer0 event counter input/toggle output pin.
	INT0	I	MFP15	External interrupt 0 input pin.
PB.6	PB.6	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH6	A	MFP1	EADC0 channel 6 analog input.
	UART1_RXD	I	MFP6	UART1 data receiver input pin.
	BPWM1_CH5	I/O	MFP10	BPWM1 channel 5 output/capture input.
	EPWM1_BRAKE1	I	MFP11	EPWM1 Brake 1 input pin.
	EPWM1_CH5	I/O	MFP12	EPWM1 channel 5 output/capture input.
	INT4	I	MFP13	External interrupt 4 input pin.
	ACMP1_O	O	MFP15	Analog comparator 1 output pin.
PB.7	PB.7	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH7	A	MFP1	EADC0 channel 7 analog input.
	UART1_TXD	O	MFP6	UART1 data transmitter output pin.
	BPWM1_CH4	I/O	MFP10	BPWM1 channel 4 output/capture input.
	EPWM1_BRAKE0	I	MFP11	EPWM1 Brake 0 input pin.
	EPWM1_CH4	I/O	MFP12	EPWM1 channel 4 output/capture input.
	INT5	I	MFP13	External interrupt 5 input pin.
	ACMP0_O	O	MFP15	Analog comparator 0 output pin.
PB.8	PB.8	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH8	A	MFP1	EADC0 channel 8 analog input.
	UART0_RXD	I	MFP5	UART0 data receiver input pin.
	UART1_nRTS	O	MFP6	UART1 request to Send output pin.
	I2C1_SMBSUS	O	MFP7	I^2C1 SMBus SMBSUS pin (PMBus CONTROL pin)
	I2C0_SDA	I/O	MFP9	I^2C0 data input/output pin.
	BPWM1_CH3	I/O	MFP10	BPWM1 channel 3 output/capture input.
	INT6	I	MFP13	External interrupt 6 input pin.
PB.9	PB.9	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH9	A	MFP1	EADC0 channel 9 analog input.
	UART0_TXD	O	MFP5	UART0 data transmitter output pin.
	UART1_nCTS	I	MFP6	UART1 clear to Send input pin.
	I2C1_SMBAL	O	MFP7	I^2C1 SMBus SMBALTER pin
	I2C0_SCL	I/O	MFP9	I^2C0 clock pin.

	Pin Name	Type	MFP	Description
	BPWM1_CH2	I/O	MFP10	BPWM1 channel 2 output/capture input.
	INT7	I	MFP13	External interrupt 7 input pin.
PB.10	PB.10	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH10	A	MFP1	EADC0 channel 10 analog input.
	UART0_nRTS	O	MFP5	UART0 request to Send output pin.
	UART4_RXD	I	MFP6	UART4 data receiver input pin.
	I2C1_SDA	I/O	MFP7	I^2C1 data input/output pin.
	BPWM1_CH1	I/O	MFP10	BPWM1 channel 1 output/capture input.
PB.11	PB.11	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH11	A	MFP1	EADC0 channel 11 analog input.
	UART0_nCTS	I	MFP5	UART0 clear to Send input pin.
	UART4_TXD	O	MFP6	UART4 data transmitter output pin.
	I2C1_SCL	I/O	MFP7	I^2C1 clock pin.
	SPI0_I2SMCLK	I/O	MFP9	SPI0 I^2S master clock output pin
	BPWM1_CH0	I/O	MFP10	BPWM1 channel 0 output/capture input.
PB.12	PB.12	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH12	A	MFP1	EADC0 channel 12 analog input.
	DAC0_OUT	A	MFP1	DAC0 channel analog output.
	ACMP0_P2	A	MFP1	Analog comparator 0 positive input 2 pin.
	ACMP1_P2	A	MFP1	Analog comparator 1 positive input 2 pin.
	SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
	UART0_RXD	I	MFP6	UART0 data receiver input pin.
	UART3_nCTS	I	MFP7	UART3 clear to Send input pin.
	EPWM1_CH3	I/O	MFP11	EPWM1 channel 3 output/capture input.
	TM3_EXT	I/O	MFP13	Timer3 external capture input/toggle output pin.
PB.13	PB.13	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH13	A	MFP1	EADC0 channel 13 analog input.
	ACMP0_P3	A	MFP1	Analog comparator 0 positive input 3 pin.
	ACMP1_P3	A	MFP1	Analog comparator 1 positive input 3 pin.
	SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
	UART0_TXD	O	MFP6	UART0 data transmitter output pin.
	UART3_nRTS	O	MFP7	UART3 request to Send output pin.

	Pin Name	Type	MFP	Description
	EPWM1_CH2	I/O	MFP11	EPWM1 channel 2 output/capture input.
	TM2_EXT	I/O	MFP13	Timer2 external capture input/toggle output pin.
PB.14	PB.14	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH14	A	MFP1	EADC0 channel 14 analog input.
	SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
	UART0_nRTS	O	MFP6	UART0 request to Send output pin.
	UART3_RXD	I	MFP7	UART3 data receiver input pin.
	EPWM1_CH1	I/O	MFP11	EPWM1 channel 1 output/capture input.
	TM1_EXT	I/O	MFP13	Timer1 external capture input/toggle output pin.
	CLKO	O	MFP14	Clock Out
PB.15	PB.15	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH15	A	MFP1	EADC0 channel 15 analog input.
	SPI0_SS	I/O	MFP4	SPI0 slave select pin.
	UART0_nCTS	I	MFP6	UART0 clear to Send input pin.
	UART3_TXD	O	MFP7	UART3 data transmitter output pin.
	EPWM0_BRAKE1	I	MFP10	EPWM0 Brake 1 input pin.
	EPWM1_CH0	I/O	MFP11	EPWM1 channel 0 output/capture input.
	TM0_EXT	I/O	MFP13	Timer0 external capture input/toggle output pin.
PC.0	PC.0	I/O	MFP0	General purpose digital I/O pin.
	SPI1_SS	I/O	MFP7	SPI1 slave select pin.
	UART2_RXD	I	MFP8	UART2 data receiver input pin.
	I2C0_SDA	I/O	MFP9	I^2C0 data input/output pin.
	EPWM1_CH5	I/O	MFP12	EPWM1 channel 5 output/capture input.
	ACMP1_O	O	MFP14	Analog comparator 1 output pin.
PC.1	PC.1	I/O	MFP0	General purpose digital I/O pin.
	SPI1_CLK	I/O	MFP7	SPI1 serial clock pin.
	UART2_TXD	O	MFP8	UART2 data transmitter output pin.
	I2C0_SCL	I/O	MFP9	I^2C0 clock pin.
	EPWM1_CH4	I/O	MFP12	EPWM1 channel 4 output/capture input.
	ACMP0_O	O	MFP14	Analog comparator 0 output pin.
	EADC0_ST	I	MFP15	EADC0 external trigger input.
PC.2	PC.2	I/O	MFP0	General purpose digital I/O pin.

	Pin Name	Type	MFP	Description
	SPI1_MOSI	I/O	MFP7	SPI1 MOSI (Master Out, Slave In) pin.
	UART2_nCTS	I	MFP8	UART2 clear to Send input pin.
	I2C0_SMBSUS	O	MFP9	I²C0 SMBus SMBSUS pin (PMBus CONTROL pin)
	UART3_RXD	I	MFP11	UART3 data receiver input pin.
	EPWM1_CH3	I/O	MFP12	EPWM1 channel 3 output/capture input.
PC.3	PC.3	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MISO	I/O	MFP7	SPI1 MISO (Master In, Slave Out) pin.
	UART2_nRTS	O	MFP8	UART2 request to Send output pin.
	I2C0_SMBAL	O	MFP9	I²C0 SMBus SMBALTER pin
	UART3_TXD	O	MFP11	UART3 data transmitter output pin.
	EPWM1_CH2	I/O	MFP12	EPWM1 channel 2 output/capture input.
PC.4	PC.4	I/O	MFP0	General purpose digital I/O pin.
	SPI1_I2SMCLK	I/O	MFP7	SPI1 I²S master clock output pin
	UART2_RXD	I	MFP8	UART2 data receiver input pin.
	I2C1_SDA	I/O	MFP9	I²C1 data input/output pin.
	UART4_RXD	I	MFP11	UART4 data receiver input pin.
	EPWM1_CH1	I/O	MFP12	EPWM1 channel 1 output/capture input.
PC.5	PC.5	I/O	MFP0	General purpose digital I/O pin.
	UART2_TXD	O	MFP8	UART2 data transmitter output pin.
	I2C1_SCL	I/O	MFP9	I²C1 clock pin.
	UART4_TXD	O	MFP11	UART4 data transmitter output pin.
	EPWM1_CH0	I/O	MFP12	EPWM1 channel 0 output/capture input.
PC.6	PC.6	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MOSI	I/O	MFP4	SPI1 MOSI (Master Out, Slave In) pin.
	UART4_RXD	I	MFP5	UART4 data receiver input pin.
	UART0_nRTS	O	MFP7	UART0 request to Send output pin.
	I2C1_SMBSUS	O	MFP8	I²C1 SMBus SMBSUS pin (PMBus CONTROL pin)
	EPWM1_CH3	I/O	MFP11	EPWM1 channel 3 output/capture input.
	BPWM1_CH1	I/O	MFP12	BPWM1 channel 1 output/capture input.
	TRACE_DATA2	O	MFP13	ETM Trace Data 2 output pin
	TM1	I/O	MFP14	Timer1 event counter input/toggle output pin.
	INT2	I	MFP15	External interrupt 2 input pin.

	Pin Name	Type	MFP	Description
PC.7	PC.7	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MISO	I/O	MFP4	SPI1 MISO (Master In, Slave Out) pin.
	UART4_TXD	O	MFP5	UART4 data transmitter output pin.
	UART0_nCTS	I	MFP7	UART0 clear to Send input pin.
	I2C1_SMBAL	O	MFP8	I^2C1 SMBus SMBALTER pin
	EPWM1_CH2	I/O	MFP11	EPWM1 channel 2 output/capture input.
	BPWM1_CH0	I/O	MFP12	BPWM1 channel 0 output/capture input.
	TRACE_DATA3	O	MFP13	ETM Trace Data 3 output pin
	TM0	I/O	MFP14	Timer0 event counter input/toggle output pin.
	INT3	I	MFP15	External interrupt 3 input pin.
PC.8	PC.8	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SDA	I/O	MFP4	I^2C0 data input/output pin.
	UART4_nCTS	I	MFP5	UART4 clear to Send input pin.
	UART1_RXD	I	MFP8	UART1 data receiver input pin.
	EPWM1_CH1	I/O	MFP11	EPWM1 channel 1 output/capture input.
	BPWM1_CH4	I/O	MFP12	BPWM1 channel 4 output/capture input.
PC.9	PC.9	I/O	MFP0	General purpose digital I/O pin.
	UART3_RXD	I	MFP7	UART3 data receiver input pin.
	EPWM1_CH3	I/O	MFP12	EPWM1 channel 3 output/capture input.
PC.10	PC.10	I/O	MFP0	General purpose digital I/O pin.
	UART3_TXD	O	MFP7	UART3 data transmitter output pin.
	EPWM1_CH2	I/O	MFP12	EPWM1 channel 2 output/capture input.
PC.11	PC.11	I/O	MFP0	General purpose digital I/O pin.
	UART0_RXD	I	MFP3	UART0 data receiver input pin.
	I2C0_SDA	I/O	MFP4	I^2C0 data input/output pin.
	EPWM1_CH1	I/O	MFP12	EPWM1 channel 1 output/capture input.
	ACMP1_O	O	MFP14	Analog comparator 1 output pin.
PC.12	PC.12	I/O	MFP0	General purpose digital I/O pin.
	UART0_TXD	O	MFP3	UART0 data transmitter output pin.
	I2C0_SCL	I/O	MFP4	I^2C0 clock pin.
	EPWM1_CH0	I/O	MFP12	EPWM1 channel 0 output/capture input.
	ACMP0_O	O	MFP14	Analog comparator 0 output pin.

	Pin Name	Type	MFP	Description
PC.13	PC.13	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH19	A	MFP1	EADC0 channel 19 analog input.
	UART2_TXD	O	MFP7	UART2 data transmitter output pin.
	BPWM0_CH4	I/O	MFP9	BPWM0 channel 4 output/capture input.
	CLKO	O	MFP13	Clock Out
	EADC0_ST	I	MFP14	EADC0 external trigger input.
PC.14	PC.14	I/O	MFP0	General purpose digital I/O pin.
	SPI0_I2SMCLK	I/O	MFP4	SPI0 I^2S master clock output pin
	CIR0_RXD	I	MFP10	CIR0 data receiver input pin.
	EPWM0_SYNC_IN	I	MFP11	EPWM0 counter synchronous trigger input pin.
	TM1	I/O	MFP13	Timer1 event counter input/toggle output pin.
PD.0	PD.0	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
	UART3_RXD	I	MFP5	UART3 data receiver input pin.
	TM2	I/O	MFP14	Timer2 event counter input/toggle output pin.
PD.1	PD.1	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
	UART3_TXD	O	MFP5	UART3 data transmitter output pin.
PD.2	PD.2	I/O	MFP0	General purpose digital I/O pin.
	SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
	UART3_nCTS	I	MFP5	UART3 clear to Send input pin.
	UART0_RXD	I	MFP9	UART0 data receiver input pin.
PD.3	PD.3	I/O	MFP0	General purpose digital I/O pin.
	SPI0_SS	I/O	MFP4	SPI0 slave select pin.
	UART3_nRTS	O	MFP5	UART3 request to Send output pin.
	UART0_TXD	O	MFP9	UART0 data transmitter output pin.
PD.4	PD.4	I/O	MFP0	General purpose digital I/O pin.
	I2C1_SDA	I/O	MFP4	I^2C1 data input/output pin.
	SPI1_SS	I/O	MFP5	SPI1 slave select pin.
PD.5	PD.5	I/O	MFP0	General purpose digital I/O pin.
	I2C1_SCL	I/O	MFP4	I^2C1 clock pin.
	SPI1_CLK	I/O	MFP5	SPI1 serial clock pin.

	Pin Name	Type	MFP	Description
PD.6	PD.6	I/O	MFP0	General purpose digital I/O pin.
	UART1_RXD	I	MFP3	UART1 data receiver input pin.
	I2C0_SDA	I/O	MFP4	I^2C0 data input/output pin.
	SPI1_MOSI	I/O	MFP5	SPI1 MOSI (Master Out, Slave In) pin.
PD.7	PD.7	I/O	MFP0	General purpose digital I/O pin.
	UART1_TXD	O	MFP3	UART1 data transmitter output pin.
	I2C0_SCL	I/O	MFP4	I^2C0 clock pin.
	SPI1_MISO	I/O	MFP5	SPI1 MISO (Master In, Slave Out) pin.
PD.8	PD.8	I/O	MFP0	General purpose digital I/O pin.
	UART2_nRTS	O	MFP4	UART2 request to Send output pin.
PD.9	PD.9	I/O	MFP0	General purpose digital I/O pin.
	UART2_nCTS	I	MFP4	UART2 clear to Send input pin.
PD.10	PD.10	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH16	A	MFP1	EADC0 channel 16 analog input.
	UART1_RXD	I	MFP3	UART1 data receiver input pin.
	INT7	I	MFP15	External interrupt 7 input pin.
PD.11	PD.11	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH17	A	MFP1	EADC0 channel 17 analog input.
	UART1_TXD	O	MFP3	UART1 data transmitter output pin.
	INT6	I	MFP15	External interrupt 6 input pin.
PD.12	PD.12	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH18	A	MFP1	EADC0 channel 18 analog input.
	UART2_RXD	I	MFP7	UART2 data receiver input pin.
	BPWM0_CH5	I/O	MFP9	BPWM0 channel 5 output/capture input.
	CLKO	O	MFP13	Clock Out
	EADC0_ST	I	MFP14	EADC0 external trigger input.
	INT5	I	MFP15	External interrupt 5 input pin.
PD.13	PD.13	I/O	MFP0	General purpose digital I/O pin.
	SPI0_I2SMCLK	I/O	MFP4	SPI0 I^2S master clock output pin
	SPI1_I2SMCLK	I/O	MFP5	SPI1 I^2S master clock output pin
PD.14	PD.14	I/O	MFP0	General purpose digital I/O pin.
	SPI0_I2SMCLK	I/O	MFP5	SPI0 I^2S master clock output pin

	Pin Name	Type	MFP	Description
	EPWM0_CH4	I/O	MFP11	EPWM0 channel 4 output/capture input.
PD.15	PD.15	I/O	MFP0	General purpose digital I/O pin.
	EPWM0_CH5	I/O	MFP12	EPWM0 channel 5 output/capture input.
	TRACE_CLK	O	MFP13	ETM Trace Clock output pin
	TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
	INT1	I	MFP15	External interrupt 1 input pin.
PE.0	PE.0	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MOSI	I/O	MFP6	SPI1 MOSI (Master Out, Slave In) pin.
	UART3_RXD	I	MFP7	UART3 data receiver input pin.
	I2C1_SDA	I/O	MFP8	I^2C1 data input/output pin.
	UART4_nRTS	O	MFP9	UART4 request to Send output pin.
PE.1	PE.1	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MISO	I/O	MFP6	SPI1 MISO (Master In, Slave Out) pin.
	UART3_TXD	O	MFP7	UART3 data transmitter output pin.
	I2C1_SCL	I/O	MFP8	I^2C1 clock pin.
	UART4_nCTS	I	MFP9	UART4 clear to Send input pin.
PE.2	PE.2	I/O	MFP0	General purpose digital I/O pin.
	EPWM0_CH5	I/O	MFP12	EPWM0 channel 5 output/capture input.
	BPWM0_CH0	I/O	MFP13	BPWM0 channel 0 output/capture input.
PE.3	PE.3	I/O	MFP0	General purpose digital I/O pin.
	EPWM0_CH4	I/O	MFP12	EPWM0 channel 4 output/capture input.
	BPWM0_CH1	I/O	MFP13	BPWM0 channel 1 output/capture input.
PE.4	PE.4	I/O	MFP0	General purpose digital I/O pin.
	EPWM0_CH3	I/O	MFP12	EPWM0 channel 3 output/capture input.
	BPWM0_CH2	I/O	MFP13	BPWM0 channel 2 output/capture input.
PE.5	PE.5	I/O	MFP0	General purpose digital I/O pin.
	EPWM0_CH2	I/O	MFP12	EPWM0 channel 2 output/capture input.
	BPWM0_CH3	I/O	MFP13	BPWM0 channel 3 output/capture input.
PE.6	PE.6	I/O	MFP0	General purpose digital I/O pin.
	UART5_RXD	I	MFP8	UART5 data receiver input pin.
	EPWM0_CH1	I/O	MFP12	EPWM0 channel 1 output/capture input.
	BPWM0_CH4	I/O	MFP13	BPWM0 channel 4 output/capture input.

	Pin Name	Type	MFP	Description
PE.7	PE.7	I/O	MFP0	General purpose digital I/O pin.
	UART5_TXD	O	MFP8	UART5 data transmitter output pin.
	EPWM0_CH0	I/O	MFP12	EPWM0 channel 0 output/capture input.
	BPWM0_CH5	I/O	MFP13	BPWM0 channel 5 output/capture input.
PE.8	PE.8	I/O	MFP0	General purpose digital I/O pin.
	UART2_TXD	O	MFP7	UART2 data transmitter output pin.
	EPWM0_CH0	I/O	MFP10	EPWM0 channel 0 output/capture input.
	EPWM0_BRAKE0	I	MFP11	EPWM0 Brake 0 input pin.
	TRACE_DATA3	O	MFP14	ETM Trace Data 3 output pin
PE.9	PE.9	I/O	MFP0	General purpose digital I/O pin.
	UART2_RXD	I	MFP7	UART2 data receiver input pin.
	EPWM0_CH1	I/O	MFP10	EPWM0 channel 1 output/capture input.
	EPWM0_BRAKE1	I	MFP11	EPWM0 Brake 1 input pin.
	TRACE_DATA2	O	MFP14	ETM Trace Data 2 output pin
PE.10	PE.10	I/O	MFP0	General purpose digital I/O pin.
	UART3_TXD	O	MFP7	UART3 data transmitter output pin.
	EPWM0_CH2	I/O	MFP10	EPWM0 channel 2 output/capture input.
	EPWM1_BRAKE0	I	MFP11	EPWM1 Brake 0 input pin.
	TRACE_DATA1	O	MFP14	ETM Trace Data 1 output pin
PE.11	PE.11	I/O	MFP0	General purpose digital I/O pin.
	UART3_RXD	I	MFP7	UART3 data receiver input pin.
	UART1_nCTS	I	MFP8	UART1 clear to Send input pin.
	EPWM0_CH3	I/O	MFP10	EPWM0 channel 3 output/capture input.
	EPWM1_BRAKE1	I	MFP11	EPWM1 Brake 1 input pin.
	TRACE_DATA0	O	MFP14	ETM Trace Data 0 output pin
PE.12	PE.12	I/O	MFP0	General purpose digital I/O pin.
	UART1_nRTS	O	MFP8	UART1 request to Send output pin.
	EPWM0_CH4	I/O	MFP10	EPWM0 channel 4 output/capture input.
	TRACE_CLK	O	MFP14	ETM Trace Clock output pin
PE.13	PE.13	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SCL	I/O	MFP4	I^2C0 clock pin.
	UART4_nRTS	O	MFP5	UART4 request to Send output pin.

	Pin Name	Type	MFP	Description
	UART1_TXD	O	MFP8	UART1 data transmitter output pin.
	EPWM0_CH5	I/O	MFP10	EPWM0 channel 5 output/capture input.
	EPWM1_CH0	I/O	MFP11	EPWM1 channel 0 output/capture input.
	BPWM1_CH5	I/O	MFP12	BPWM1 channel 5 output/capture input.
PE.14	PE.14	I/O	MFP0	General purpose digital I/O pin.
	UART2_TXD	O	MFP3	UART2 data transmitter output pin.
PE.15	PE.15	I/O	MFP0	General purpose digital I/O pin.
	UART2_RXD	I	MFP3	UART2 data receiver input pin.
PF.0	PF.0	I/O	MFP0	General purpose digital I/O pin.
	UART1_TXD	O	MFP2	UART1 data transmitter output pin.
	I2C1_SCL	I/O	MFP3	I^2C1 clock pin.
	UART0_TXD	O	MFP4	UART0 data transmitter output pin.
	BPWM1_CH0	I/O	MFP12	BPWM1 channel 0 output/capture input.
	ICE_DAT	I/O	MFP14	Serial wired debugger data pin. Note: It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
PF.1	PF.1	I/O	MFP0	General purpose digital I/O pin.
	UART1_RXD	I	MFP2	UART1 data receiver input pin.
	I2C1_SDA	I/O	MFP3	I^2C1 data input/output pin.
	UART0_RXD	I	MFP4	UART0 data receiver input pin.
	BPWM1_CH1	I/O	MFP12	BPWM1 channel 1 output/capture input.
	ICE_CLK	I	MFP14	Serial wired debugger clock pin. Note: It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
PF.2	PF.2	I/O	MFP0	General purpose digital I/O pin.
	UART0_RXD	I	MFP3	UART0 data receiver input pin.
	I2C0_SDA	I/O	MFP4	I^2C0 data input/output pin.
	XT1_OUT	O	MFP10	External 4~24 MHz (high speed) crystal output pin.
	BPWM1_CH1	I/O	MFP11	BPWM1 channel 1 output/capture input.
PF.3	PF.3	I/O	MFP0	General purpose digital I/O pin.
	UART0_TXD	O	MFP3	UART0 data transmitter output pin.
	I2C0_SCL	I/O	MFP4	I^2C0 clock pin.
	XT1_IN	I	MFP10	External 4~24 MHz (high speed) crystal input pin.

	Pin Name	Type	MFP	Description
	BPWM1_CH0	I/O	MFP11	BPWM1 channel 0 output/capture input.
PF.4	PF.4	I/O	MFP0	General purpose digital I/O pin.
	UART2_TXD	O	MFP2	UART2 data transmitter output pin.
	UART2_nRTS	O	MFP4	UART2 request to Send output pin.
	EPWM0_CH1	I/O	MFP7	EPWM0 channel 1 output/capture input.
	BPWM0_CH5	I/O	MFP8	BPWM0 channel 5 output/capture input.
	X32_OUT	O	MFP10	External 32.768 kHz crystal output pin.
PF.5	PF.5	I/O	MFP0	General purpose digital I/O pin.
	UART2_RXD	I	MFP2	UART2 data receiver input pin.
	UART2_nCTS	I	MFP4	UART2 clear to Send input pin.
	EPWM0_CH0	I/O	MFP7	EPWM0 channel 0 output/capture input.
	BPWM0_CH4	I/O	MFP8	BPWM0 channel 4 output/capture input.
	EPWM0_SYNC_OUT	O	MFP9	EPWM0 counter synchronous trigger output pin.
	X32_IN	I	MFP10	External 32.768 kHz crystal input pin.
	EADC0_ST	I	MFP11	EADC0 external trigger input.
PF.6	PF.6	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MOSI	I/O	MFP5	SPI0 MOSI (Master Out, Slave In) pin.
	UART4_RXD	I	MFP6	UART4 data receiver input pin.
PF.7	PF.7	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MISO	I/O	MFP5	SPI0 MISO (Master In, Slave Out) pin.
	UART4_TXD	O	MFP6	UART4 data transmitter output pin.
PF.8	PF.8	I/O	MFP0	General purpose digital I/O pin.
	SPI0_CLK	I/O	MFP5	SPI0 serial clock pin.
	UART5_nCTS	I	MFP6	UART5 clear to Send input pin.
PF.9	PF.9	I/O	MFP0	General purpose digital I/O pin.
	SPI0_SS	I/O	MFP5	SPI0 slave select pin.
	UART5_nRTS	O	MFP6	UART5 request to Send output pin.
PF.10	PF.10	I/O	MFP0	General purpose digital I/O pin.
	SPI0_I2SMCLK	I/O	MFP5	SPI0 I^2S master clock output pin
	UART5_RXD	I	MFP6	UART5 data receiver input pin.
PF.11	PF.11	I/O	MFP0	General purpose digital I/O pin.
	UART5_TXD	O	MFP6	UART5 data transmitter output pin.

	Pin Name	Type	MFP	Description
	TM3	I/O	MFP13	Timer3 event counter input/toggle output pin.
PF.12	PF.12	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SCL	I/O	MFP4	I^2C0 clock pin.
	UART5_TXD	O	MFP6	UART5 data transmitter output pin.
	UART3_TXD	O	MFP7	UART3 data transmitter output pin.
	UART1_TXD	O	MFP8	UART1 data transmitter output pin.
	I2C1_SCL	I/O	MFP9	I^2C1 clock pin.
	EPWM0_CH2	I/O	MFP10	EPWM0 channel 2 output/capture input.
	BPWM0_CH0	I/O	MFP11	BPWM0 channel 0 output/capture input.
	TRACE_DATA1	O	MFP13	ETM Trace Data 1 output pin
	CIR0_RXD	I	MFP15	CIR0 data receiver input pin.
PF.13	PF.13	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SDA	I/O	MFP4	I^2C0 data input/output pin.
	UART5_RXD	I	MFP6	UART5 data receiver input pin.
	UART3_RXD	I	MFP7	UART3 data receiver input pin.
	UART1_RXD	I	MFP8	UART1 data receiver input pin.
	I2C1_SDA	I/O	MFP9	I^2C1 data input/output pin.
	EPWM0_CH3	I/O	MFP10	EPWM0 channel 3 output/capture input.
	BPWM0_CH1	I/O	MFP11	BPWM0 channel 1 output/capture input.
	TRACE_DATA0	O	MFP13	ETM Trace Data 0 output pin
PF.14	PF.14	I/O	MFP0	General purpose digital I/O pin.
	EPWM1_BRAKE0	I	MFP9	EPWM1 Brake 0 input pin.
	EPWM0_BRAKE0	I	MFP10	EPWM0 Brake 0 input pin.
	EPWM0_CH4	I/O	MFP12	EPWM0 channel 4 output/capture input.
	CLKO	O	MFP13	Clock Out
	TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
	INT5	I	MFP15	External interrupt 5 input pin.
PF.15	PF.15	I/O	MFP0	General purpose digital I/O pin.
	EPWM0_BRAKE0	I	MFP11	EPWM0 Brake 0 input pin.
	EPWM0_CH1	I/O	MFP12	EPWM0 channel 1 output/capture input.
	TM2	I/O	MFP13	Timer2 event counter input/toggle output pin.
	CLKO	O	MFP14	Clock Out

	Pin Name	Type	MFP	Description
	INT4	I	MFP15	External interrupt 4 input pin.
PG.2	PG.2	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SMBAL	O	MFP4	I^2C0 SMBus SMBALTER pin
	I2C1_SCL	I/O	MFP5	I^2C1 clock pin.
	TM0	I/O	MFP13	Timer0 event counter input/toggle output pin.
PG.3	PG.3	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SMBSUS	O	MFP4	I^2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
	I2C1_SDA	I/O	MFP5	I^2C1 data input/output pin.
	TM1	I/O	MFP13	Timer1 event counter input/toggle output pin.
PG.4	PG.4	I/O	MFP0	General purpose digital I/O pin.
	TM2	I/O	MFP13	Timer2 event counter input/toggle output pin.
PG.9	PG.9	I/O	MFP0	General purpose digital I/O pin.
	BPWM0_CH5	I/O	MFP12	BPWM0 channel 5 output/capture input.
PG.10	PG.10	I/O	MFP0	General purpose digital I/O pin.
	BPWM0_CH4	I/O	MFP12	BPWM0 channel 4 output/capture input.
PG.11	PG.11	I/O	MFP0	General purpose digital I/O pin.
	BPWM0_CH3	I/O	MFP12	BPWM0 channel 3 output/capture input.
PG.12	PG.12	I/O	MFP0	General purpose digital I/O pin.
	BPWM0_CH2	I/O	MFP12	BPWM0 channel 2 output/capture input.
PG.13	PG.13	I/O	MFP0	General purpose digital I/O pin.
	BPWM0_CH1	I/O	MFP12	BPWM0 channel 1 output/capture input.
PG.14	PG.14	I/O	MFP0	General purpose digital I/O pin.
	BPWM0_CH0	I/O	MFP12	BPWM0 channel 0 output/capture input.
PG.15	PG.15	I/O	MFP0	General purpose digital I/O pin.
	CLKO	O	MFP14	Clock Out
	EADC0_ST	I	MFP15	EADC0 external trigger input.
PH.4	PH.4	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MISO	I/O	MFP3	SPI1 MISO (Master In, Slave Out) pin.
PH.5	PH.5	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MOSI	I/O	MFP3	SPI1 MOSI (Master Out, Slave In) pin.
PH.6	PH.6	I/O	MFP0	General purpose digital I/O pin.
	SPI1_CLK	I/O	MFP3	SPI1 serial clock pin.

	Pin Name	Type	MFP	Description
PH.7	PH.7	I/O	MFP0	General purpose digital I/O pin.
	SPI1_SS	I/O	MFP3	SPI1 slave select pin.
PH.8	PH.8	I/O	MFP0	General purpose digital I/O pin.
	SPI1_CLK	I/O	MFP6	SPI1 serial clock pin.
	UART3_nRTS	O	MFP7	UART3 request to Send output pin.
	I2C1_SMBAL	O	MFP8	I^2C1 SMBus SMBALTER pin
	UART1_TXD	O	MFP10	UART1 data transmitter output pin.
PH.9	PH.9	I/O	MFP0	General purpose digital I/O pin.
	SPI1_SS	I/O	MFP6	SPI1 slave select pin.
	UART3_nCTS	I	MFP7	UART3 clear to Send input pin.
	I2C1_SMBSUS	O	MFP8	I^2C1 SMBus SMBSUS pin (PMBus CONTROL pin)
	UART1_RXD	I	MFP10	UART1 data receiver input pin.
PH.10	PH.10	I/O	MFP0	General purpose digital I/O pin.
	SPI1_I2SMCLK	I/O	MFP6	SPI1 I^2S master clock output pin
	UART4_TXD	O	MFP7	UART4 data transmitter output pin.
	UART0_TXD	O	MFP8	UART0 data transmitter output pin.
PH.11	PH.11	I/O	MFP0	General purpose digital I/O pin.
	UART4_RXD	I	MFP7	UART4 data receiver input pin.
	UART0_RXD	I	MFP8	UART0 data receiver input pin.
	EPWM0_CH5	I/O	MFP11	EPWM0 channel 5 output/capture input.
PI.0	PI.0	I/O	MFP0	General purpose digital I/O pin.
	UART0_TXD	O	MFP3	UART0 data transmitter output pin.
	I2C0_SCL	I/O	MFP4	I^2C0 clock pin.
	UART5_TXD	O	MFP6	UART5 data transmitter output pin.
	UART2_TXD	O	MFP7	UART2 data transmitter output pin.
	I2C1_SCL	I/O	MFP9	I^2C1 clock pin.
	EPWM0_CH4	I/O	MFP11	EPWM0 channel 4 output/capture input.
	EPWM1_CH0	I/O	MFP12	EPWM1 channel 0 output/capture input.
	ACMP0_O	O	MFP14	Analog comparator 0 output pin.
PI.1	PI.1	I/O	MFP0	General purpose digital I/O pin.
	UART0_RXD	I	MFP3	UART0 data receiver input pin.
	I2C0_SDA	I/O	MFP4	I^2C0 data input/output pin.

	Pin Name	Type	MFP	Description
	UART5_RXD	I	MFP6	UART5 data receiver input pin.
	UART2_RXD	I	MFP7	UART2 data receiver input pin.
	I2C1_SDA	I/O	MFP9	I^2C1 data input/output pin.
	EPWM0_CH5	I/O	MFP11	EPWM0 channel 5 output/capture input.
	EPWM1_CH1	I/O	MFP12	EPWM1 channel 1 output/capture input.
	ACMP1_O	O	MFP14	Analog comparator 1 output pin.
PI.2	PI.2	I/O	MFP0	General purpose digital I/O pin.
	UART1_TXD	O	MFP3	UART1 data transmitter output pin.
	I2C0_SCL	I/O	MFP4	I^2C0 clock pin.
	UART5_TXD	O	MFP6	UART5 data transmitter output pin.
	I2C1_SCL	I/O	MFP9	I^2C1 clock pin.
	UART4_TXD	O	MFP11	UART4 data transmitter output pin.
	BPWM0_CH5	I/O	MFP12	BPWM0 channel 5 output/capture input.
	EADC0_ST	I	MFP15	EADC0 external trigger input.
PI.3	PI.3	I/O	MFP0	General purpose digital I/O pin.
	UART1_RXD	I	MFP3	UART1 data receiver input pin.
	I2C0_SDA	I/O	MFP4	I^2C0 data input/output pin.
	UART5_RXD	I	MFP6	UART5 data receiver input pin.
	I2C1_SDA	I/O	MFP9	I^2C1 data input/output pin.
	UART4_RXD	I	MFP11	UART4 data receiver input pin.
	BPWM0_CH4	I/O	MFP12	BPWM0 channel 4 output/capture input.
PI.4	PI.4	I/O	MFP0	General purpose digital I/O pin.
	UART4_TXD	O	MFP7	UART4 data transmitter output pin.
	UART0_TXD	O	MFP8	UART0 data transmitter output pin.
	UART1_TXD	O	MFP10	UART1 data transmitter output pin.
	EPWM0_CH5	I/O	MFP11	EPWM0 channel 5 output/capture input.
	CIR0_RXD	I	MFP14	CIR0 data receiver input pin.
	ACMP0_O	O	MFP15	Analog comparator 0 output pin.
PI.5	PI.5	I/O	MFP0	General purpose digital I/O pin.
	UART4_RXD	I	MFP7	UART4 data receiver input pin.
	UART0_RXD	I	MFP8	UART0 data receiver input pin.
	UART1_RXD	I	MFP10	UART1 data receiver input pin.

	Pin Name	Type	MFP	Description
	EPWM0_CH4	I/O	MFP11	EPWM0 channel 4 output/capture input.
	ACMP1_O	O	MFP15	Analog comparator 1 output pin.

Table 4.3-1 GPIO Multi-function Table

5 BLOCK DIAGRAM

5.1 NuMicro® M471V/M471K Block Diagram

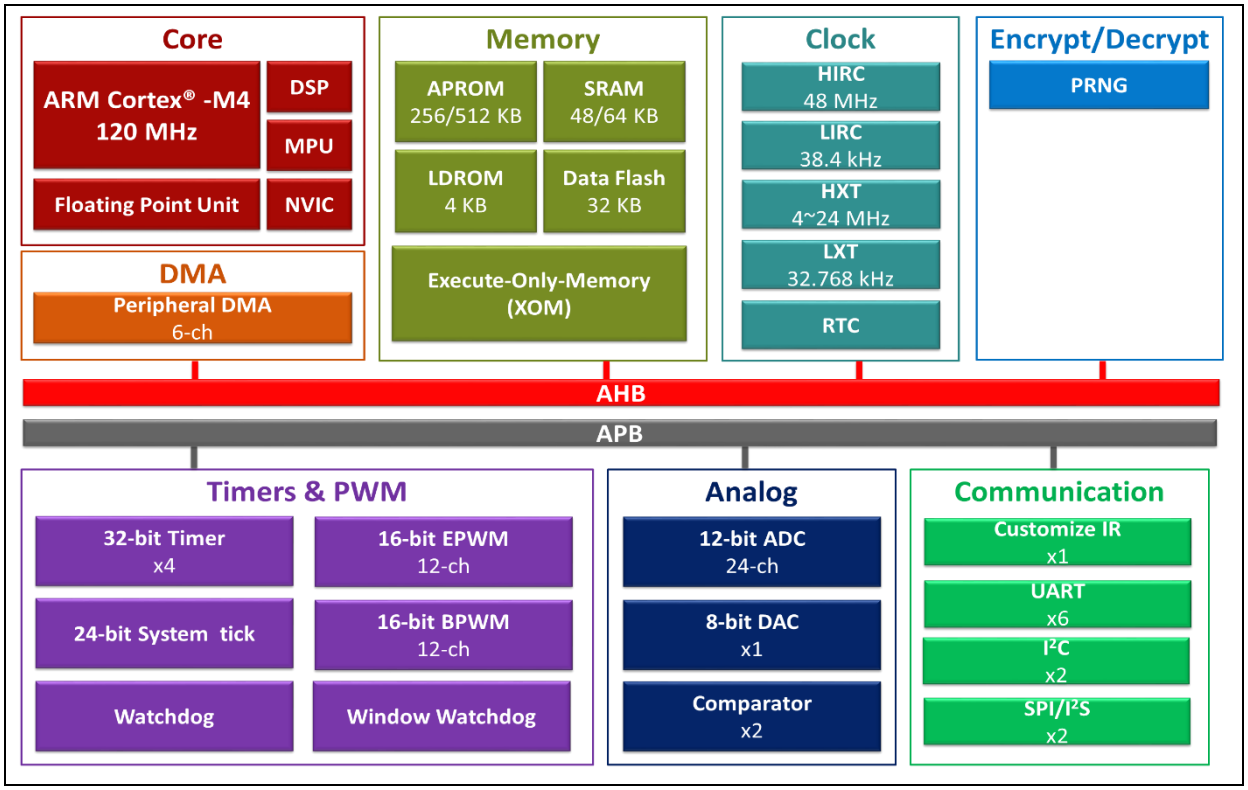


Figure 5.1-1 NuMicro® M471V/M471K Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 Arm® Cortex®-M4 Core

The Cortex®-M4 processor, a configurable, multistage, 32-bit RISC processor, has three AMBA AHB-Lite interfaces for best parallel performance and includes an NVIC component. The processor with optional hardware debug functionality can execute Thumb code and is compatible with other Cortex®-M profile processors. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. The Cortex®-M4F is a processor with the same capability as the Cortex®-M4 processor and includes floating point arithmetic functionality. The NuMicro® M471V/M471K series is embedded with Cortex®-M4F processor. Throughout this document, the name Cortex®-M4 refers to both Cortex®-M4 and Cortex®-M4F processors. Figure 6.1-1 shows the functional controller of the processor.

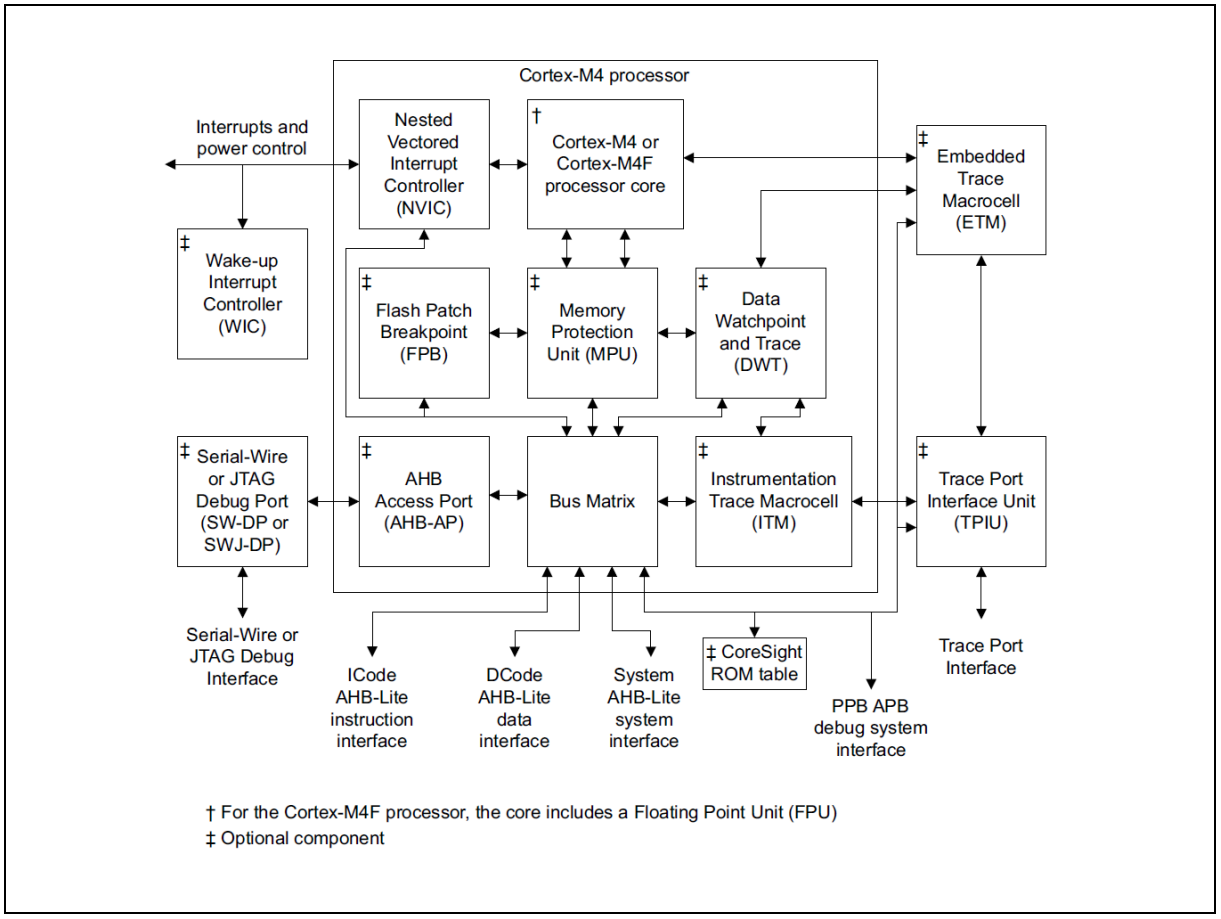


Figure 6.1-1 Cortex®-M4 Block Diagram

Cortex®-M4 processor features:

- A low gate count processor core, with low latency interrupt processing that has:
  - A subset of the Thumb instruction set, defined in the *ARMv7-M Architecture Reference Manual*
  - Banked Stack Pointer (SP)
  - Hardware integer divide instructions, SDIV and UDIV
  - Handler and Thread modes

- Thumb and Debug states
- Support for interruptible-continued instructions LDM, STM, PUSH, and POP for low interrupt latency
- Automatic processor state saving and restoration for low latency *Interrupt Service Routine (ISR)* entry and exit
- Support for ARMv6 big-endian byte-invariant or little-endian accesses
- Support for ARMv6 unaligned accesses

- Floating Point Unit (FPU) in the Cortex®-M4F processor providing:
  - 32-bit instructions for single-precision (C float) data-processing operations
  - Combined Multiply and Accumulate instructions for increased precision (Fused MAC)
  - Hardware support for conversion, addition, subtraction, multiplication with optional accumulate, division, and square-root
  - Hardware support for denormals and all IEEE rounding modes
  - 32 dedicated 32-bit single precision registers, also addressable as 16 double-word registers
  - Decoupled three stage pipeline
- Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing. Features include:
  - External interrupts. Configurable from 1 to 240 (the NuMicro® M471V/M471K series configured with 64 interrupts)
  - Bits of priority, configurable from 3 to 8
  - Dynamic reprioritization of interrupts
  - Priority grouping which enables selection of preempting interrupt levels and nonpreempting interrupt levels
  - Support for tril-chaining and late arrival of interrupts, which enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
  - Processor state automatically saved on interrupt entry, and restored on interrupt exit with on instruction overhead
  - Support for Wake-up Interrupt Controller (WIC) with Ultra-low Power Sleep mode
- Memory Protection Unit (MPU). An optional MPU for memory protection, including:
  - Eight memory regions
  - Sub Region Disable (SRD), enabling efficient use of memory regions
  - The ability to enable a background region that implements the default memory map attributes
- Low-cost debug solution that features:
  - Debug access to all memory and registers in the system, including access to memory mapped devices, access to internal core registers when the core is halted, and access to debug control registers even while SYSRESETn is asserted.
  - Serial Wire Debug Port(SW-DP) or Serial Wire JTAG Debug Port (SWJ-DP) debug access
  - Optional Flash Patch and Breakpoint (FPB) unit for implementing breakpoints and

code patches

- Optional Data Watchpoint and Trace (DWT) unit for implementing watchpoints, data tracing, and system profiling
- Optional Instrumentation Trace Macrocell (ITM) for support of printf() style debugging
- Optional Trace Port Interface Unit (TPIU) for bridging to a Trace Port Analyzer (TPA), including Single Wire Output (SWO) mode
- Optional Embedded Trace Macrocell (ETM) for instruction trace.

- Bus interfaces:
  - Three Advanced High-performance Bus-Lite (AHB-Lite) interfaces: ICode, Dcode, and System bus interfaces
  - Private Peripheral Bus (PPB) based on Advanced Peripheral Bus (APB) interface
  - Bit-band support that includes atomic bit-band write and read operations.
  - Memory access alignment
  - Write buffer for buffering of write data
  - Exclusive access transfers for multiprocessor systems

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Reset
- System Power Distribution
- SRAM Memory Orginization
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset sourcces are from peripheral signals. Software reset can trigger reset through setting control registers.

- Hardware Reset Sources
  - Power-on Reset
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex®-M4 core only by writing 1 to CPURST (SYS_IPRST0[1])

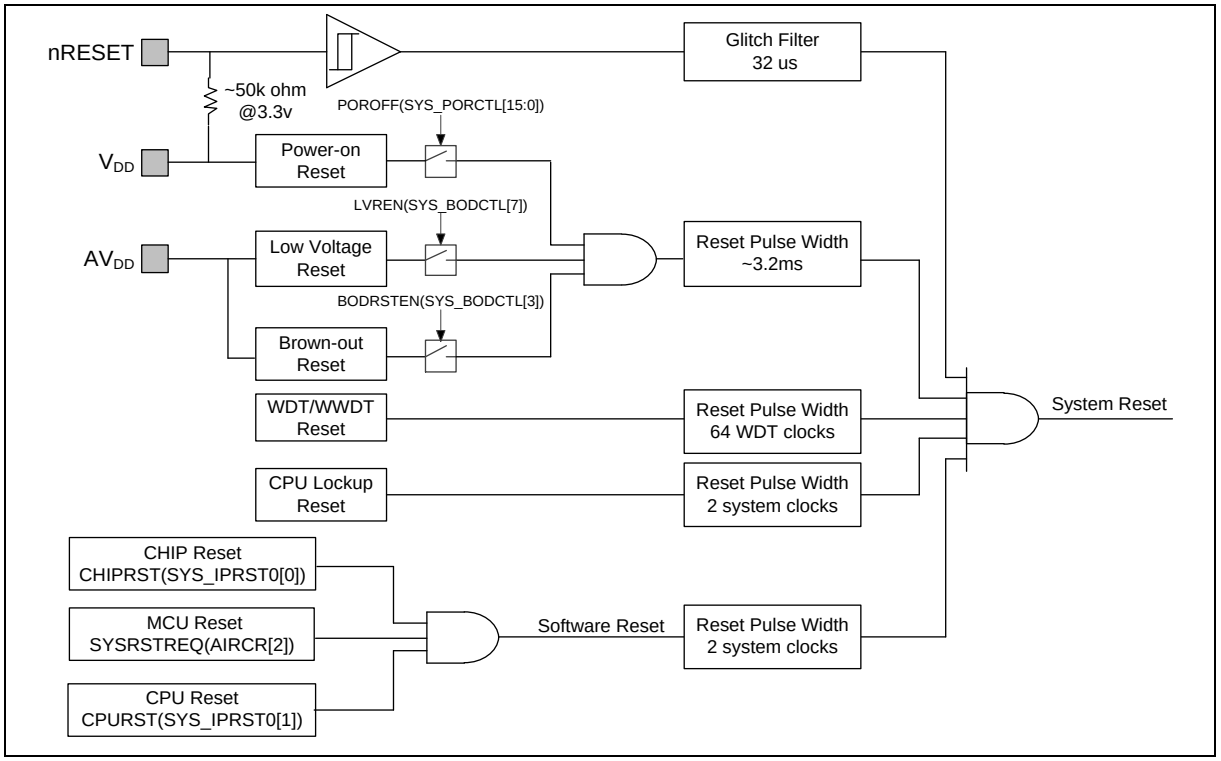


Figure 6.2-1 System Reset Sources

There are a total of 9 reset sources in the NuMicro® family. In general, CPU reset is used to reset Cortex®-M4 only; the other reset sources will reset Cortex®-M4 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6.2-1

Reset Sources **Register**	**POR**	**NRESET**	**WDT**	**LVR**	**BOD**	**Lockup**	**CHIP**	**MCU**	**CPU**
SYS_RSTSTS	Bit 0 = 1	Bit 1 = 1	Bit 2 = 1	Bit 3 = 1	Bit 4 = 1	Bit 8 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIPRST (SYS_IPRST0[0])	0x0	-	-	-	-	-	-	-	-
BODEN (SYS_BODCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
BODVL (SYS_BODCTL[2:1])									
BODRSTEN (SYS_BODCTL[3])									
HXTEN (CLK_PWRCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	
LXTEN (CLK_PWRCTL[1])	0x0	-	-	-	-	-	-	-	-
WDTCKEN (CLK_APBCLK0[0])	0x1	-	0x1	-	-	-	0x1	-	-
HCLKSEL	Reload from	Reload from	Reload from	Reload from	Reload from	Reload from	Reload from	Reload from	-

(CLK_CLKSEL0[2:0])	CONFIG0	CONFIG0	CONFIG0	CONFIG0	CONFIG0	CONFIG0	CONFIG0	CONFIG0	
WDTSEL (CLK_CLKSEL1[1:0])	0x3	0x3	-	-	-	-	-	-	-
HXTSTB (CLK_STATUS[0])	0x0	-	-	-	-	-	-	-	-
LXTSTB (CLK_STATUS[1])	0x0	-	-	-	-	-	-	-	-
PLLSTB (CLK_STATUS[2])	0x0	-	-	-	-	-	-	-	-
HIRCSTB (CLK_STATUS[4])	0x0	-	-	-	-	-	-	-	-
CLKSFAIL (CLK_STATUS[7])	0x0	0x0	-	-	-	-	-	-	-
RSTEN (WDT_CTL[1]) WDTEN (WDT_CTL[7])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
WDT_CTL except bit 1 and bit 7.	0x0700	0x0700	0x0700	0x0700	0x0700	-	0x0700	-	-
WDT_ALTCTL	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_RLDCNT	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CTL	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	-	0x3F0800	-	-
WWDT_STATUS	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CNT	0x3F	0x3F	0x3F	0x3F	0x3F	-	0x3F	-	-
BS (FMC_ISPCTL[1]) BL (FMC_ISPCTL[16])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
CBS (FMC_ISPSTS[2:1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
VECMAP (FMC_ISPSTS[23:9])	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	-	Reload base on CONFIG0	-	-
Other Peripheral Registers	Reset Value								-
FMC Registers	Reset Value								
Note: '-' means that the value of register keeps original setting.									

Table 6.2-1 Reset Value of Registers

6.2.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an

asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 V_{DD} and the state keeps longer than 32 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 V_{DD} and the state keeps longer than 32 us (glitch filter). The PINRF(SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6.2-2 shows the nRESET reset waveform.

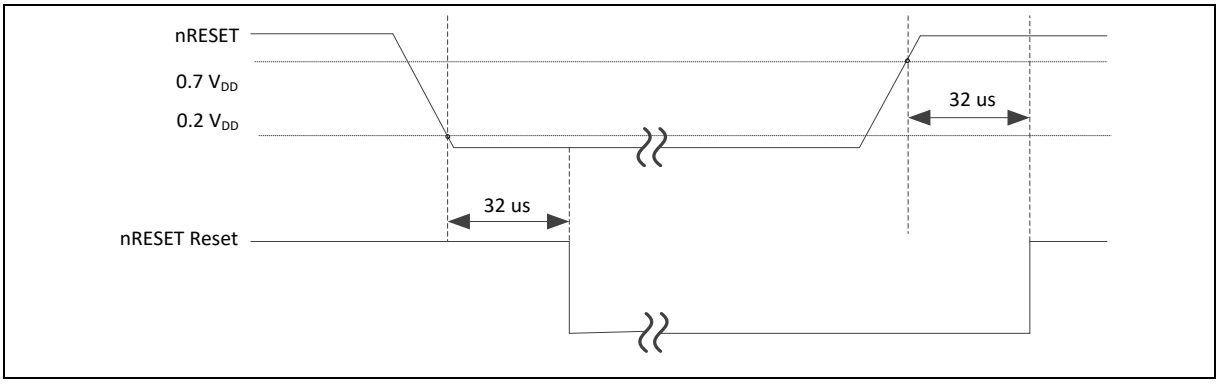


Figure 6.2-2 nRESET Reset Waveform

6.2.2.2 Power-on Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF(SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.2-3 shows the power-on reset waveform.

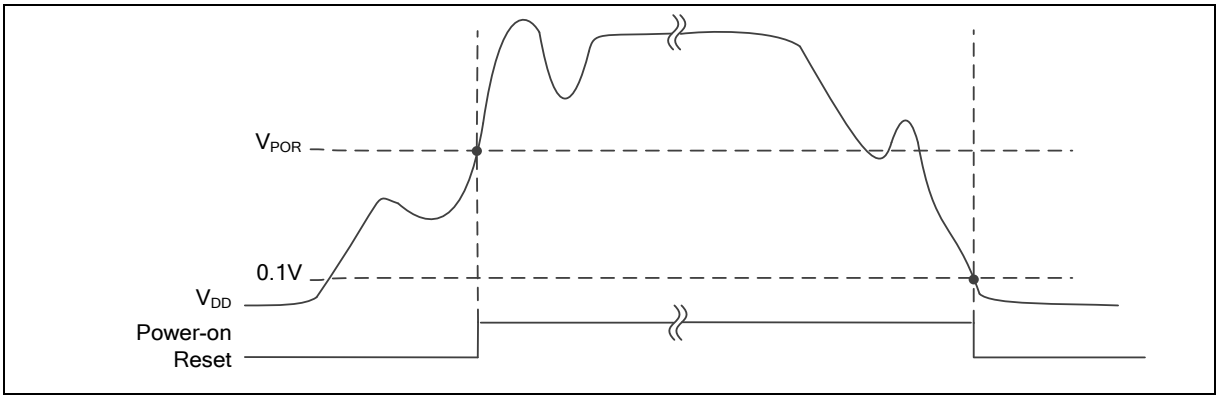


Figure 6.2-3 Power-on Reset (POR) Waveform

6.2.2.3 Low Voltage Reset (LVR)

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_BODCTL[7]) to 1, after 200us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6.2-4 shows the Low Voltage Reset waveform.

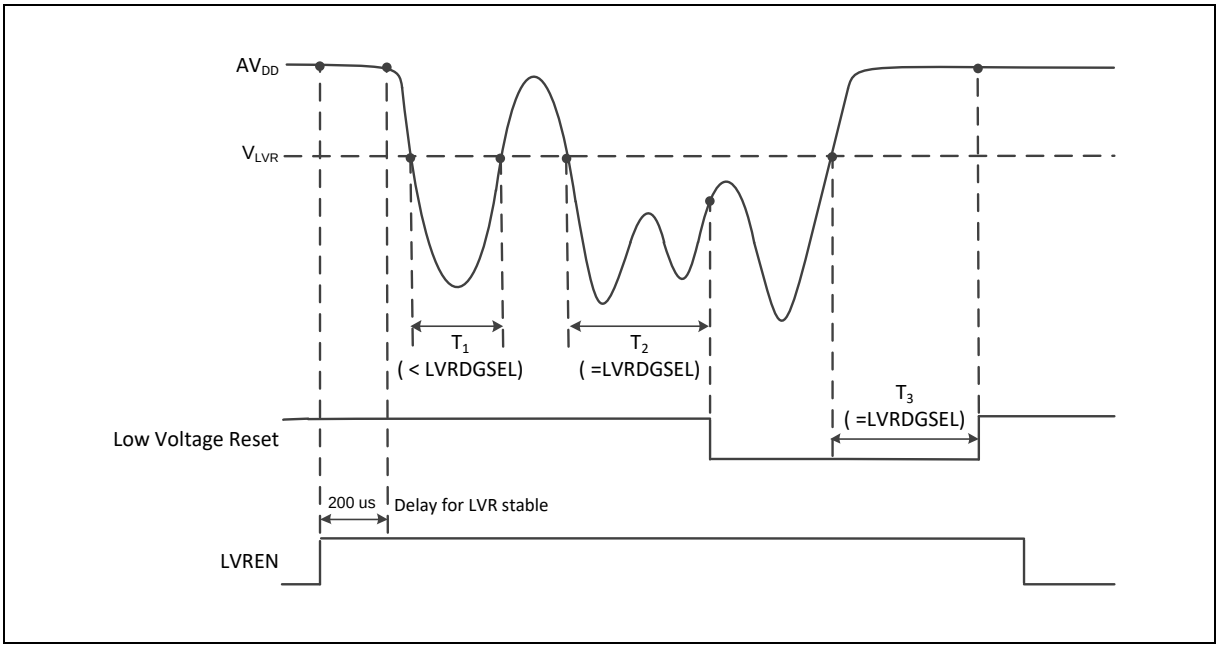


Figure 6.2-4 Low Voltage Reset (LVR) Waveform

6.2.2.4 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), Brown-out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} which is decided by BODEN and BODVL (SYS_BODCTL[17:16]) and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[10:8]), chip will be reset. The BOD reset will control the chip in reset state until the AV_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time set by BODDGSEL. The default value of BODEN, BODVL and BODRSTEN (SYS_BODCTL[3]) is set by Flash controller user configuration register CBODEN (CONFIG0 [19]), CBOV (CONFIG0 [22:21]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6.2-5 shows the Brown-out Detector waveform.

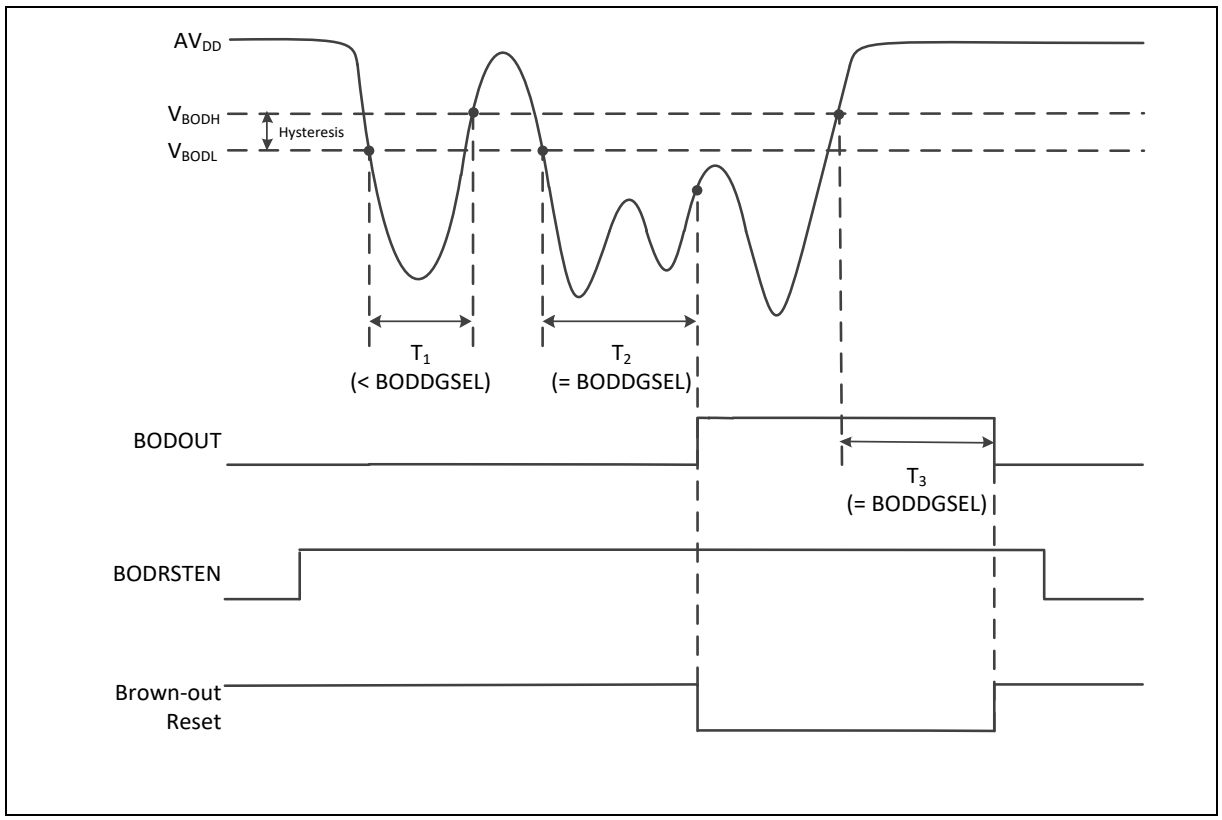


Figure 6.2-5 Brown-out Detector (BOD) Waveform

6.2.2.5 Watchdog Timer Reset (WDT)

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer(WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS_RSTSTS[2]).

6.2.2.6 CPU Lockup Reset

CPU enters lockup status after CPU produces hardfault at hardfault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an unrecoverable exception following the activation of the processor's built in system state protection hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

6.2.2.7 CPU Reset, CHIP Reset and MCU Reset

The CPU Reset means only Cortex®-M4 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST(SYS_IPRST0[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is same with Power-on Reset. The CPU and all peripherals are reset and BS(FMC_ISPCTL[1]) bit is automatically reloaded from CONFIG0 setting. User can set the CHIPRST(SYS_IPRST0[0]) to 1 to assert the CHIP Reset signal.

The MCU Reset is similar with CHIP Reset. The difference is that BS(FMC_ISPCTL[1]) will not be reloaded from CONFIG0 setting and keep its original software setting for booting from APROM or

LDROM. User can set the SYSRESETREQ(AIRCR[2]) to 1 to assert the MCU Reset.

6.2.3 System Power Distribution

In this chip, power distribution is divided into two segments:

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.8 V power for digital operation and I/O pins.

The outputs of internal voltage regulators (LDO) require an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}). Figure 6.2-6 shows the NuMicro® M471V/M471K power distribution.

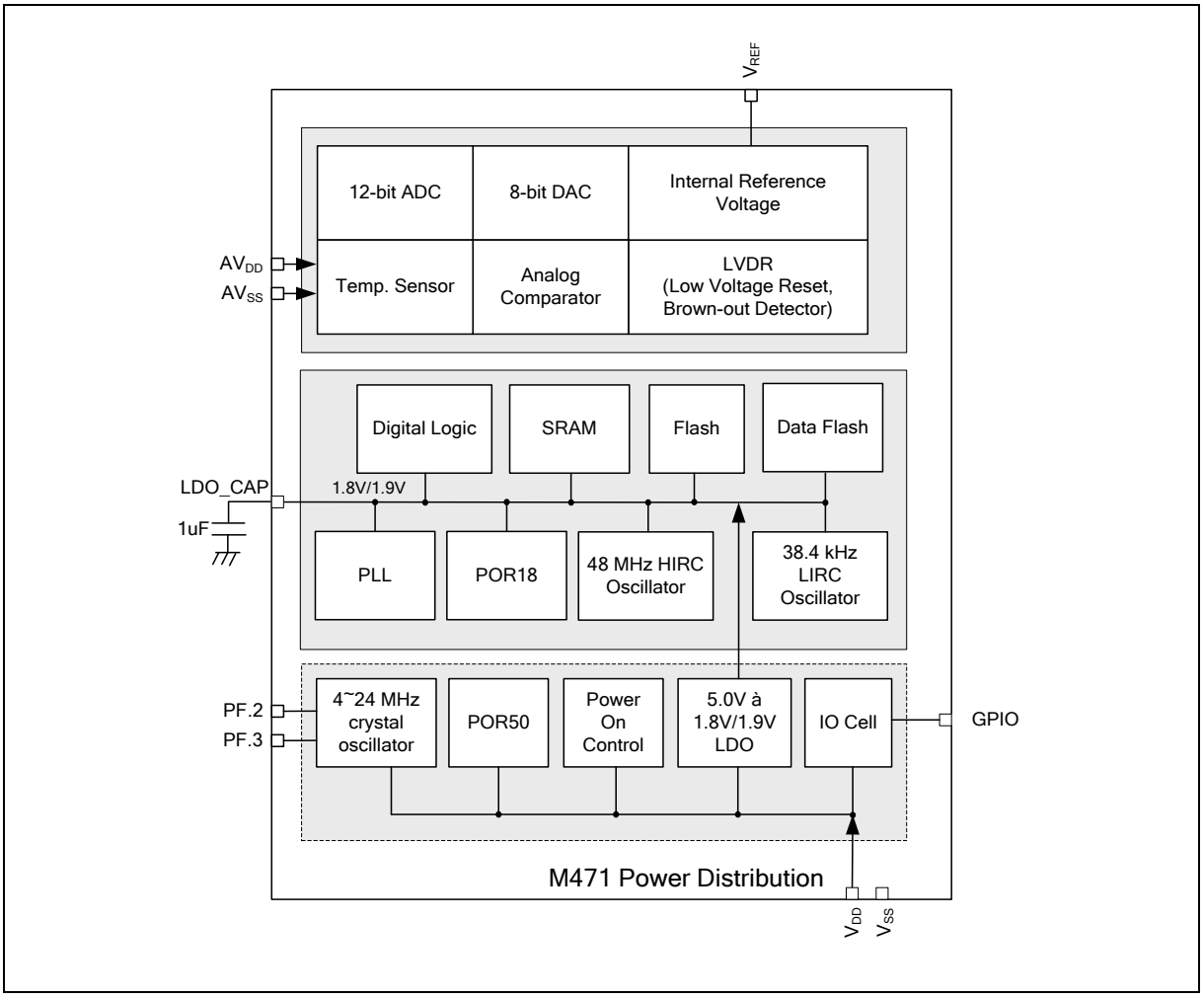


Figure 6.2-6 NuMicro® M471V/M471K Power Distribution Diagram

6.2.4 Power Modes and Wake-up Sources

The NuMicro® M471V/M471K series has power manager unit to support several operating modes for saving power. Table 6.2-2 lists all power modes in the M471V/M471K series.

Mode	CPU Operating Maximum Speed (MHz)	LDO_CAP (V)	Clock Disable
Normal mode	96	1.80	All clocks are disabled by control register.
Turbo mode	120	1.90	All clocks are disabled by control register.
Idle mode	CPU enter Sleep mode	1.80/1.90	Only CPU clock is disabled.
Normal Power-down mode (NPD)	CPU enters Deep Sleep mode	1.80/1.90	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.

Table 6.2-2 Power Mode Table

There are different power mode entry settings for each power mode. They have different entry setting and leaving condition. Table 6.2-3 shows the entry setting for each power mode. When chip power-on, chip is running at normal mode. User can enter each mode by setting SLEEPDEEP (SCR[2]), PDEN (CLK_PWRCTL[7]) and PDMSEL (CLK_PMUCTL[2:0]) and execute WFI instruction.

Register/Instruction Mode	SLEEPDEEP (SCR[2])	PDEN (CLK_PWRCTL[7])	PDMSEL (CLK_PMUCTL[2:0])	CPU Run WFI Instruction
Normal mode	0	0	0	NO
Idle mode	0	0	0	YES
Normal Power-down mode	1	1	0	YES

Table 6.2-3 Power Mode Difference Table

There are several wake-up sources in Idle mode and Power-down mode. Table 6.2-4 lists the available clocks for each power mode.

Power Mode	Normal Mode	Idle Mode	Power-Down Mode
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content retended.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-Up Sources	N/A	All interrupts	RTC, WDT, I²C, Timer, UART, GPIO, EINT, ACMP, CIR0 and BOD.
Available Clocks	All	All except CPU clock	LXT and LIRC
After Wake-Up	N/A	CPU back to normal mode	CPU back to normal mode

Table 6.2-4 Power Mode Definition Table

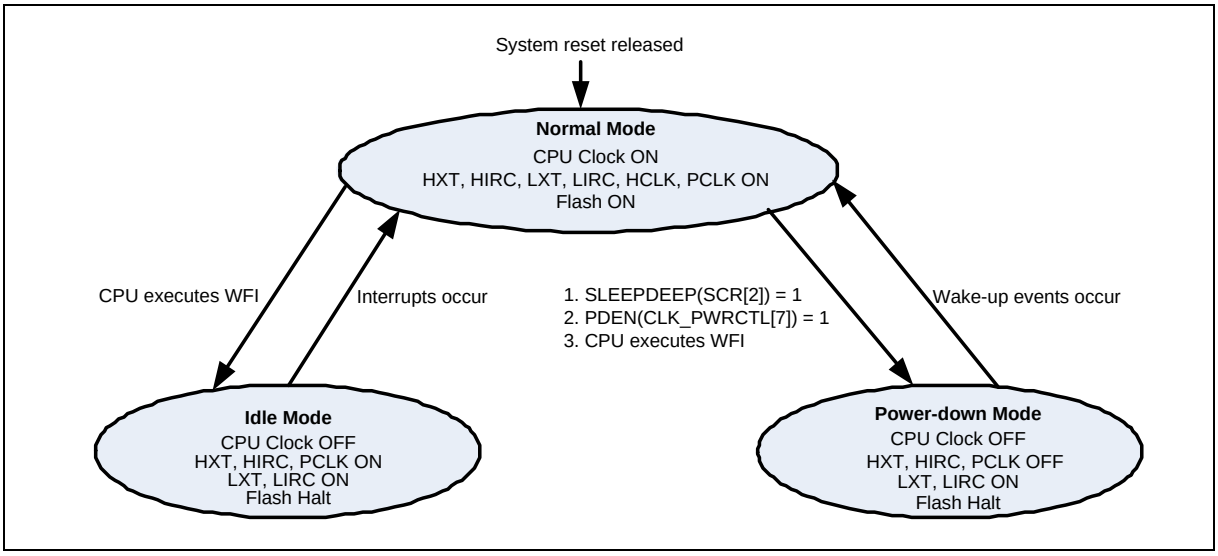


Figure 6.2-7 Power Mode State Machine

	Idle Mode	NPD
HXT	ON	Halt
HIRC	ON	Halt
LXT	ON	ON/OFF[1]
LIRC	ON	ON/OFF[2]
PLL	ON	Halt
HCLK/PCLK	ON	Halt
CPU	Halt	Halt
SRAM retention	ON	ON
FLASH	ON	Halt
TIMER	ON	ON/OFF[3]
WDT	ON	ON/OFF[4]
RTC	ON	ON/OFF[5]
UART	ON	ON/OFF[6]
CIR0	ON	ON/OFF[7]
Others	ON	Halt

Table 6.2-5 Clocks in Power Modes

Note:

1. LXT ON or OFF depends on SOFTWARE setting in normal mode.
2. LIRC ON or OFF depends on SOFTWARE setting in normal mode.
3. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is on.
4. If WDT clock source is selected as LIRC and LIRC is on.

5. If RTC clock source is selected as LXT and LXT is on.
6. If UART clock source is selected as LXT and LXT is on.
7. If CIR0 clock source is selected as LIRC/LXT and LIRC/LXT is on.

Wake-up sources in Normal Power-down mode (NPD):

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 6.2-6 lists the condition about how to enter Power-down mode again for each peripheral.

User needs to wait this condition before setting PDEN(CLK_PWRCTL[7]) and execute WFI to enter Power-down mode.

Wake-Up Source	Wake-Up Condition	Power-Down Mode	Re-Entering Power-Down Mode Condition
		NPD	
BOD	Brown-Out Detector Reset / Interrupt	V	After software writes 1 to clear BODIF (SYS_BODCTL[4]).
LVR	LVR Reset	V	After software writes 1 to clear LVRF (SYS_RSTSTS[3])
POR	POR Reset	V	After software writes 1 to clear PORF (SYS_RSTSTS[0])
EINT	External Interrupt	V	After software write 1 to clear the Px_INTSRC[n] bit.
GPIO	GPIO Interrupt	V	After software write 1 to clear the Px_INTSRC[n] bit.
TIMER	Timer Interrupt	V	After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]).
WDT	WDT Interrupt	V	After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect).
RTC	Alarm Interrupt	V	After software writes 1 to clear ALMIF (RTC_INTSTS[0]).
	Time Tick Interrupt	V	After software writes 1 to clear TICKIF (RTC_INTSTS[1]).
UART	nCTS Wake-Up	V	After software writes 1 to clear CTSWKF (UARTx_WKSTS[0]).
	RX Data Wake-Up	V	After software writes 1 to clear DATWKF (UARTx_WKSTS[1]).
	Received FIFO Threshold Wake-Up	V	After software writes 1 to clear RFRTWKF (UARTx_WKSTS[2]).
	RS-485 AAD Mode Wake-Up	V	After software writes 1 to clear RS485WKF (UARTx_WKSTS[3]).
	Received FIFO Threshold Time-out Wake-Up	V	After software writes 1 to clear TOUTWKF (UARTx_WKSTS[4]).
I^2C	Address match Wake-Up	V	After software writes 1 to clear WKAKDONE (I2C_WKSTS[1]). Then software writes 1 to clear WKIF(I2C_WKSTS[0]).
ACMP	Comparator Power-Down Wake-Up Interrupt	V	After software writes 1 to clear WKIF0 (ACMP_STATUS[8]) and WKIF1 (ACMP_STATUS[9]).
CIR0	CIR0 receive pattern match Wake-Up	V	After software writes 1 to clear PDWKF (CIR_STATUS[10]).

Table 6.2-6 Re-Entering Power-down Mode Condition

6.2.5 Power Modes and Power Level Transition

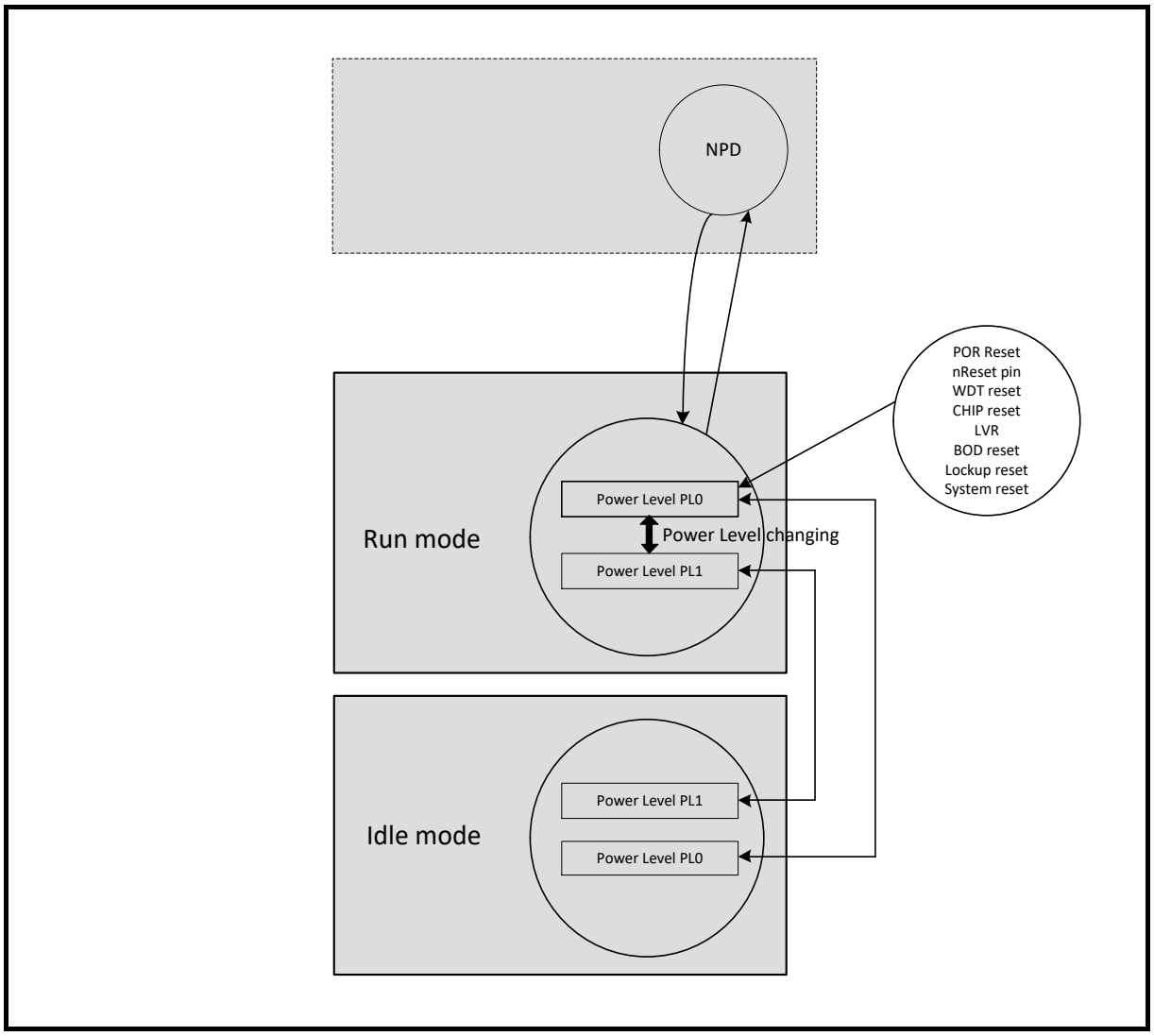


Figure 6.2-8 NuMicro® M471V/M471K Power Distribution Diagram

6.2.6 System Memory Map

The NuMicro® M471V/M471K series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.2-7. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. The NuMicro® M471V/M471K series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0007_FFFF	FLASH_BA	FLASH Memory Space (512 Kbytes)
0x0040_0000 – 0x0040_7FFF	DFLASH_BA	Data FLASH Memory Space (32 Kbytes)
0x2000_0000 – 0x2000_7FFF	SRAM0_BA	SRAM Memory Space (32 Kbytes)
0x2000_8000 – 0x2000_FFFF	SRAM1_BA	SRAM Memory Space (32 Kbytes)
Peripheral Controllers Space (0x4000_0000 – 0x400F_FFFF)		

0x4000_0000 – 0x4000_01FF	SYS_BA	System Control Registers
0x4000_0200 – 0x4000_02FF	CLK_BA	Clock Control Registers
0x4000_0300 – 0x4000_03FF	NMI_BA	NMI Control Registers
0x4000_4000 – 0x4000_4FFF	GPIO_BA	GPIO Control Registers
0x4000_8000 – 0x4000_8FFF	PDMA_BA	Peripheral DMA Control Registers
0x4000_C000 – 0x4000_CFFF	FMC_BA	Flash Memory Control Registers
0x4000_F000 – 0x4000_FFFF	DFMC_BA	Data Flash Memory Control Registers
0x4003_1000 – 0x4003_1FFF	CRC_BA	CRC Generator Registers
APB Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4004_0000 – 0x4004_00FF	WDT_BA	Watchdog Timer Control Registers
0x4004_0100 – 0x4004_0FFF	WWDT_BA	Window Watchdog Timer Control Registers
0x4004_1000 – 0x4004_1FFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4004_3000 – 0x4004_3FFF	EADC0_BA	Enhanced Analog-Digital-Converter 0 (EADC0) Control Registers
0x4004_5000 – 0x4004_5FFF	ACMP01_BA	Analog Comparator 0/ 1 Control Registers
0x4004_7000 – 0x4004_7FFF	DAC_BA	DAC Control Registers
0x4005_0000 – 0x4005_0FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4005_1000 – 0x4005_1FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4005_8000 – 0x4005_8FFF	EPWM0_BA	EPWM0 Control Registers
0x4005_9000 – 0x4005_9FFF	EPWM1_BA	EPWM1 Control Registers
0x4005_A000 – 0x4005_AFFF	BPWM0_BA	BPWM0 Control Registers
0x4005_B000 – 0x4005_BFFF	BPWM1_BA	BPWM1 Control Registers
0x4005_F000 – 0x4005_FFFF	CIR0_BA	Custermize IR Control Registers
0x4006_1000 – 0x4006_1FFF	SPI0_BA	SPI0 Control Registers
0x4006_2000 – 0x4006_2FFF	SPI1_BA	SPI1 Control Registers
0x4007_0000 – 0x4007_0FFF	UART0_BA	UART0 Control Registers
0x4007_1000 – 0x4007_1FFF	UART1_BA	UART1 Control Registers
0x4007_2000 – 0x4007_2FFF	UART2_BA	UART2 Control Registers
0x4007_3000 – 0x4007_3FFF	UART3_BA	UART3 Control Registers
0x4007_4000 – 0x4007_4FFF	UART4_BA	UART4 Control Registers
0x4007_5000 – 0x4007_5FFF	UART5_BA	UART5 Control Registers
0x4008_0000 – 0x4008_0FFF	I2C0_BA	I^2C0 Control Registers
0x4008_1000 – 0x4008_1FFF	I2C1_BA	I^2C1 Control Registers
0x400B_A000 – 0x400B_AFFF	PRNG_BA	PRNG Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers

0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6.2-7 Address Space Assignments for On-Chip Controllers

6.2.7 SRAM Memory Orginization

The M471V/M471K supports embedded SRAM with total 64 Kbytes size and the SRAM organization is separated to two banks: SRAM bank0 and SRAM bank1. The first bank has 32 Kbytes address space, the second bank has 32 Kbyte address space. These two banks address space can be accessed simultaneously. The SRAM bank0 supports parity error check to make sure chip operating more stable.

- Supports total 64 Kbytes SRAM
- Supports byte / half word / word write
- Supports fixed 32 Kbytes SRAM bank0 for independent access
- Supports parity error check function for SRAM bank0
- Supports oversize response error
- Supports remap address to 0x1000_0000

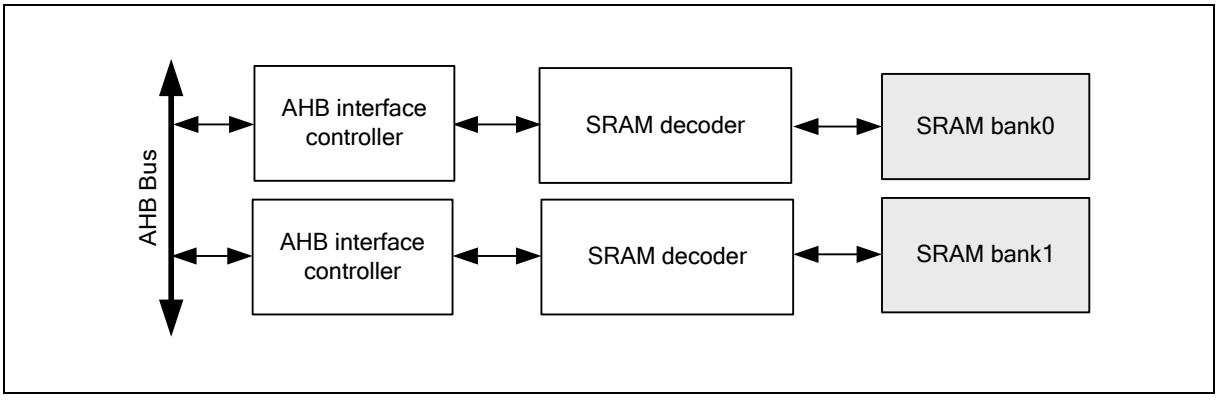


Figure 6.2-9 SRAM Block Diagram

Figure 6.2-9 shows the SRAM organization of M471. There are two SRAM banks in M471. The bank0 is addressed to 32 Kbytes and the bank1 is addressed to 32 Kbytes. The bank0 address space is from 0x2000_0000 to 0x2000_7FFF. The bank1 address space is from 0x2000_8000 to 0x2000_FFFF. The address between 0x2001_0000 to 0x3FFF_FFFF is illegal memory space and chip will enter hardfault if CPU accesses these illegal memory addresses.

The address of each bank is remapping from 0x2000_0000 to 0x1000_0000. CPU can access SRAM bank0 through 0x2000_0000 to 0x2000_7FFF or 0x1000_0000 to 0x1000_7FFF, and access SRAM bank1 through 0x2000_8000 to 0x2000_FFFF or 0x1000_8000 to 0x1000_FFFF.

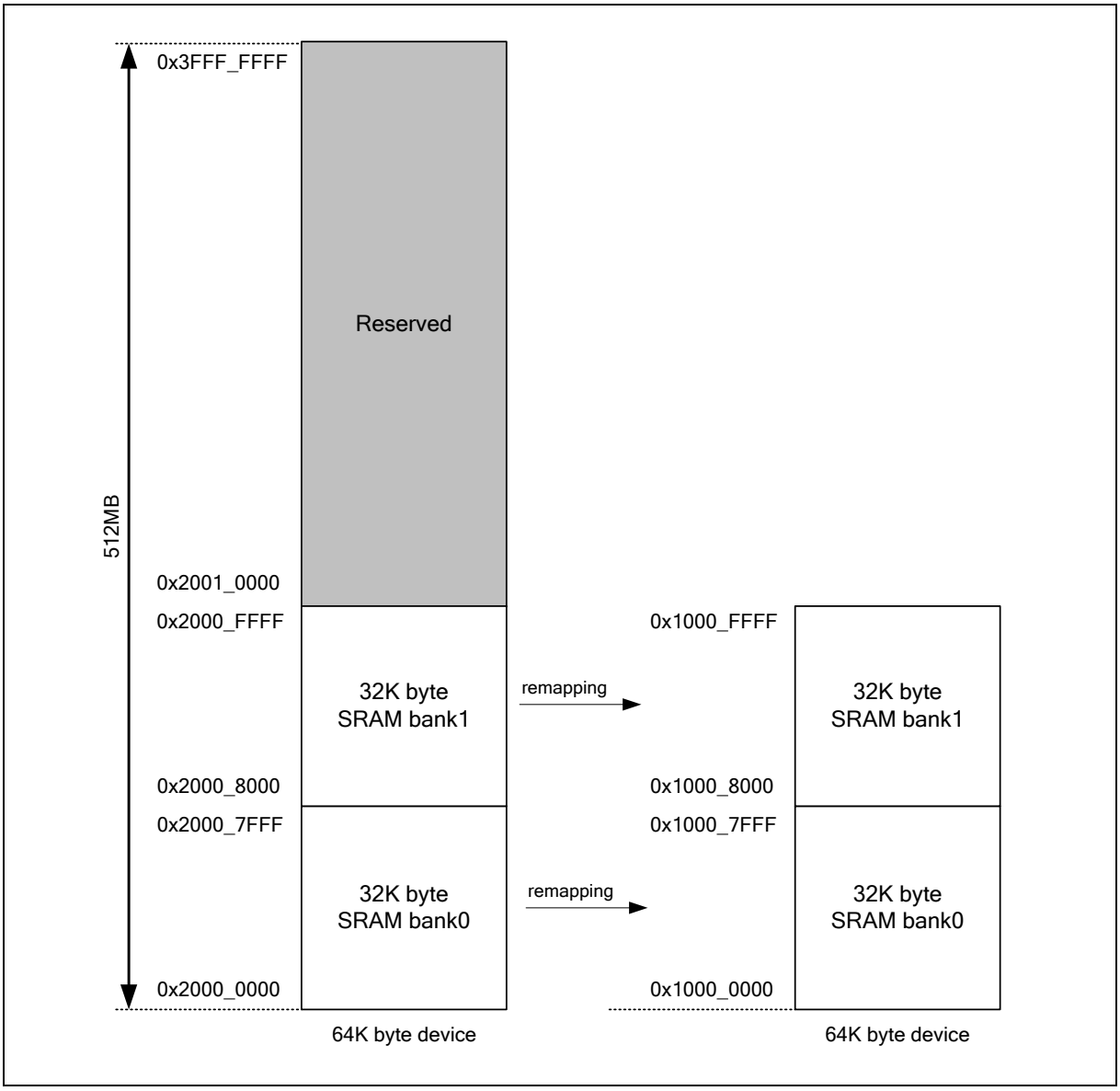


Figure 6.2-10 SRAM Memory Organization

SRAM bank0 has byte parity error check function. When CPU is accessing SRAM bank0, the parity error checking mechanism is dynamic operating. As parity error occured, the PERRIF (SYS_SRAM_STATUS[0]) will be asserted to 1 and the SYS_SRAM_ERRADDR register will recode the address with parity error. Chip will enter interrupt when SRAM parity error occurred if PERRIEN (SYS_SRAM_INTCTL[0]) is set to 1. When SRAM parity error occured, chip will stop detecting SRAM parity error until user writes 1 to clear the PERRIF(SYS_SRAM_STATUS[0]) bit.

6.2.8 Bus Matrix

The M471V/M471K supports Bus Matrix to manage the access arbitration between masters. The access arbitration can be selected by INTACTEN (SYS_AHBMCTL[0]) to use round-robin algorithm or set Cortex®-M4 CPU as the highest bus priority.

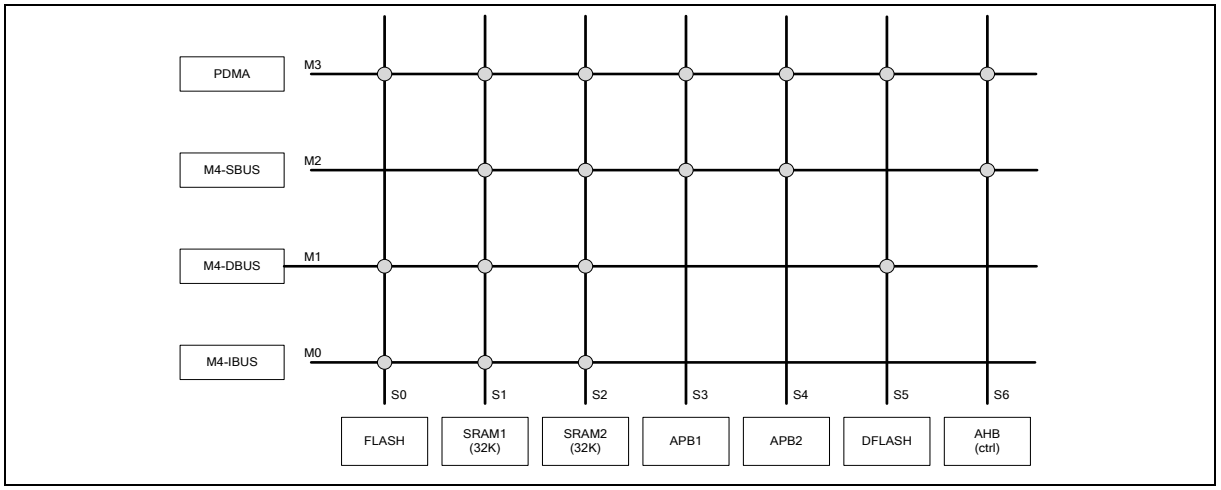


Figure 6.2-11 NuMicro® M471V/M471K Bus Matrix Diagram

6.2.9 HIRC Auto Trim

This chip supports auto-trim function: the HIRC trim (48 MHz RC oscillator), according to the accurate LXT (32.768 kHz crystal oscillator), automatically gets accurate HIRC output frequency, 0.25 % deviation within all temperature ranges.

For instance, the system needs an accurate 48 MHz clock. In such case, if neither using PLL as the system clock source nor soldering 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_IRCTCTL[10] reference clock selection) to “1”, set FREQSEL (SYS_IRCTCTL[1:0] trim frequency selection) to “01”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_IRCTISTS[0] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within 0.25% deviation.

6.2.10 Internal V_{REF}

This chip supports internal V_{REF} function, depend on setting of VREFCTL(SYS_VREFCTL[4:0]) to generate different reference voltage for ADC/DAC/ACMP. User has to enable PRELOADEN (SYS_VREFCTL[6]) to fit the Tstable when VREFCTL(SYS_VREFCTL[4:0]) change setting (except set to 00000) to make sure that V_{REF} works well. Tstable depends on different situations has different requirement, please refer to the relative Datasheet.

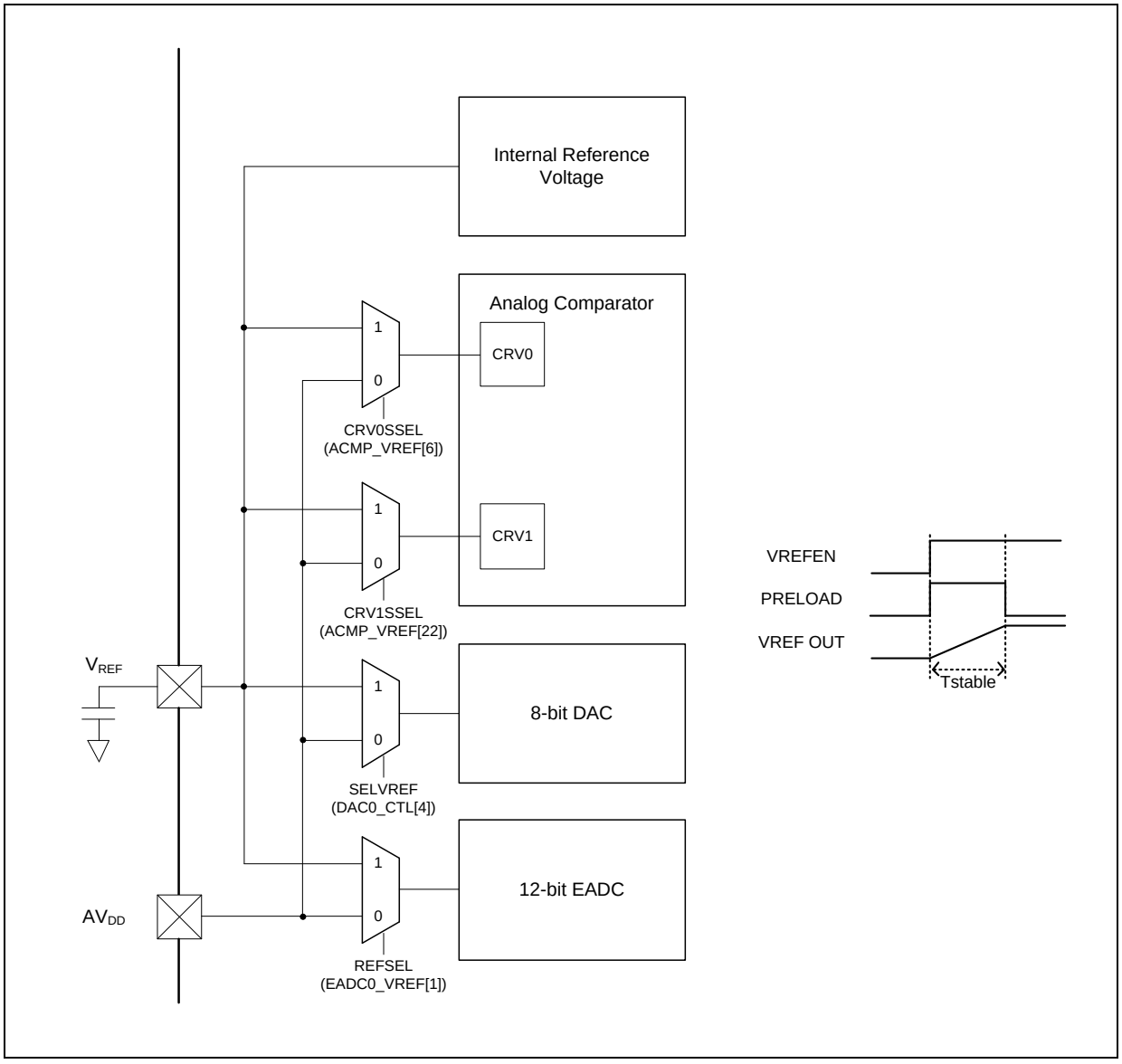


Figure 6.2-12 NuMicro® M471V/M471K V_{REF} Diagram

6.2.11 UART0_TXD Modulation with EPWM

This chip supports UART0_TXD to modulate with EPWM channel. User can set MODPWMSEL(SYS_MODCTL[7:4]) to choose which EPWM0 channel to modulate with UART0_TXD and set MODEN(SYS_MODCTL[0]) to enable modulation function. User can set TXDINV(UART_LINE[8]) to inverse UART0_TXD before modulating with EPWM.

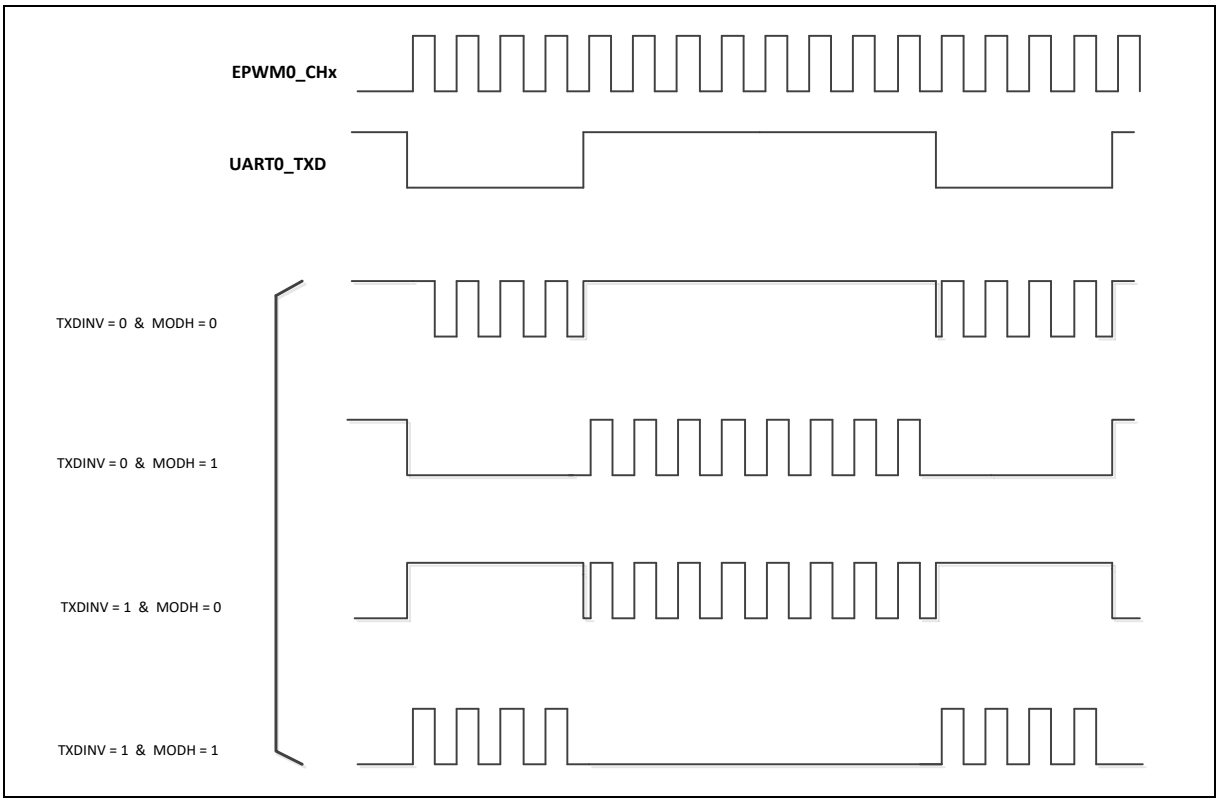


Figure 6.2-11 UART0_TXD Modulated with EPWM Channel

6.2.12 Register Lock Control

Some of the system control registers need to be protected to avoid inadvertent write and disturb the chip operation. These system control registers are protected after the power-on reset till user disables register protection. For user to program these protected registers, a register protection disable sequence needs to be followed by a special programming. The register protection disable sequence is writing the data “59h”, “16h” “88h” to the register SYS_REGLCTL address at 0x4000_0100 continuously. Any different data value, different sequence or any other write to other address during these three data writing will abort the whole sequence.

SYS_IPRST0	**Address 0x4000_0008**
SYS_ALTCTL	address 0x4000_0014
SYS_BODCTL	address 0x4000_0018
SYS_PORCTL	address 0x4000_0024
SYS_VREFCTL	address 0x4000_0028
SYS_SRAM_BISTCTL	address 0x4000_00D0
SYS_SRAM_PARITY	address 0x4000_00D8
SYS_RCADJ	address 0x4000_0110

SYS_HIRC2TCTL	address 0x4000_018C
SYS_HXTTCTL	address 0x4000_0190
SYS_ACMPTCTL	address 0x4000_0194
SYS_PORDISAN	address 0x4000_01EC
SYS_PLCTL	address 0x4000_01F8
CLK_PWRCTL	address 0x4000_0200
CLK_APBCLK0	address 0x4000_0208
CLK_CLKSEL0	address 0x4000_0210
CLK_CLKSEL1	address 0x4000_0214
CLK_PLLCTL	address 0x4000_0240
CLK_PLL2CTL	address 0x4000_0244
CLK_PLLTEST	address 0x4000_0248
CLK_PMUCTL	address 0x4000_0290
NMIEN	address 0x4000_0300
AHBMCTL	address 0x4000_0400
FMC_FTCTL	address 0x4000_5018
FMC_ICPCMD	address 0x4000_501C
FMC_ISPCTL	address 0x4000_C000
FMC_ISPTRG	address 0x4000_C010
FMC_FTCTL	address 0x4000_C018
FMC_ICPCTL	address 0x4000_C01C
FMC_ISPSTS	address 0x4000_C040
FMC_CYCCTL	address 0x4000_C04C
FMC_KPKEYTRG	address 0x4000_C05C
FMC_KPKEYSTS	address 0x4000_C060
WDT_CTL	address 0x4004_0000
WDT_ALTCTL	address 0x4004_0004
EADC_TEST	address 0x4004_3200
ACMP_TEST	address 0x4004_5FF8
DAC0_TEST	address 0x4004_7FF0
DAC1_TEST	address 0x4004_7FF8
TIMER0_CTL	address 0x4005_0000
TIMER1_CTL	address 0x4005_0100
TIMER2_CTL	address 0x4005_1000
TIMER3_CTL	address 0x4005_1100

TIMER0_PWMCTL	address 0x4005_0040
TIMER1_PWMCTL	address 0x4005_0140
TIMER2_PWMCTL	address 0x4005_1040
TIMER3_PWMCTL	address 0x4005_1140
TIMER0_PWMDTCTL	address 0x4005_0058
TIMER1_PWMDTCTL	address 0x4005_0158
TIMER2_PWMDTCTL	address 0x4005_1058
TIMER3_PWMDTCTL	address 0x4005_1158
TIMER0_PWMBRKCTL	address 0x4005_0070
TIMER1_PWMBRKCTL	address 0x4005_0170
TIMER2_PWMBRKCTL	address 0x4005_1070
TIMER3_PWMBRKCTL	address 0x4005_1170
TIMER0_PWMSWBRK	address 0x4005_007C
TIMER1_PWMSWBRK	address 0x4005_017C
TIMER2_PWMSWBRK	address 0x4005_107C
TIMER3_PWMSWBRK	address 0x4005_117C
TIMER0_PWMINTEN1	address 0x4005_0084
TIMER1_PWMINTEN1	address 0x4005_0184
TIMER2_PWMINTEN1	address 0x4005_1084
TIMER3_PWMINTEN1	address 0x4005_1184
TIMER0_PWMINTSTS1	address 0x4005_008C
TIMER1_PWMINTSTS1	address 0x4005_018C
TIMER2_PWMINTSTS1	address 0x4005_108C
TIMER3_PWMINTSTS1	address 0x4005_118C
EPWM_CTL0	address 0x4005_8000/0x4005_9000
EPWM_CTL1	address 0x4005_8000/0x4005_9000
EPWM_DTCTL0_1	address 0x4005_8070/0x4005_9070
EPWM_DTCTL2_3	address 0x4005_8074/0x4005_9074
EPWM_DTCTL4_5	address 0x4005_8078/0x4005_9078
EPWM_BRKCTL0_1	address 0x4005_80C8/0x4005_90C8
EPWM_BRKCTL2_3	address 0x4005_80CC/0x4005_90CC
EPWM_BRKCTL4_5	address 0x4005_80D0/0x4005_90D0
EPWM_SWBRK	address 0x4005_80DC/0x4005_90DC
EPWM_INTEN1	address 0x4005_80E4/0x4005_90E4
EPWM_INTSTS1	address 0x4005_80EC/0x4005_90EC

EPWM_SELFTEST	address 0x4005_8300/0x4005_9300
BPWM_CTL0	address 0x4005_A000/0x4005_B000
BPWM_SELFTEST	address 0x4005_A030/0x4005_B030
SYST_VAL	address 0xE000_E018

6.2.13 System Timer (SysTick)

The Cortex®-M4 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_VAL) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_LOAD) on the next clock cycle, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_VAL value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_LOAD value rather than an arbitrary value when it is enabled.

If the SYST_LOAD is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the "*Arm® Cortex®-M4 Technical Reference Manual*" and "*Arm® v6-M Architecture Reference Manual*".

6.2.14 Nested Vectored Interrupt Controller (NVIC)

The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked, or nested, interrupts to enable tail-chaining of interrupts. You can only fully access the NVIC from privileged mode, but you can cause interrupts to enter a pending state in user mode if you enable the Configuration and Control Register. Any other user mode access causes a bus fault. You can access all NVIC registers using byte, halfword, and word accesses unless otherwise stated. NVIC registers are located within the SCS (System Control Space). All NVIC registers and system debug registers are little-endian regardless of the endianness state of the processor.

The NVIC supports:

- An implementation-defined number of interrupts, in the range 1-240 interrupts.
- A programmable priority level of 0-16 for each interrupt; a higher level corresponds to a lower priority, so level 0 is the highest interrupt priority.
- Level and pulse detection of interrupt signals.
- Dynamic reprioritization of interrupts.
- Grouping of priority values into group priority and subpriority fields.
- Interrupt tail-chaining.
- An external Non Maskable Interrupt (NMI)
- WIC with Ultra-low Power Sleep mode support

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead. This provides low latency exception handling.

6.2.14.1 Exception Model and System Interrupt Map

Table 6.2-8 lists the exception model supported by M471V/M471K series. Software can set 16 levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0x00” and the lowest priority is denoted as “0xF0” (The 4-LSB always 0). The default priority of all the user-configurable interrupts is “0x00”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

When any interrupts is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. On system reset, the vector table is fixed at address 0x00000000. Privileged software can write to the VTOR to relocate the vector table start address to a different memory location, in the range 0x00000080 to 0x3FFFFF80,

The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Exception Type	Vector Number	Vector Address	Priority
Reset	1	0x00000004	-3
NMI	2	0x00000008	-2
Hard Fault	3	0x0000000C	-1
Memory Manager Fault	4	0x00000010	Configurable
Bus Fault	5	0x00000014	Configurable
Usage Fault	6	0x00000018	Configurable
Reserved	7 ~ 10		Reserved

SVCall	11	0x0000002C	Configurable
Debug Monitor	12	0x00000030	Configurable
Reserved	13		Reserved
PendSV	14	0x00000038	Configurable
SysTick	15	0x0000003C	Configurable
Interrupt (IRQ0 ~ IRQ)	16 ~ 111	0x00000000 + (Vector Number)*4	Configurable

Table 6.2-8 Exception Model

Vector Number	Interrupt Number (Bit in Interrupt Registers)	Interrupt Name	Interrupt Description
0 ~ 15	-	-	System exceptions
16	0	BODOUT	Brown-Out low voltage detected interrupt
17	1	IRC_INT	IRC TRIM interrupt
18	2	PWRWU_INT	Clock controller interrupt for chip wake-up from power-down state
19	3	SRAM_PERR	SRAM parity check error interrupt
20	4	CLKFAIL	Clock fail detected interrupt
21	5	FMC_INT	FMC ISP interrupt
22	6	RTC_INT	Real time clock interrupt
23	7	TAMP_INT	Tamper interrupt
24	8	WDT_INT	Watchdog Timer interrupt
25	9	WWDT_INT	Window Watchdog Timer interrupt
26	10	EINT0	External interrupt from PA.6 or PB.5 pins
27	11	EINT1	External interrupt from PA.7, PB.4 or PD.15pins
28	12	EINT2	External interrupt from PB.3 or PC.6 pin
29	13	EINT3	External interrupt from PB.2 or PC.7 pin
30	14	EINT4	External interrupt from PA.8, PB.6 or PF.15 pin
31	15	EINT5	External interrupt from PB.7, PD.12 or PF.14 pin
32	16	GPA_INT	External interrupt from PA[15:0] pin
33	17	GPB_INT	External interrupt from PB[15:0] pin
34	18	GPC_INT	External interrupt from PC[15:0] pin
35	19	GPD_INT	External interrupt from PD[15:0] pin
36	20	GPE_INT	External interrupt from PE[15:0] pin
37	21	GPF_INT	External interrupt from PF[15:0] pin
38	22	Reserved	Reserved

39	23	SPI0_INT	SPI0 interrupt
40	24	BRAKE0_INT	EPWM0 brake interrupt
41	25	EPWM0_P0_INT	EPWM0 pair 0 interrupt
42	26	EPWM0_P1_INT	EPWM0 pair 1 interrupt
43	27	EPWM0_P2_INT	EPWM0 pair 2 interrupt
44	28	BRAKE1_INT	EPWM1 brake interrupt
45	29	EPWM1_P0_INT	EPWM1 pair 0 interrupt
46	30	EPWM1_P1_INT	EPWM1 pair 1 interrupt
47	31	EPWM1_P2_INT	EPWM1 pair 2 interrupt
48	32	TMR0_INT	Timer 0 interrupt
49	33	TMR1_INT	Timer 1 interrupt
50	34	TMR2_INT	Timer 2 interrupt
51	35	TMR3_INT	Timer 3 interrupt
52	36	UART0_INT	UART0 interrupt
53	37	UART1_INT	UART1 interrupt
54	38	I2C0_INT	I^2C0 interrupt
55	39	I2C1_INT	I^2C1 interrupt
56	40	PDMA_INT	PDMA interrupt
57	41	DAC_INT	DAC interrupt
58	42	EADC0_INT0	EADC0 interrupt source 0
59	43	EADC0_INT1	EADC0 interrupt source 1
60	44	ACMP01_INT	ACMP0 and ACMP1 interrupt
61	45	Reserved	Reserved
62	46	EADC0_INT2	EADC0 interrupt source 2
63	47	EADC0_INT3	EADC0 interrupt source 3
64	48	UART2_INT	UART2 interrupt
65	49	UART3_INT	UART3 interrupt
66	50	Reserved	Reserved
67	51	SPI1_INT	SPI1 interrupt
68	52	Reserved	Reserved
69	53	Reserved	Reserved
70	54	Reserved	Reserved
71	55	Reserved	Reserved
72	56	Reserved	Reserved
73	57	Reserved	Reserved

74	58	Reserved	Reserved
75	59	Reserved	Reserved
76	60	Reserved	Reserved
77	61	Reserved	Reserved
78	62	Reserved	Reserved
80	64	Reserved	Reserved
81	65	Reserved	Reserved
82	66	Reserved	Reserved
83	67	Reserved	Reserved
84	68	Reserved	Reserved
85	69	Reserved	Reserved
86	70	Reserved	Reserved
87	71	PRNG_INT	PRNG interrupt
88	72	GPG_INT	External interrupt from PG[15:0] pin
89	73	EINT6	External interrupt from PB.8 or PD.11 pin
90	74	UART4_INT	UART4 interrupt
91	75	UART5_INT	UART5 interrupt
92	76	Reserved	Reserved
93	77	Reserved	Reserved
94	78	BPWM0_INT	BPWM0 interrupt
95	79	BPWM1_INT	BPWM1 interrupt
96	80	Reserved	Reserved
97	81	Reserved	Reserved
98	82	Reserved	Reserved
99	83	Reserved	Reserved
100	84	Reserved	Reserved
101	85	Reserved	Reserved
102	86	Reserved	Reserved
103	87	Reserved	Reserved
105	88	GPH_INT	External interrupt from PH[11:0] pin
105	89	EINT7	External interrupt from PB.9 or PD.10 pin
106	90	Reserved	Reserved
107	91	Reserved	Reserved
108	92	Reserved	Reserved
109	93	Reserved	Reserved

110	94	Reserved	Reserved
111	95	Reserved	Reserved
112	96	Reserved	Reserved
113	97	Reserved	Reserved
114	98	Reserved	Reserved
115	99	Reserved	Reserved
116	100	Reserved	Reserved
117	101	Reserved	Reserved
118	102	Reserved	Reserved
119	103	Reserved	Reserved
120	104	Reserved	Reserved
121	105	Reserved	Reserved
122	106	Reserved	Reserved
123	107	Reserved	Reserved
124	108	Reserved	Reserved
125	109	Reserved	Reserved
126	110	GPI_INT	External interrupt from PI[5:0] pin
127	111	CIR0_INT	CIR0 interrupt

Table 6.2-9 Interrupt Number Table

6.2.14.2 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(CLK_PWRCTL[7]) and Cortex®-M4 core executes the WFI instruction. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT) and 48 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. Figure 6.3-1 shows the clock generator and the overview of the clock source control.

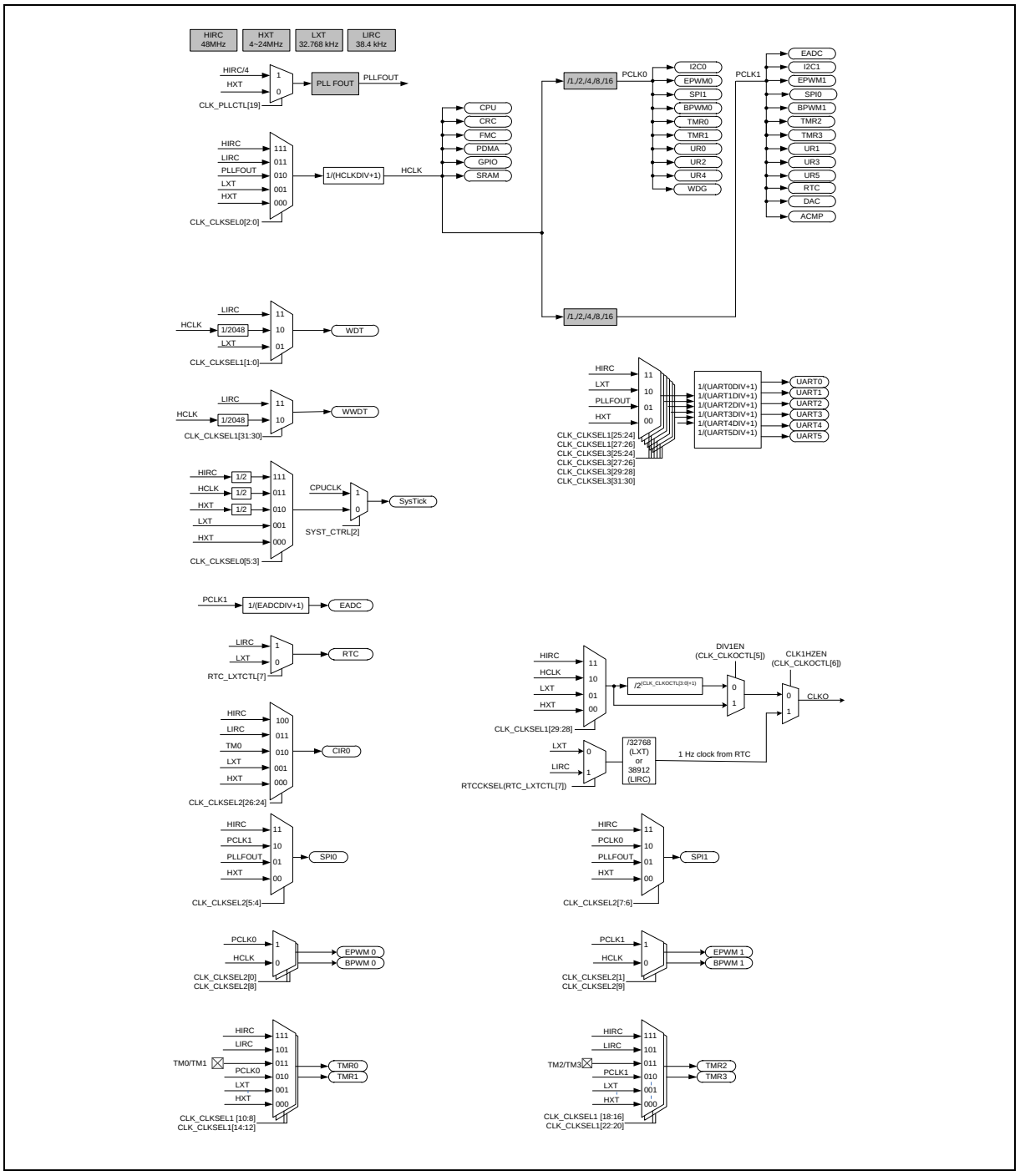


Figure 6.3-1 Clock Generator Global View Diagram

6.3.2 Clock Generator

The clock generator consists of 5 clock sources, which are listed below:

- 32.768 kHz external low speed crystal oscillator (LXT)
- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLLFOUT), PLL source can be selected from

external 4~24 MHz external high speed crystal (HXT) or 48 MHz internal high speed oscillator divided by 4 (HIRC/4)

- 48 MHz internal high speed RC oscillator (HIRC)
- 38.4 kHz internal low speed RC oscillator (LIRC)

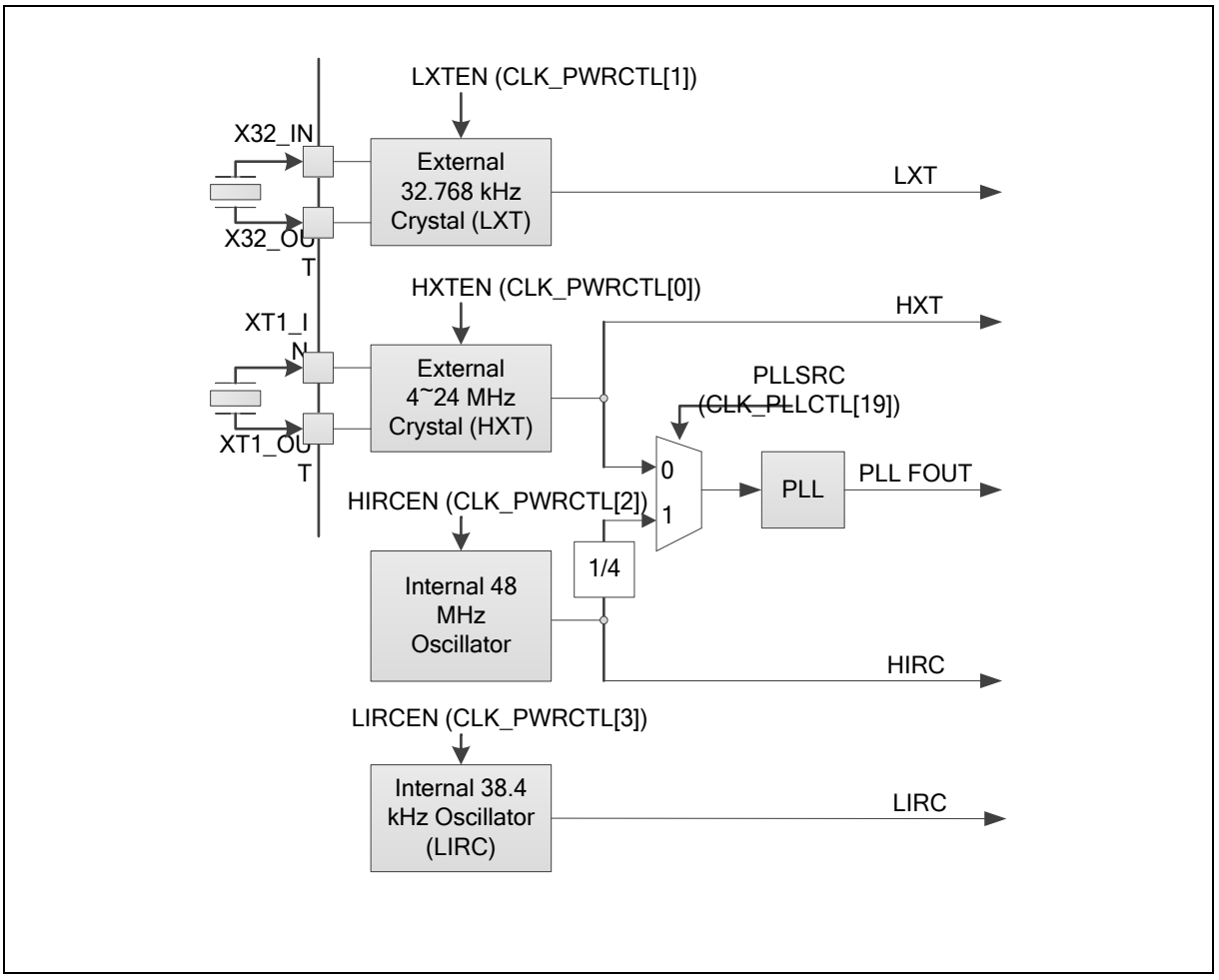


Figure 6.3-2 Clock Generator Block Diagram

6.3.3 System Clock and SysTick Clock

The system clock has 5 clock sources, which were generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0[2:0]). The block diagram is shown in Figure 6.3-3.

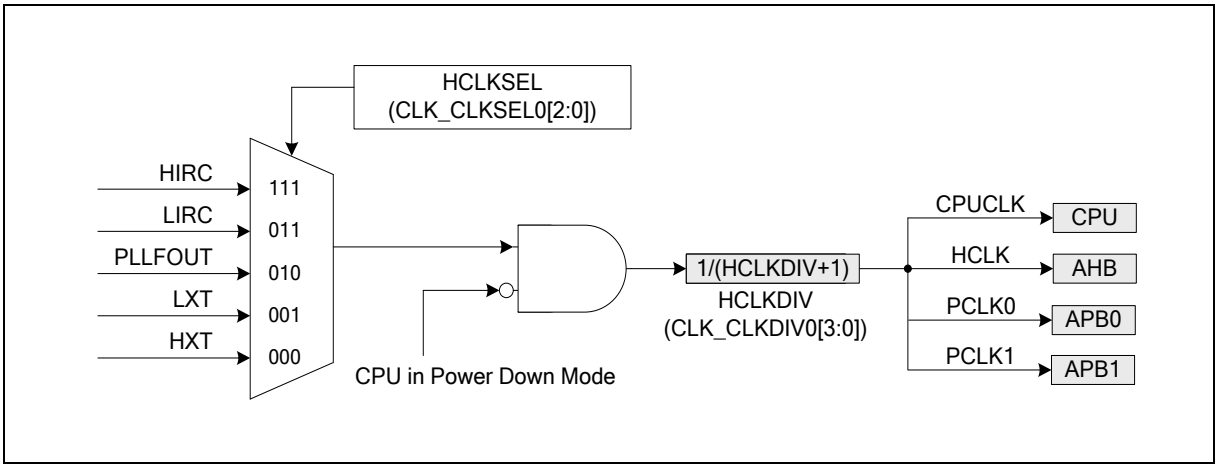


Figure 6.3-3 System Clock Block Diagrams

There are two clock fail detectors to observe HXT and LXT clock source and they have individual enable and interrupt control. When HXT detector is enabled, the HIRC clock is enabled automatically. When LXT detector is enabled, the LIRC clock is enabled automatically.

When HXT clock detector is enabled, the system clock will auto switch to HIRC if HXT clock stop being detected on the following condition: system clock source comes from HXT or system clock source comes from PLL with HXT as the input of PLL. If HXT clock stop condition is detected, the HXTFIF (CLK_CLKDSTS[0]) is set to 1 and chip will enter interrupt if HXTFIEN (CLK_CLKDCTL[5]) is set to 1. User can trying to recover HXT by disable HXT and enable HXT again to check if the clock stable bit is set to 1 or not. If HXT clock stable bit is set to 1, it means HXT is recover to oscillate after re-enable action and user can switch system clock to HXT again.

Figure 6.3-4 shows The HXT clock stops detection and system clock switches to HIRC procedure

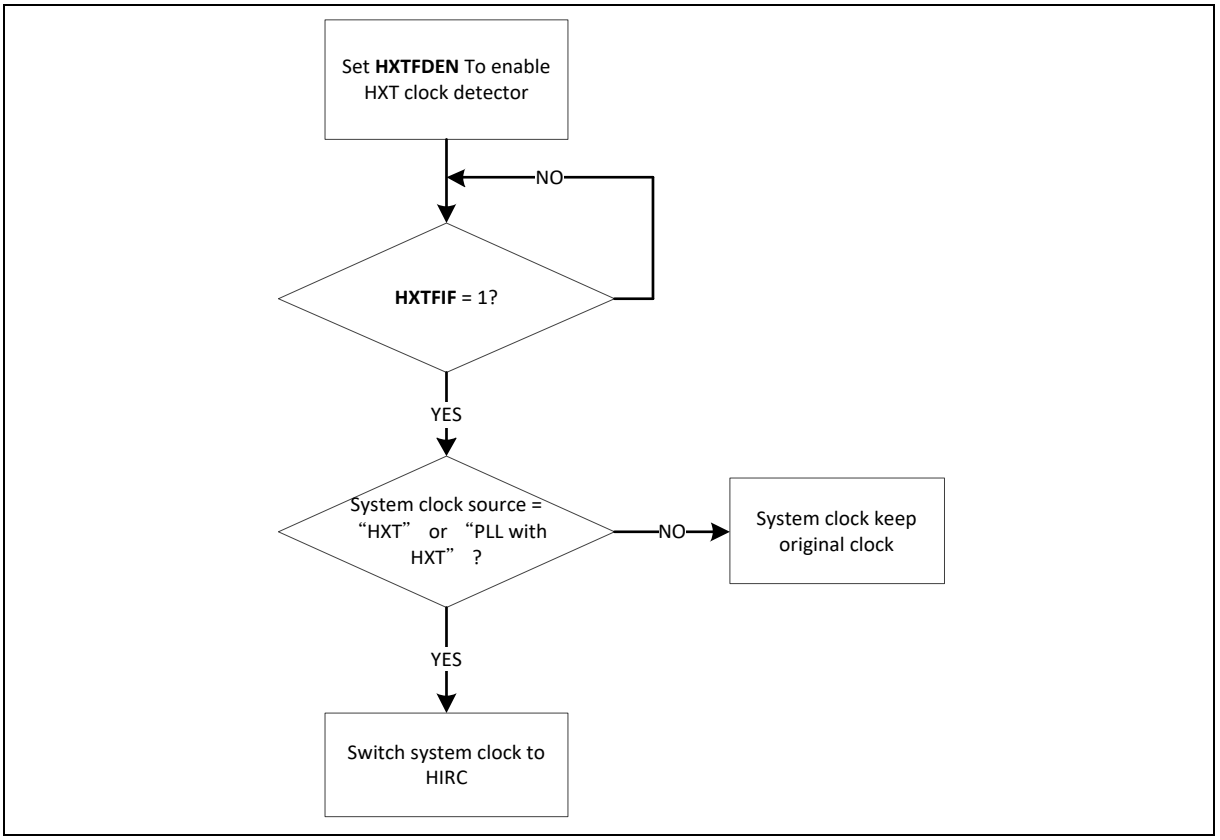


Figure 6.3-4 HXT Stop Protect Procedure

The formula of UPERBD and LOWERBD as below

- HIRC_period * 2048 < HXT_period * UPERBD
- HIRC_period* 2048 > HXT_period* LOWERBD

The clock source of SysTick in Cortex®-M4 core can use CPU clock or external clock (SYST_CTRL[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in Figure 6.3-5.

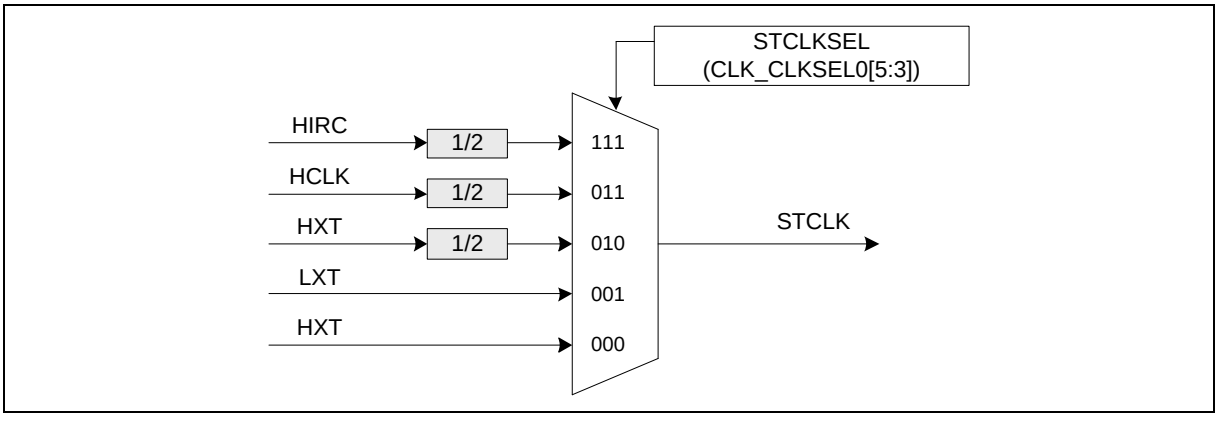


Figure 6.3-5 SysTick Clock Control Block Diagram

6.3.4 Peripherals Clock

Each peripheral clock has its own clock source selection. Refer to the CLK_CLKSEL1, CLK_CLKSEL2 and CLK_CLKSEL3 register.

6.3.5 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

For theses clocks, which still keep active, are listed below:

- Clock Generator
  - 38.4 kHz internal low speed RC oscillator (LIRC) clock
  - 32.768 kHz external low speed crystal oscillator (LXT) clock
- Peripherals Clock (When the modules adopt LXT or LIRC as clock source)

6.3.6 Clock Output

This device is equipped with a power-of-2 frequency divider which is composed of 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]).

When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stays in low state.

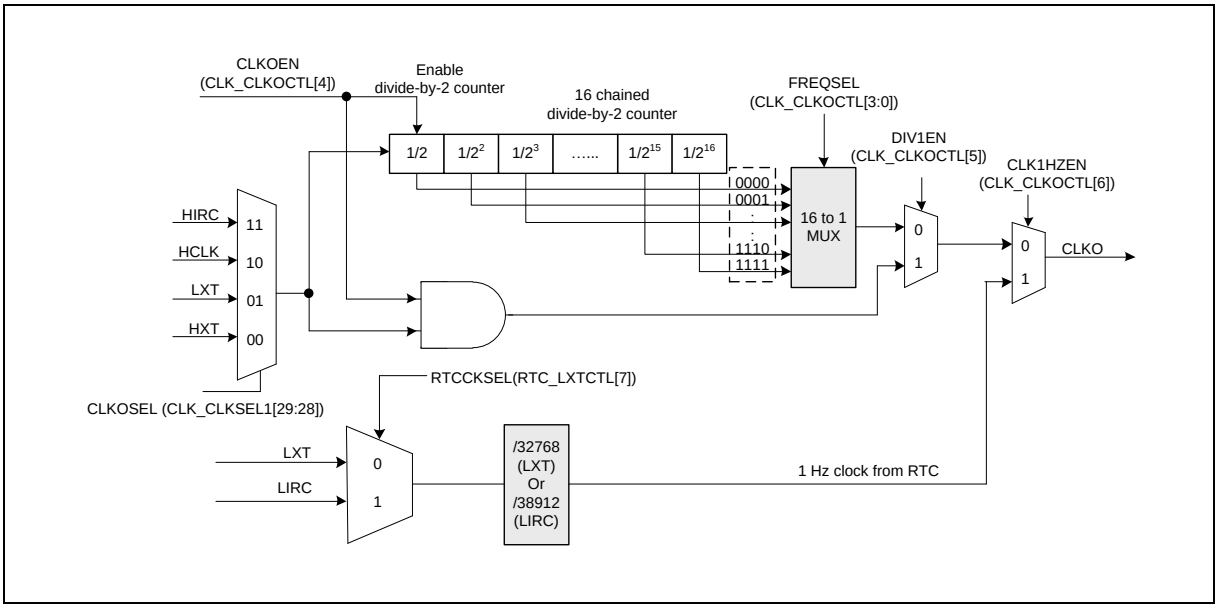


Figure 6.3-6 Clock Output Block Diagram

6.4 Flash Memeory Controller (FMC)

6.4.1 Overview

The FMC is equipped with 256/512 Kbytes on-chip embedded Flash for application and configurable Data Flash to store some application dependent data. Thus, the total size of application rom (APROM) is 256/512 Kbytes. A User Configuration block provides for system initiation. A 4 Kbytes loader ROM (LDROM) is used for In-System-Programming (ISP) function. A 4 Kbytes cache with zero wait cycle is used to improve Flash access performance. This chip also supports In-Application-Programming (IAP) function. User switches the code executing without chip reset after the embedded Flash is updated.

6.4.2 Features

- Supports dual-bank Flash macro for safe firmware upgrade
- Supports 256/512 Kbytes application ROM (APROM)
- Supports 4 Kbytes loader ROM (LDROM)
- Supports 4 XOM (eXecution Only Memory) regions to conceal user program in APROM.
- Supports 16 bytes User Configuration block to control system initiation
- Supports 2 Kbytes page erase for all embedded Flash
- Supports bank erase for APROM, except for XOM regions
- Supports 32-bit/64-bit and multi-word Flash programming function
- Supports fast Flash programming verification function
- Supports CRC32 checksum calculation function
- Supports Flash all one verification function
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded Flash memory
- Supports cache memory to improve Flash access performance and reduce power consumption (4K cache 1 way)

6.5 Data Flash Memory Controller (DFMC)

6.5.1 Overview

The DFMC is equipped with 32 Kbytes on-chip Data Flash to store some application dependent data.

6.5.2 Features

- Supports 32 Kbytes application Data Flash
- Supports 256 bytes page erase for all embedded Flash
- Supports CRC32 checksum calculation function
- Supports Data Flash all one verification function
- Supports In-System-Programming (ISP) to update embedded Data Flash memory

FMC Features	M471
32 KB Data ROM	●
256 B page erase	●
Mass erase for Data Flash.	●
CRC32 checksum calculation function	●
hardware Writer mode and In-Circuit-Programming (ICP)	●
smart entry detection on Writer mode and ICP	●

Table 6.5-1 FMC Features Comparison Table at Different Chip

6.6 General Purpose I/O (GPIO)

6.6.1 Overview

This chip has up to 119 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 119 pins are arranged in 9 ports named as PA, PB, PC, PD, PE, PF, PG, PH and PI. PA, PB, PD, PE and PF has 16 pins on port. PC has 15 pins on port. PG has 10 pins on port. PH has 8 pins on port. PI has 6 pins on port. Each of the 119 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins are depending on CIOINI (CONFIG0[10]).

6.6.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports High Drive and High Slew Rate I/O mode
- Configurable default I/O mode of all pins after reset by CIOINI (CONFIG0[10]) setting
  - CIOINI = 0, all GPIO pins in Quasi-bidirectional mode after chip reset
  - CIOINI = 1, all GPIO pins in input mode after chip reset
- Support independent pull-up control
- Enabling the pin interrupt function will also enable the wake-up function

6.7 PDMA Controller (PDMA)

6.7.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. The PDMA controller has a total of 6 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

6.7.2 Features

- Supports 6 independently configurable channels
- Selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and UART, SPI, EPWM, TIMER, EADC, DAC, ACMP and I^2C request
- Supports Scatter-Gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports time-out function on channel 0 and channel1

6.8 Timer Controller (TMR)

6.8.1 Overview

The timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

The timer controller also provides four PWM generators. Each PWM generator supports one PWM output and two selectable PWM output channels (TMx or TMx_EXT). The output state of PWM output pin can be control by polarity control, output enable control and output channel select.

6.8.2 Features

6.8.2.1 Timer Function Features

- Four sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin (TMx_EXT) event for interval measurement
- Supports external capture pin (TMx_EXT) event to reset 24-bit up counter
- Supports internal clock (HIRC, LIRC) and external clock (HXT, LXT) for capture event
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger BPWM, EPWM, EADC, DAC and PDMA function
- Supports internal capture triggered while internal ACMP output signal transition
- Supports Inter-Timer trigger mode

6.8.2.2 PWM Function Features

- Supports PWM generator with two selectable output channels
- Supports 16-bit PWM counter
  - Up count operation type
  - One-shot or auto-reload counter operation mode
- Supports 8-bit prescale from 1 to 256
- Supports 16-bit compare register and period register and double buffer for period register and compare register
- Supports tri-state enable and polarity control for each PWM selectable output channels
- Supports interrupt on the following events:
  - PWM period point, up-count compared point events
- Supports wake-up when interrupt occurs when clock source is LXT or LIRC

- PWM can generator output in Power-down mode
- Supports trigger EADC, PDMA, and DAC on the following events:
  - PWM period point and up-count compared point events

6.9 Watchdog Timer (WDT)

6.9.1 Overview

The Watchdog Timer (WDT) is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake up system from Idle/Power-down mode.

6.9.2 Features

- 20-bit free running up counter for WDT time-out interval
- Selectable time-out interval (2^4 ~ 2^{20}) and the time-out interval is 0.416 ms ~ 27.306 s if WDT_CLK = 38.4 kHz.
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026、130、18 or 3 WDT_CLK reset delay period
- Supports to force WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as 38.4 kHz or LXT.

6.10 Window Watchdog Timer (WWDT)

6.10.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software running to uncontrollable status by any unpredictable condition.

6.10.2 Features

- 6-bit down counter value (CNTDAT, WWDT_CNT[5:0]) and 6-bit compare value (CMPDAT, WWDT_CTL[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value (PSCSEL, WWDT_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode

6.11 Real Time Clock (RTC)

6.11.1 Overview

The Real Time Clock (RTC) controller provides the real time and calendar message. The RTC offers programmable time tick and alarm match interrupts. The data format of time and calendar messages are expressed in BCD format. A digital frequency compensation feature is available to compensate external crystal oscillator frequency accuracy.

6.11.2 Features

- Supports real time counter in RTC_TIME (hour, minute, second) and calendar counter in RTC_CAL (year, month, day) for RTC time and calendar check.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) settings in RTC_TALM and RTC_CALM.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) mask enable in RTC_TAMSK and RTC_CAMSK.
- Selectable 12-hour or 24-hour time scale in RTC_CLKFMT register.
- Supports Leap Year indication in RTC_LEAPYEAR register.
- Supports Day of the Week counter in RTC_WEEKDAY register.
- Frequency of RTC clock source compensate by RTC_FREQADJ register.
- All time and calendar message expressed in BCD format.
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second.
- Supports RTC Time Tick and Alarm Match interrupt.
- Supports 1 Hz clock output.
- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated.
- Supports Daylight Saving Time software control in RTC_DSTCTL.

6.12 EPWM Generator and Capture Timer (EPWM)

6.12.1 Overview

The chip provides two EPWM generators — EPWM0 and EPWM1. Each EPWM supports 6 channels of EPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit EPWM counter with 16-bit comparator. The EPWM counter supports up, down and up-down counter types. EPWM uses comparator compared with counter to generate events. These events use to generate EPWM pulse, interrupt and trigger signal for EADC/DAC to start conversion.

The EPWM generator supports two standard EPWM output modes: Independent mode and Complementary mode, they have difference architecture. There are two output functions based on standard output modes: Group function and Synchronous function. Group function can be enabled under Independent mode or complementary mode. Synchronous function only enabled under complementary mode. Complementary mode has two comparators to generate various EPWM pulse with 12-bit dead-time generator and another free trigger comparator to generate trigger signal for EADC. For EPWM output control unit, it supports polarity output, independent pin mask and brake functions.

The EPWM generator also supports input capture function. It supports latch EPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened. Capture function also support PDMA to transfer captured data to memory.

6.12.2 Features

6.12.2.1 EPWM Function Features

- Supports maximum clock frequency up to maximum PLL frequency
- Supports up to two EPWM modules, each module provides 6 output channels
- Supports independent mode for EPWM output/Capture input channel
- Supports complementary mode for 3 complementary paired EPWM output channel
  - Dead-time insertion independent control with 12-bit resolution
  - Synchronous function for phase control
  - Two compared values during one period
- Supports 12-bit prescaler from 1 to 4096
- Supports 16-bit resolution EPWM counter
  - Up, down and up/down counter operation type
- Supports one-shot or auto-reload counter operation mode
- Supports group function
- Supports synchronous function
- Supports mask function and tri-state enable for each EPWM pin
- Supports brake function
  - Brake source from pin, analog comparator and system safety events (clock failed, SRAM parity error, Brown-out detection and CPU lockup).
  - Noise filter for brake source from pin
  - Leading edge blanking (LEB) function for brake source from analog comparator
  - Edge detect brake source to control brake state until brake interrupt cleared
  - Level detect brake source to auto recover function after brake condition removed

- Supports interrupt on the following events:
  - EPWM counter matches 0, period value or compared value
  - Brake condition happened
- Supports trigger EADC/DAC on the following events:
  - EPWM counter matches 0, period value or compared value
  - EPWM counter match free trigger comparator compared value (only for EADC)
  - Support EPWM trigger EADC event prescaler feature
- Supports PDMA transfer for Interrupt Flag Accumulator function
- Supports EPWM output accumulator stop counter mode
- Supports Fault Detect Function.
- Supports External Pin Trigger function

6.12.2.2 Capture Function Features

- Supports 3-bit capture input noise filter
- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option
- Supports PDMA transfer function for EPWM all channels

6.13 Basic PWM Generator and Capture Timer (BPWM)

6.13.1 Overview

The chip provides two BPWM generators — BPWM0 and BPWM1. Each BPWM supports 6 channels of BPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit BPWM counter with 16-bit comparator. The BPWM counter supports up, down and up-down counter types, all 6 channels share one counter. BPWM uses the comparator compared with counter to generate events. These events are used to generate BPWM pulse, interrupt and trigger signal for EADC0 to start conversion. For BPWM output control unit, it supports polarity output, independent pin mask and tri-state output enable.

The BPWM generator also supports input capture function to latch BPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened.

6.13.2 Features

6.13.2.1 BPWM Function Features

- Supports maximum clock frequency up to maximum PLL frequency.
- Supports up to two BPWM modules; each module provides 6 output channels
- Supports independent mode for BPWM output/Capture input channel
- Supports 12-bit prescalar from 1 to 4096
- Supports 16-bit resolution BPWM counter; each module provides 1 BPWM counter
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each BPWM pin
- Supports interrupt in the following events:
  - BPWM counter matches 0, period value or compared value
- Supports trigger EADC0 in the following events:
  - BPWM counter matches 0, period value or compared value

6.13.2.2 Capture Function Features

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

	M471
Trigger numbers for EADC	1

Table 6.13-1 BPWM Features Comparison Table

6.14 UART Interface Controller (UART)

6.14.1 Overview

The chip provides six channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs serial-to-parallel conversion on data received from the peripheral and parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports eleven types of interrupts. The UART controller supports flow control function. The UART controller also supports IrDA SIR, LIN, RS-485 and Single-wire function modes and auto-baud rate measuring function.

6.14.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16 bytes or 1/1 byte entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next START bit by setting DLY (UART_TOUT[15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
  - 9600 bps for UART_CLK is selected LXT.
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable PARITY bit, even, odd, no parity or stick PARITY bit generation and detection
  - Programmable STOP bit, 1, 1.5, or 2 STOP bit generation
- Supports IrDA SIR function mode
  - 3/16 bit duration for normal mode
- Supports LIN function mode (Only UART0/UART1 with LIN function)
  - LIN master/slave mode
  - Programmable break generation function for transmitter
  - Break detection function for receiver
- Supports RS-485 function mode
  - RS-485 9-bit mode
  - Hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Supports PDMA transfer function
- Supports Single-wire function mode

- Supports baud rate compensation function

UART Feature	UART0/ UART1	UART2 ~ UART5
FIFO	16 Bytes	1 Bytes
Auto Flow Control (CTS/RTS)	√	√
IrDA	√	√
LIN	√	-
RS-485 Function Mode	√	√
nCTS Wake-up	√	√
Incoming Data Wake-up	√	√
Received Data FIFO reached threshold Wake-up	√	-
RS-485 Address Match (AAD mode) Wake-up	√	-
Auto-Baud Rate Measurement	√	√
STOP bit Length	1, 1.5, 2 bit	1, 1.5, 2 bit
Word Length	5, 6, 7, 8 bits	5, 6, 7, 8 bits
Even / Odd Parity	√	√
Stick Bit	√	√
Baud Rate Compensation	√	-

Table 6.14-1 M471V/M471K series UART Features

6.15 Serial Peripheral Interface (SPI)

6.15.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains up to two sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each SPI controller can be configured as a master or a slave device and supports the PDMA function to access the data buffer. Each SPI controller also supports I^2S mode to connect external audio CODEC.

6.15.2 Features

- SPI Mode
  - Up to two sets of SPI controllers
  - Supports Master or Slave mode operation
  - Master mode up to 24 MHz
  - Slave mode up to 24 MHz when SPI master device supports adjustment function of RX data sampling clock
  - Slave mode up to 18 MHz when SPI master device does not support adjustment function of RX data sampling clock
  - Configurable bit length of a transaction word from 4 to 32-bit
  - Provides separate 4-level of 32-bit (or 8-level of 16-bit) transmit and receive FIFO buffers which depends on SPI setting of data width
  - Supports MSB first or LSB first transfer sequence
  - Supports Byte Reorder function
  - Supports Byte or Word Suspend mode
  - Supports PDMA transfer
  - Supports 3-Wire, no slave selection signal, bi-direction interface
  - Supports one data channel half-duplex transfer
  - Supports receive-only mode
- I^2S Mode
  - Supports Master or Slave
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Each provides two 4-level FIFO data buffers, one for transmitting and the other for receiving
  - Supports monaural and stereo audio data
  - Supports PCM mode A, PCM mode B, I^2S and MSB justified data format
  - Supports two PDMA requests, one for transmitting and the other for receiving

6.16 I²C Serial Interface Controller (I²C)

6.16.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are two sets of I²C controllers which support Power-down wake-up function.

6.16.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports up to two I²C ports
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflow
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing and 10-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Supports PDMA with one buffer capability
- Supports setup/hold time programmable
- Supports Bus Management (SM/PM compatible) function

6.17 Customize IR Receiver (CIR)

6.17.1 Overview

The CIR controller supports to receive data from the output pin of IR receiver. The received data will be stored in registers and wait for further analysis.

6.17.2 Features

- Supports one channel CIR control signal receiver.
- Supports 5 clock sources with 3-bit prescale for vary bit rate sampling.
- Supports a digital filter to be used to filter out noise.
- Supports observeing the noise filter output signal.
- Supports input signal inversion.
- Supports two 32-bit data registers and receive buffer full flag.
- Supports Header, Data0, Data1, End and Special patterns.
- Supports to receive data in Power-down mode and be woken up by specified first 8 bits data pattern. (User needs to switch clock source to LIRC before entering Power-down mode.)
- Offers 11 different kinds of interrupt options and flags.
- Supports receive error detection.
- Supports three receive formats for the CIR control signal waveform.
- Clock PCLK frequency must be faster than CIR internal clock CIR0_CLK frequency.

6.18 CRC Controller (CRC)

6.18.1 Overview

The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32 settings.

6.18.2 Features

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-8: $X^8 + X^2 + X + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Programmable seed value
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1's complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports using PDMA to write data to perform CRC operation

6.19 Pseudo Random Number Generator (PRNG)

6.19.1 Overview

The PRNG core supports 64, 128, 192 and 256 bits random number generation.

6.19.2 Features

- PRNG
  - Supports 64, 128, 192 and 256 bits random number generation

6.20 Enhanced 12-bit Analog-to-Digital Converter (EADC)

6.20.1 Overview

The chip contains one 12-bit successive approximation analog-to-digital converter (SAR EADC converter) with 24 external input channels and 3 internal channels. The EADC converter can be started by software trigger, EPWM0/1 triggers, BPWM0/1 triggers, timer0~3 overflow pulse triggers, ADINT0 interrupt EOC (End of conversion) and ADINT1 interrupt EOC pulse trigger and external pin (EADC0_ST) input signal.

6.20.2 Features

- Analog input voltage range: 0~ V_{REF} (Max to 5.5V)
- Reference voltage from V_{REF} pin or AV_{DD}
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 24 single-end analog external input channels or 1 pair differential analog input channels
- Up to 3 internal channels, they are band-gap voltage (V_{BG}), temperature sensor (V_{TEMP}) , and DAC0 output
- Four EADC interrupts (ADINT0~3) with individual interrupt vector addresses for EADC
- Maximum EADC clock frequency is 36 MHz for EADC
- Up to 1.895 MSPS conversion rate for EADC
- Supports calibration function and calibration interrupt
- Supports internal reference voltage V_{REF}: 2.048V, 2.56V, 3.072V, and 4.096V.
- Supports power-down mode and ultra low frequency mode
- Up to 27 sample modules
  - Sample modules0~23 is configurable for EADC converter channel (EADC_CH0~23) and trigger source for each EADC
  - Sample module 24~26 is fixed for channel 24, 25, 26 input sources as band-gap voltage, temperature sensor, and DAC output
  - Double buffer for sample control logic module 0~3
  - Configurable sampling time for each sample module
  - Conversion results are held in 27 data registers with valid and overrun indicators.
- Averaging (2^n times, n=0~8) to support up to 12-bit result and over-sampling, or called Accumulation, (2^n times, n=0~8) to support up to 16-bit result
- Any EADC conversion of each EADC can be started by:
  - Write 1 to SWTRGn (EADC_SWTRG[n], n = 0~26)
  - External pin EADC0_ST
  - Timer0~3 overflow pulse triggers
  - ADINT0 and ADINT1 interrupt EOC (End of conversion) pulse triggers
  - EPWM/BPWM triggers
- Supports PDMA transfer
- Conversion Result Monitor by Compare Mode

6.21 Digital to Analog Converter (DAC)

6.21.1 Overview

The DAC module is a 8-bit, voltage output digital-to-analog converter. It can be configured to used in conjunction with the PDMA controller. The DAC integrates a voltage output buffer that can be used to reduce output impendence and drive external loads directly without having to add an external operational amplifier.

6.21.2 Features

- Analog output voltage range: 0~AV_{DD}.
- Supports 8-bit output mode.
- Rail to rail settle time 5us.
- Supports up to one 8-bit 200 KSPS voltage type DAC without buffer.
- Reference voltage from internal reference voltage (INT_VREF), V_{REF} pin.
- Supports software and hardware trigger, including Timer0~3, EPWM0, EPWM1, and external trigger pin to start DAC conversion.
- Supports PDMA mode.

6.22 Analog Comparator Controller (ACMP)

6.22.1 Overview

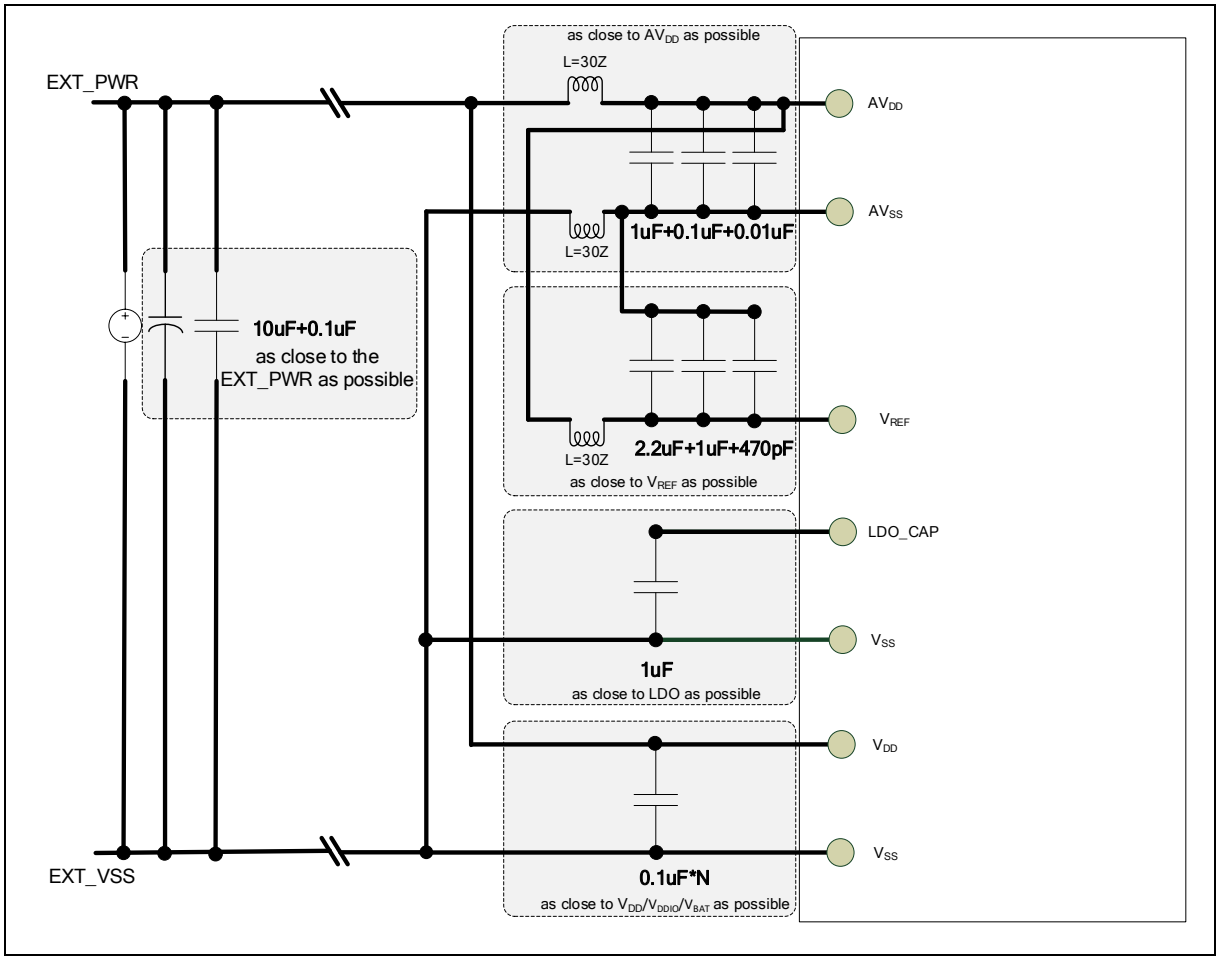
The chip provides two comparators. The comparator output is logic 1 when positive input is greater than negative input; otherwise, the output is 0. Each comparator can be configured to generate an interrupt when the comparator output value changes.

6.22.2 Features

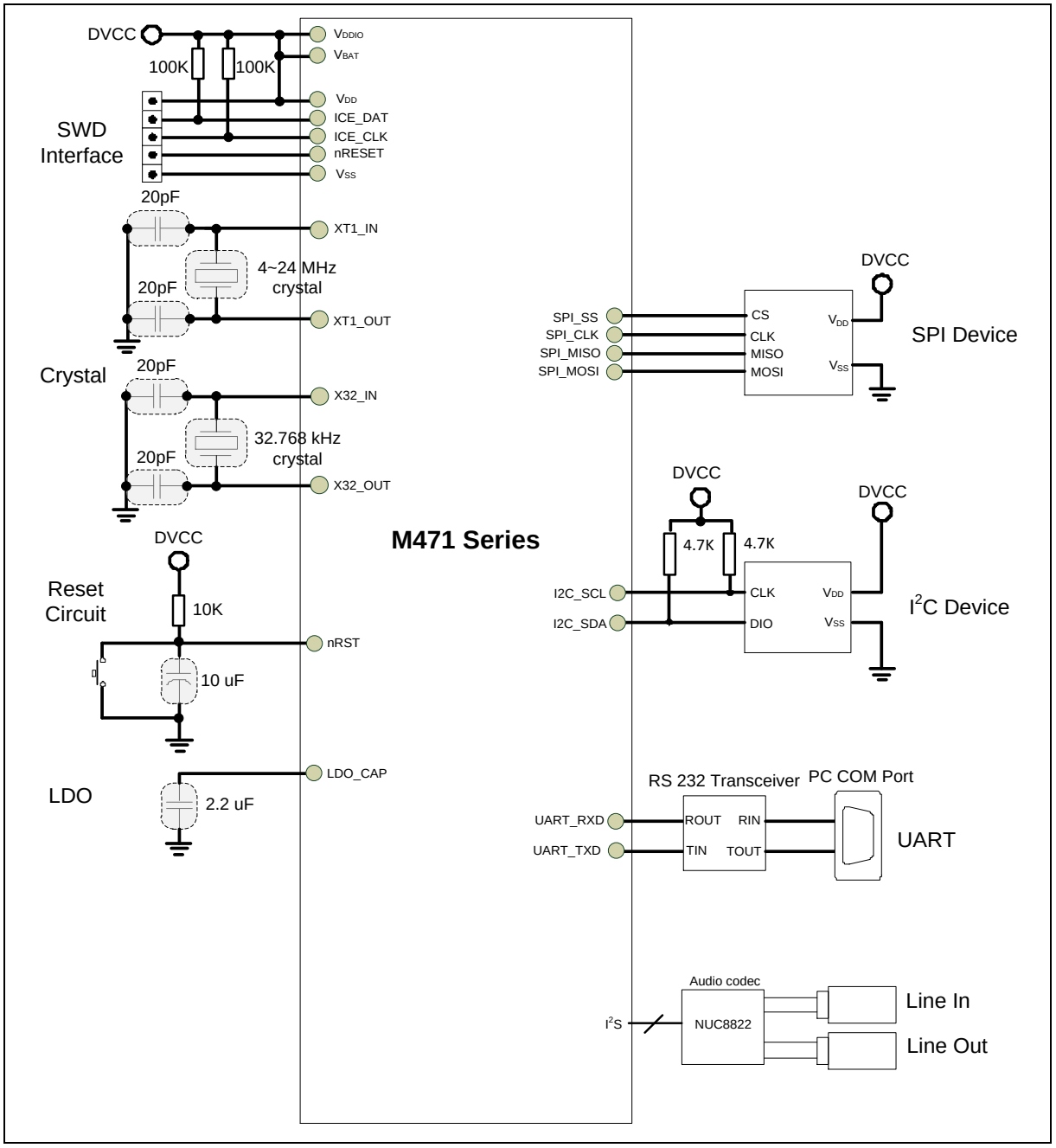
- Analog input voltage range: 0 ~ AV_{DD} (voltage of AV_{DD} pin)
- Up to two rail-to-rail analog comparators
- Supports hysteresis function
  - Supports programmable hysteresis window: 0mV, 10mV, 20mV, 30mV, 40mV, 50mV
- Supports wake-up function
- Selectable input sources of positive input and negative input
- ACMP0 supports:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP0_P0, ACMP0_P1, ACMP0_P2, or ACMP0_P3
  - 4 negative sources:
    - ACMP0_N
    - Supports Comparator Reference Voltage (CRV)
    - Internal band-gap voltage (VBG)
    - DAC0 output (DAC0_OUT)
- ACMP1 supports:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP1_P0, ACMP1_P1, ACMP1_P2, or ACMP1_P3
  - 4 negative sources:
    - ACMP1_N
    - Supports Comparator Reference Voltage (CRV)
    - Internal band-gap voltage (VBG)
    - DAC0 output (DAC0_OUT)
- Shares one ACMP interrupt vector for all comparators
- Interrupts generated when compare results change (Interrupt event condition is programmable)
- Supports triggers for break events and cycle-by-cycle control for EPWM
- Supports window compare mode and window latch mode
- Supports offset calibration

7 APPLICATION CIRCUIT

7.1 Power Supply Scheme



7.2 Peripheral Application Scheme



8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Stresses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

8.1.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}[*1]	DC power supply	-0.3	6.5	V
ΔV_{DD}	Variations between different V_{DD} power pins	-	50	mV
$\|V_{DD} - AV_{DD}\|$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
ΔV_{SS}	Variations between different ground pins	-	50	mV
$\|V_{SS} - AV_{SS}\|$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV
V_{IN}	Input voltage on any other pin[*2]	V_{SS}-0.3	6.5	V

Notes:

1. All main power (V_{DD}, AV_{DD}) and ground (V_{SS}, AV_{SS}) pins must be connected to the external power supply.
2. Refer to Table 8.1-2 for the values of the maximum allowed injected current

Table 8.1-1 Voltage Characteristics

8.1.2 Current Characteristics

Symbol	Description	Min	Max	Unit
ΣI_{DD} [*1]	Maximum current into V_{DD}	-	200	mA
ΣI_{SS}	Maximum current out of V_{SS}	-	100	
I_{IO}	Maximum current sunk by a I/O Pin	-	20	
	Maximum current sourced by a I/O Pin	-	20	
	Maximum current sunk by total I/O Pins [*2]	-	100	
	Maximum current sourced by total I/O Pins [*2]	-	100	
$I_{INJ(PIN)}$ [*3]	Maximum injected current by a I/O Pin	-	±5	
$\Sigma I_{INJ(PIN)}$ [*3]	Maximum injected current by total I/O Pins	-	±25	

Note:

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by $V_{IN}>AV_{DD}$ and a negative injection is caused by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 8.1-2 Current Characteristics

8.1.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA})$

- T_A = ambient temperature (℃)
- θ_{JA} = thermal resistance junction-ambient (℃/Watt)
- P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	105	℃
T_J	Operating junction temperature	-40	-	125	
T_{ST}	Storage temperature	-65	-	150	
θ_{JA}[*1]	Thermal resistance junction-ambient 64-pin LQFP(7x7 mm)	-	58	-	℃/Watt
	Thermal resistance junction-ambient 100-pin LQFP(14x14 mm)	-	46	-	℃/Watt
	Thermal resistance junction-ambient 128-pin LQFP(14x14 mm)	-	38.5	-	℃/Watt

Note:

1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions

Table 8.1-3 Thermal Characteristics

8.1.4 EMC Characteristics

8.1.4.1 Electrostatic discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

8.1.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latchup

performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

8.1.4.3 Electrical fast transients (EFT)

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system..

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International ElectrotechnicalCommission (IEC).

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[*1]	Electrostatic discharge,human body mode	-8K	-	8K	V
V_{CDM}[*2]	Electrostatic discharge,charge device model	-1K	-	1K	
V_{MM}[*]	Electrostatic discharge,machine model	-400	-	400	
LU[*3]	Pin current for latch-up[*3]	-350	-	350	mA
V_{EFT}[*4] [*5]	Fast transient voltage burst	-4.4	-	+4.4	kV

Notes:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test.
5. The performace cretia class is 4A.

Table 8.1-4 EMC Characteristics

8.1.5 Package Moisture Sensitivity (MSL)

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing.

Pacakge	MSL
64-pin LQFP(7x7 mm) [*1]	MSL 3
100-pin LQFP(14x14 mm) [*1]	MSL 3
128-pin LQFP(14x14 mm) [*1]	MSL 3

Note:

1. Determined according to IPC/JEDEC J-STD-020

Table 8.1-5 Package Moisture Sensitivity (MSL)

8.1.6 Soldering Profile

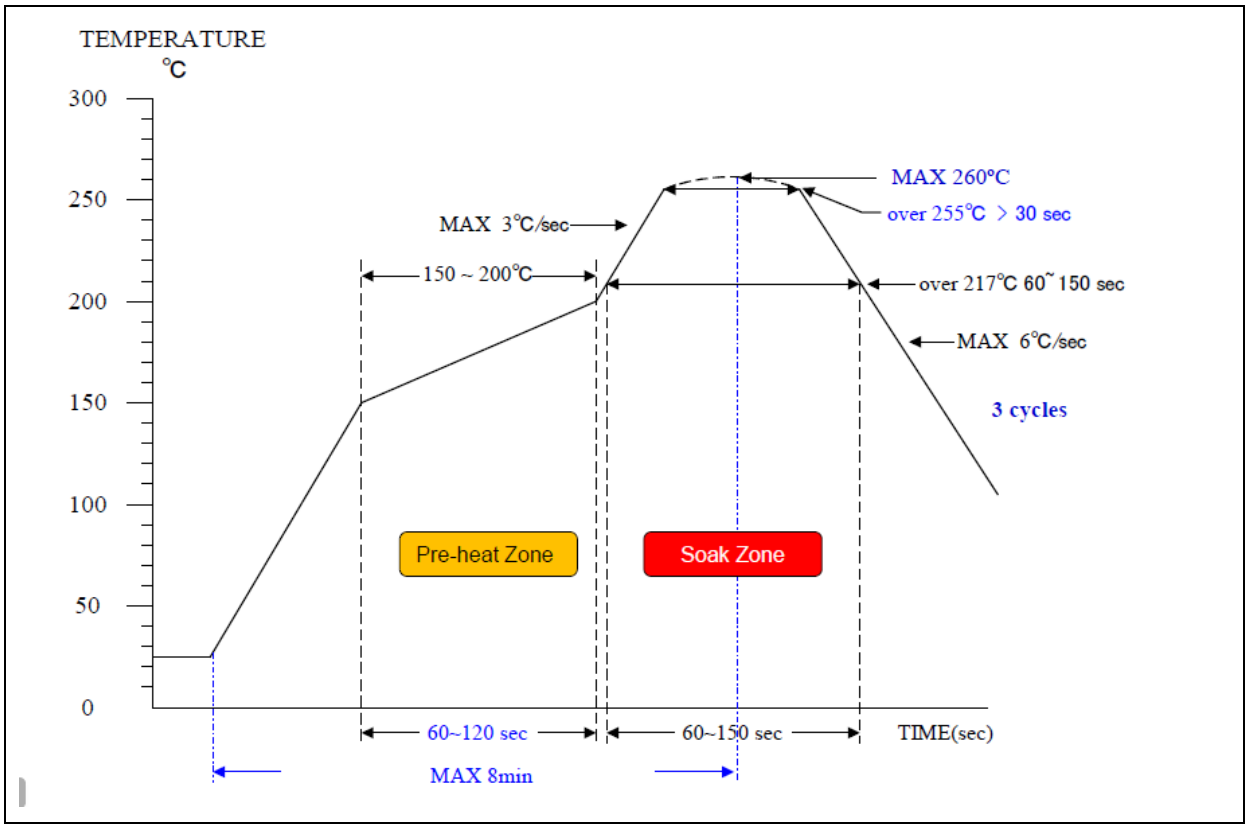


Figure 8.1-1 Soldering profile from J-STD-020C

Porfile Feature	Pb Free Package
Average ramp-up rate (217℃ to peak)	3℃/sec. max
Preheat temperature 150℃ ~200℃	60 sec. to 120 sec.
Temperature maintained above 217℃	60 sec. to 150 sec.
Time with 5℃ of actual peak temperature	> 30 sec.
Peak temperature range	260℃
Ramp-down rate	6℃/sec ax.
Time 25℃ to peak temperature	8 min. max
Note: 1. Determined according to J-STD-020C	

Table 8.1-6 Soldering Profile

8.2 General Operating Conditions

(V_{DD}-V_{SS} = 2.5 ~ 5.5V, T_A = 25°C, HCLK = 48 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
f_{HCLK}	Internal AHB clock frequency	-	-	120	MHz	
V_{DD}	Operation voltage	2.5	-	5.5	V	
AV_{DD}[*1]	Analog operation voltage	V_{DD}				
V_{REF}	Analog reference voltage	2.5	-	AV_{DD}		
V_{LDO}	LDO output voltage	-	1.8	-		
V_{BG}	Band-gap voltage	1.18	1.21	1.245	V	
T_{VBG_ADC}[*3]	ADC sampling time when reading the band-gap voltage	10	-	-	µS	
C_{LDO}[*2]	LDO output capacitor on each pin	1			µF	
R_{ESR}[*3]	ESR of C_{LDO} output capacitor	-	-	0.5	Ω	
I_{RUSH}[*3]	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	100	400	mA	
E_{RUSH}[*3]	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	-	1.8	-	µC	V_{DD} = 1.8 V, T_A = 105 °C, I_{RUSH} = 90 mA for 80µs

Note:

1. It is recommended to power V_{DD} and AV_{DD} from the same source. A maximum difference of 0.3 V between V_{DD} and AV_{DD} can be tolerated during power-on and power-off operation .
2. To ensure stability, an external 1 µF output capacitor, C_{LDO} must be connected between the LDO_CAP pin and the closest GND pin of the device. Solid tantalum and multilayer ceramic capacitors are suitable as output capacitor. Additional 100 nF bypass capacitor between LDO_CAP pin and the closest GND pin of the device helps decrease output noise and improves the load transient response.
3. Guaranteed by design, not tested in production

Table 8.2-1 General operating conditions

8.3 DC Electrical Characteristics

8.3.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for V_{DD} = 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 2.5 ~ 5.5 V unless otherwise specified.
- $V_{DD} = AV_{DD}$
- When the peripherals are enabled HCLK is the system clock, $f_{PCLK0, 1} = f_{HCLK}$.
- Program run CoreMark® code in Flash.

Symbol	Conditions	F_{HCLK}	Typ [*1]	Max[*1][*2]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_RUN}	Normal run mode with PL0 (PLSEL = 00), executed from Flash, all peripherals disable HCLK is set as PLL clock ($f_{PCLK0, 1}$ = 1/2 f_{HCLK}.)	120 MHz	43.93	51.25	52.50	53.80	mA
	Normal run mode with PL1 (PLSEL = 01), executed from Flash, all peripherals disable HCLK is set as PLL clock	100 MHz	35.37	39.06	40.40	41.75	
		96 MHz	35.02	38.66	40.05	41.40	
		72 MHz	26.82	30.47	31.72	32.98	
		60 MHz	22.72	26.38	27.54	28.78	
	Normal run mode with PL1 (PLSEL = 01), executed from Flash, all peripherals disable HCLK is set as HIRC, HXT clock	48 MHz	16.23	16.82	17.67	18.74	
		24 MHz	8.68	9.01	9.84	10.87	
		12 MHz	4.85	5.06	5.86	6.89	
		4 MHz	2.30	2.41	3.22	4.22	
		24 MHz	9.41	13.05	14.02	15.15	
		12 MHz	5.64	9.27	10.18	11.27	
		4 MHz	3.10	6.75	7.60	8.67	
	Normal run mode with PL1 (PLSEL = 01), executed from Flash, all peripherals disable HCLK is set as LIRC or LXT clock	38.4 kHz	0.106	0.147	0.930	1.923	
		32 kHz	0.103	0.150	0.934	1.937	
	Normal run mode with PL0 (PLSEL = 00), executed from Flash, all peripherals enable HCLK is set as PLL clock	120 MHz	63.63	72.69	74.42	76.14	
	Normal run mode with PL1	100 MHz	58.82	62.99	64.98	66.59	

	(PLSEL = 01), executed from Flash, all peripherals enable HCLK is set as PLL clock	96 MHz	57.57	61.66	63.67	65.30	
		72 MHz	43.86	47.86	49.59	51.08	
		60 MHz	36.99	40.94	42.53	43.95	
	Normal run mode with PL1 (PLSEL = 01), executed from Flash, all peripherals enable HCLK is set as HIRC, HXT clock	48 MHz	25.82	26.94	27.96	29.09	
		24 MHz	16.30	17.04	18.01	19.09	
		12 MHz	10.15	10.65	11.54	12.60	
		4 MHz	6.05	6.37	7.24	8.26	
		24 MHz	15.19	18.93	20.10	21.30	
		12 MHz	9.09	12.79	13.80	14.96	
		4 MHz	5.01	8.70	9.60	10.70	
	Normal run mode with PL1 (PLSEL = 01), executed from Flash, all peripherals enable HCLK is set as LIRC or LXT clock	38.4 kHz	0.113	0.151	0.936	1.930	
		32 kHz	0.111	0.158	0.944	1.943	

Notes:

1. When analog peripheral blocks such as DAC, ADC, ACMP, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-1 Current consumption in Normal Run mode

Symbol	Conditions	F_{HCLK}	Typ [*1]	Max[*1][*2]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_IDLE}	Idle run mode with PL0 (PLSEL = 00), executed from Flash, all peripherals disable HCLK is set as PLL clock ($f_{PCLK0, 1}$ = 1/2 f_{HCLK}.)	120 MHz	11.46	16.37	17.35	18.53	mA
	Idle run mode with PL1 (PLSEL = 01), executed from Flash, all peripherals disable HCLK is set as PLL clock	100 MHz	9.67	13.44	14.40	15.52	
		96 MHz	10.34	14.05	15.07	16.21	
		72 MHz	8.26	11.97	12.91	14.02	
		60 MHz	7.23	10.93	11.84	12.95	
	Idle run mode with PL1 (PLSEL = 01), executed from Flash, all peripherals disable HCLK is set as HIRC, HXT clock	48 MHz	3.77	3.97	4.79	5.81	
		24 MHz	2.43	2.57	3.38	4.39	
		12 MHz	1.73	1.84	2.64	3.64	
		4 MHz	1.26	1.35	2.13	3.14	
		24 MHz	3.20	6.87	7.71	8.78	
		12 MHz	2.53	6.19	7.03	8.10	
		4 MHz	2.07	5.72	6.55	7.60	
	Idle run mode with PL1 (PLSEL = 01), executed from	38.4 kHz	0.096	0.140	0.922	1.915	

	Flash, all peripherals disable HCLK is set as LIRC or LXT clock	32 kHz	0.095	0.141	0.924	1.923	
	Idle run mode with PL0 (PLSEL = 00), executed from Flash, all peripherals enable HCLK is set as PLL clock	120 MHz	32.72	40.27	41.68	43.05	
	Idle run mode with PL1 (PLSEL = 01), executed from Flash, all peripherals enable HCLK is set as PLL clock	100 MHz	34.40	38.64	40.34	41.79	
		96 MHz	34.10	38.25	39.99	41.46	
		72 MHz	26.16	30.20	31.70	33.06	
		60 MHz	22.20	26.18	27.56	28.87	
	Idle run mode with PL1 (PLSEL = 01), executed from Flash, all peripherals enable HCLK is set as HIRC, HXT clock	48 MHz	13.80	14.54	15.55	16.66	
		24 MHz	10.23	10.77	11.71	12.80	
		12 MHz	7.07	7.46	8.35	9.41	
		4 MHz	4.97	5.25	6.10	7.14	
		24 MHz	9.22	12.98	14.04	15.21	
		12 MHz	6.12	9.83	10.80	11.92	
		4 MHz	4.03	7.70	8.61	9.69	
	Idle run mode with PL1 (PLSEL = 01), executed from Flash, all peripherals enable HCLK is set as LIRC or LXT clock	38.4 kHz	0.104	0.144	0.927	1.93	
		32 kHz	0.103	0.150	0.933	1.941	

Notes:

1. When analog peripheral blocks such as DAC, ADC, ACMP, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-2 Current consumption in Idle mode

Symbol	Test Conditions	LIRC 38.4 kHz	LXT[*1] 32.768 kHz	Typ[*2] T_A = 25 °C	Max[*3][*4] T_A = 25 °C	Max[*3][*4] T_A = 85 °C	Max[*3][*4] T_A = 105 °C	Unit
I_{DD_PD}	Power-down mode, all peripherals disable	-	-	24.348	62	903	2015	µA
	Power-down mode, WDT/Timer/UART/RTC enable and run	-	V	26.066	65	913	2027	
	Power-down mode, WDT/Timer/UART enable and run	V	-	26.236	65	913	2027	
	Power-down mode, WDT/Timer/UART/RTC enable and run, WDT use LIRC, UART/Timer/RTC use LXT	V	V	27.469	67	919	2037	

Notes:

1. Crystal used: AURUM XF66RU000032C0 with a C_L of 12.5 pF for L2 gain level.
2. V_{DD} = AV_{DD} = 3.3V, LVR17 enabled, POR disabled and BOD disabled.
3. Based on characterization, not tested in production unless otherwise specified.
4. When analog peripheral blocks such as DAC, ADC and ACMP are ON, an additional power consumption should be considered.
5. Based on characterization, tested in production.

Table 8.3-3 Chip Current Consumption in Power-down mode

8.3.2 On-Chip Peripheral Current Consumption

- The typical values for T_A= 25 °C and V_{DD} = AV_{DD} = 3.3 V unless otherwise specified.
- All GPIO pins are set as output high of push pull mode without multi-function.
- HCLK is the system clock, f_{HCLK} = 120 MHz, $f_{PCLK0, 1}$ = 1/2 f_{HCLK}.
- The result value is calculated by measuring the difference of current consumption between all peripherals clocked off and only one peripheral clocked on

Peripheral	I_{DD}[*1]	Unit
PDMA0_ON	1038	µA
ISP_ON	~0	
STCLK_ON	418	
CRC_ON	144	
FMCIDLE_ON	1738	
GPICK_ON	204	
GPACK_ON	201	
GPBCK_ON	211	
GPCCK_ON	203	
GPDCK_ON	203	
GPECK_ON	201	
GPFCK_ON	211	
GPGCK_ON	200	
GPHCK_ON	216	
WDT_ON	552	
RTC_ON	104	
TMR0_ON	607	
TMR1_ON	602	
TMR2_ON	616	
TMR3_ON	621	
CLKO_ON	610	
ACMP01_ON	524	
I2C0_ON	230	
I2C1_ON	195	
SPI0_ON	1571	
SPI1_ON	1595	
UART0_ON	1014	
UART1_ON	1267	

UART2_ON	996	
UART3_ON	984	
UART4_ON	957	
UART5_ON	956	
ADC_ON	1344	
DAC0_ON	69	
CIR0_ON	242	
EPWM0_ON	967	
EPWM1_ON	925	
BPWM0_ON	227	
BPWM1_ON	194	
PRNG_ON	154	

Notes:

1. Guaranteed by characterization results, not tested in production.
2. When the ADC is turned on, add an additional power consumption per ADC for the analog part.
3. When the ACMP is turned on, add an additional power consumption per ACMP for the analog part.
4. When the DAC is turned on, add an additional power consumption per DAC for the analog part.

Table 8.3-4 Peripheral Current Consumption

8.3.3 Wakeup Time from Low-Power Modes

The wakeup times given in Table 8.2-1 is measured on a wakeup phase with a 48 MHz HIRC oscillator.

Symbol	Parameter	Typ	Max	Unit
t_{WU_IDLE}	Wakeup from IDLE mode	5	6	cycles
t_{WU_NPD}[*1][*2]	Wakeup from normal Power-down mode	15.2	18	uS
t_{ET_IDLE}	Enter to IDLE mode	1	1	cycles
t_{ET_NPD}	Enter to normal Power-down mode	10	13	cycles

Notes:

1. Based on test during characterization, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.

Table 8.3-5 Low-power mode wakeup timings

8.3.4 I/O Current Injection Characteristics

In general, I/O current injection due to external voltages below V_{SS} or above V_{DD} should be avoided during normal product operation. However, the analog compoenent of the MCU is most likely to be affected by the injection current , but it is not easily clarified when abnormal injection accidentally happens. It is recommended to add a Schottky diode (pin to ground or pin to V_{DD}) to pins that include analog function which may potentially injection currents.

Symbol	Parameter	Negative injection	Positive injection	Unit	Test Condition
$I_{INJ(PIN)}$	Injected current by a I/O Pin	-0	0	mA	Injected current on nReset pins
		-0	0		Injected current on PF2~PF5, PA10, PA11 and PB0~PB15 for analog input function
		-5	+5		Injected current on any other I/O except analog input pin

Table 8.3-6 I/O current injection characteristics

8.3.5 I/O DC Characteristics

8.3.5.1 PIN Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low voltage (Schmitt trigger)	0	-	$0.3*V_{DD}$	V	
	Input low voltage (TTL trigger)	0	-	0.8		V_{DD} = 4.5 V
		0	-	0.7		V_{DD} = 2.7 V
		0	-	0.5		V_{DD} = 2.5 V
V_{IH}	Input high voltage (Schmitt trigger)	$0.7*V_{DD}$	-	V_{DD}	V	
	Input high voltage (TTL trigger)	2	-	V_{DD}		V_{DD} = 5.5 V
		1.5	-	V_{DD}		V_{DD} = 3.3 V
		1.1	-	V_{DD}		V_{DD} = 2.5 V
V_{HY}[*1]	Hysteresis voltage of schmitt input	-	$0.2*V_{DD}$	-	V	
I_{LK}[*2]	Input leakage current	-1	-	1	µA	$V_{SS} < V_{IN} < V_{DD}$, Open-drain or input only mode
		-1	-	1		$V_{DD} < V_{IN} < 5$ V, Open-drain or input only mode on any other 5v tolerance pins
R_{PU}[*1]	Pull up resistor		77		kΩ	V_{DD} =5.5V

Notes:

1. Guaranteed by characterization result, not tested in production.
2. Leakage could be higher than the maximum value, if abnormal injection happens.

Table 8.3-7 I/O input Characteristics

8.3.5.2 I/O Output Characteristics

Symbol	Parameter	Min (sim)	Typ	Max (sim)	Unit	Test Conditions
I_{SR}[*1] [*2]	Source current for quasi-bidirectional mode and high level	-70.99	-110	-	μA	V_{DD} = 4.5 V V_{IN}=(V_{DD}-0.4) V
		-41.71	-67	-	μA	V_{DD} = 2.7 V V_{IN}=(V_{DD}-0.4) V
		-37.73	-61	-	μA	V_{DD} = 2.5 V V_{IN}=(V_{DD}-0.4) V
	Source current for push-pull mode and high level	-5.696	-8.12	-	mA	V_{DD} = 4.5 V V_{IN}=(V_{DD}-0.4) V
		-3.349	-4.87	-	mA	V_{DD} = 2.7 V V_{IN}=(V_{DD}-0.4) V
		-3.032	-4.40	-	mA	V_{DD} = 2.5 V V_{IN}=(V_{DD}-0.4) V
I_{SK}[*1] [*2]	Sinkcurrent for push-pull mode and low level	9.486	14.07	-	mA	V_{DD} = 4.5 V V_{IN}= 0.4 V
		5.648	8.75	-	mA	V_{DD} = 2.7 V V_{IN}= 0.4 V
		5.147	8.05	-	mA	V_{DD} = 2.5 V V_{IN}= 0.4 V
C_{IO}[*1]	I/O pin capacitance	-	5	-	pF	

Notes:

1. Guaranteed by characterization result, not tested in production.
2. The I_{SR} and I_{SK} must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.

Table 8.3-8 I/O output Characteristics

8.3.5.3 nRESET Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{ILR}	Negative going threshold, nRESET	-	-	0.3*V_{DD}	V	
V_{IHR}	Positive going threshold, nRESET	0.7*V_{DD}	-	-	V	
R_{RST}[*1]	Internal nRESET pull up resistor	30	50	190	kΩ	V_{DD}=5.5V
t_{FR}[*1]	nRESET input filtered pulse time	-	20	-	μS	Normal run and Idle mode
		26	-	38		Power-down mode

Notes:

1. Guaranteed by characterization result, not tested in production.
2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.

Table 8.3-9 nRESET Input Characteristics

8.4 AC Electrical Characteristics

8.4.1 48 MHz Internal High Speed RC Oscillator (HIRC)

The 48 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.5	-	5.5	V	
f_{HRC}	Oscillator frequnecy	47.52	48	48.48	MHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-1	-	1	%	T_A = 25 °C, V_{DD} = 3.3V
		-2[*1]	-	2[*1]	%	T_A = -40°C ~ +105 °C, V_{DD} = 2.5 ~ 5.5V
I_{HRC}[*1]	Operating current	-	400	700	μA	
T_S[*2]	Stable time		11	20	μS	T_A = -40°C ~ +105 °C, V_{DD} = 2.5 ~ 5.5V

Notes:

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design.

Table 8.4-1 48 MHz Internal High Speed RC Oscillator(HIRC) Characteristics

8.4.1 38.4 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{DD}	Operating voltage	2.5	-	5.5	V	
F_{LRC} [*2]	Oscillator frequnecy	-	38.4	-	kHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-2	-	2	%	T_A = 25 °C, V_{DD} = 3.3V
		-15	-	15	%	T_A=-40~105°C V_{DD}=2.5V~5.5V Without software calibration
I_{LRC}	Operating current	-	1	1.6	µA	V_{DD} = 3.3V
T_S	Stable time	-	200	500	µS	T_A=-40~105°C V_{DD}=2.5V~5.5V

Notes:

1. Guaranteed by characterization, not tested in production.
2. The 38.4 kHz low speed RC oscillator can be calibrated by user.
3. Guaranteed by design.

Table 8.4-2 38.4 kHz Internal Low Speed RC Oscillator(LIRC) Characteristics

8.4.2 External 4~24 MHz High Speed Crystal/Ceramic Resonator (HXT) Characteristics

The high-speed external (HXT) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the XT1_IN and XT1_Out pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
V_{DD}	Operating voltage	2.5	-	5.5	V	
R_f	Internal feedback resister	-	250	-	kΩ	
f_{HXT}	Oscillator frequency	4	-	24	MHz	
I_{HXT}	Current consumption (Crystal type)	-	0.3	1	mA	4 MHz, Gain = L0, C_L = 12.5 pF
		-	1	4		12 MHz, Gain = L1, C_L = 12.5 pF
		-	1.5	6.7		16 MHz, Gain = L2, C_L = 12.5 pF
		-	2.2	9		24 MHz, Gain = L3, C_L = 12.5 pF
I_{HXT}	Current consumption (Resonator type)	-	0.45	2	mA	4 MHz, Gain = L0, C_L = 30 pF
		-	0.8	3.2		12 MHz, Gain = L1, C_L = 20 pF
		-	1.5	8		16 MHz, Gain = L2, C_L = 10 pF
		-	2	9		24 MHz, Gain = L3, C_L = 10 pF
T_S	Stable time (Crystal type)	-	4.5	8.5	mS	4 MHz, Gain = L0, C_L = 12.5 pF
		-	3	3.5		12 MHz, Gain = L1, C_L = 12.5 pF
		-	2.5	2.8		16 MHz, Gain = L2, C_L = 12.5 pF
		-	1.5	2		24 MHz, Gain = L3, C_L = 12.5 pF
T_S	Stable time (Resonator type)	-	1.04	1.1	mS	4 MHz, Gain = L0, C_L = 30 pF
		-	0.35	0.4		12 MHz, Gain = L1, C_L = 20 pF
		-	0.26	0.3		16 MHz, Gain = L2, C_L = 10 pF
		-	0.21	0.25		24 MHz, Gain = L3, C_L = 10 pF
Du_{HXT}	Duty cycle	40	-	60	%	
Vpp	Peak-to-peak amplitude	$0.3*V_{DD}$	$0.5*V_{DD}$	$0.7*V_{DD}$	V	

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions

Notes:

1. Guaranteed by characterization, not tested in production.

Table 8.4-3 External 4~24 MHz High Speed Crystal (HXT) Oscillator

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
Rs	Equivalent series resisotr(ESR)	-	-	150	Ω	Crystal @4 MHz, C_L = 12.5 pF, Gain = L0
		-	-	120		Crystal @12 MHz, C_L = 12.5 pF, Gain = L1
		-	-	100		Crystal @16 MHz, C_L = 12.5 pF, Gain = L2
		-	-	80		Crystal @24 MHz, C_L = 12.5 pF, Gain = L3
		-	-	40		Ceramic Resonator @4 MHz, C_L = 30 pF, Gain = L0
		-	-	20		Ceramic Resonator @12 MHz, C_L = 20 pF, Gain = L1
		-	-	60		Ceramic Resonator @16 MHz, C_L = 10 pF, Gain = L2
		-	-	60		Ceramic Resonator @24 MHz, C_L = 10 pF, Gain = L3

Notes:

1. Guaranteed by characterization, not tested in production.
2. Safety factor (S_f) must be higher than 5 for HXT to determine the oscillator safe operation during the application life. If Safety factor isn't enough, the HXT gain need be changed to higher driving level.

$$S_f = \frac{-R}{Crystal\ ESR} = \frac{R_{ADD} + R_S}{R_S}$$

R_{ADD}: The value of smallest series resistance preventing the oscillator from starting up successfully. This resistance is only used to measure Safety factor (S_f) of crystal in engineer stage, not for mass produciton.

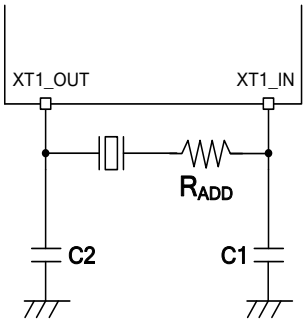


Table 8.4-4 External 4~24 MHz High Speed Crystal Characteristics

8.4.2.1 Typical Crystal Application Circuits

For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 10 pF ~ 20 pF range, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. The crystal manufacturer typically specifies a load capacitance which is the series combination of C1 and C2. PCB and MCU pin capacitance must be included (8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

CRYSTAL	C1	C2	R1
4 MHz ~ 24 MHz	10 ~ 20 pF	10 ~ 20 pF	without

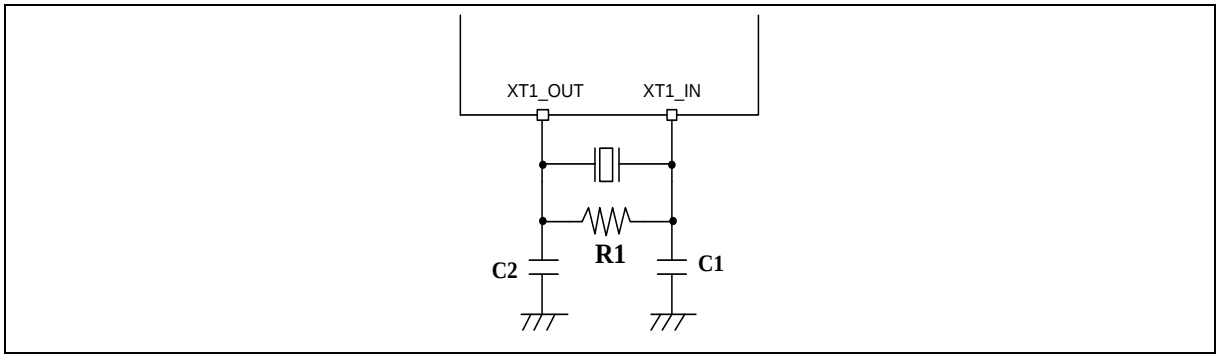
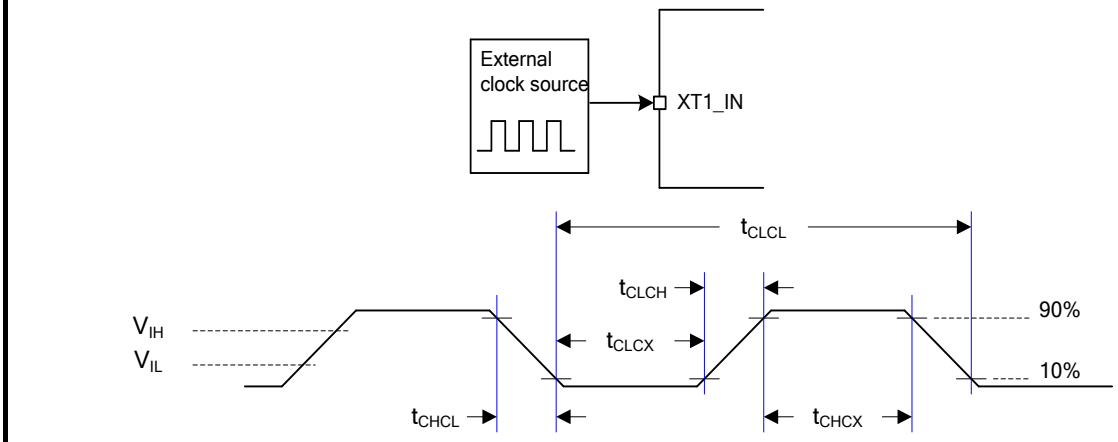


Figure 8.4-1 Typical Crystal Application Circuit

8.4.3 External 4~24 MHz High Speed Clock Input Signal Characteristics

For clock input mode the HXT oscillator is switched off and XT1_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{HXT_ext}	External user clock source frequency	1	-	24	MHz	
t_{CHCX}	Clock high time	16	-	-	nS	
t_{CLCX}	Clock low time	16	-	-	nS	
t_{CLCH}	Clock rise time	-	-	10	nS	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	10	nS	High (90%) to low level (10%) fall time
Du_{E_HXT}	Duty cycle	40	-	60	%	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	XT1_IN should be set as Schmitt Trigger Mode
V_{IL}	Input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Notes:

1. Guaranteed by characterization, not tested in production.

Table 8.4-5 External 4~24 MHz High Speed Clock Input Signal

8.4.4 External 32.768 kHz Low Speed Crystal/Ceramic Resonator (LXT) Characteristics

The low-speed external (LXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the X32_OUT and X32_IN pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{DD}	Operation voltage	2.5	-	5.5	V	
T_{LXT}	Temperature range	-40	-	105	°C	
R_f	Internal feedback resistor	-	6	-	MΩ	
F_{LXT}	Oscillator frequency		32.768		kHz	
I_{LXT}	Current consumption	0.3	0.55	4.4	µA	ESR=35 kΩ, C_L = 12.5 pF, Gain = L0
		0.3	0.65	4.6		ESR=35 kΩ, C_L = 12.5 pF, Gain = L1
		0.4	0.72	4.8		ESR=35 kΩ, C_L = 12.5 pF, Gain = L2
		0.55	0.9	5.2		ESR=70 kΩ, C_L = 12.5 pF, Gain = L3
		0.57	1	5.4		ESR=70 kΩ, C_L = 12.5 pF, Gain = L4
		0.62	1.1	5.6		ESR=70 kΩ, C_L = 12.5 pF, Gain = L5
		0.75	1.3	6		ESR=90 kΩ, C_L = 12.5 pF, Gain = L6
		0.92	1.6	6.6		ESR=90 kΩ, C_L = 12.5 pF, Gain = L7
Ts_{LXT}	Stable time	-	1	2	S	
Du_{LXT}	Duty cycle	30	-	70	%	
V_{pp}	Peak-to-peak amplitude	-	0.5	-	V	

Notes:
1. Guaranteed by characterization, not tested in production.

Table 8.4-6 External 32.768 kHz Low Speed Crystal (LXT) Oscillator

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Rs	Equivalnet Series Resisotr(ESR)	-	35	70	kΩ	Crystal @32.768 kHz

Table 8.4-7 External 32.768 kHz Low Speed Crystal Characteristics

8.4.4.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R1
32.768 kHz, ESR < 70 KΩ	5 ~ 20 pF	5 ~ 20 pF	without

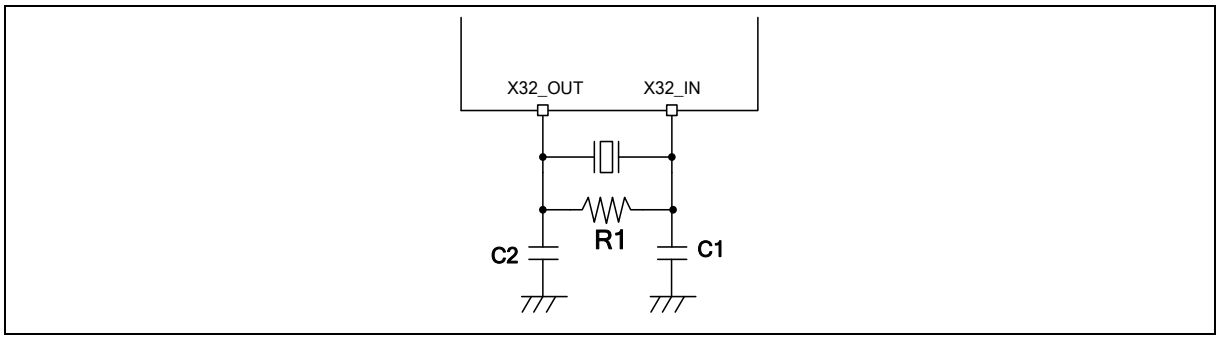
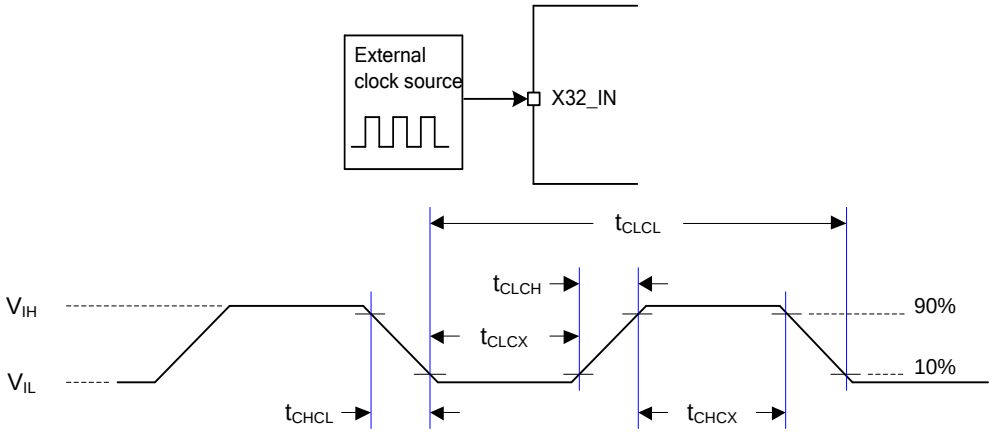


Figure 8.4-2 Typical 32.768 kHz Crystal Application Circuit

8.4.5 External 32.768 kHz Low Speed Clock Input Signal Characteristics

For clock input mode the LXT oscillator is switched off and X32_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{LXT_ext}	External clock source frequency	-	32.768	-	kHz	
t_{CHCX}	Clock high time	450	-	-	nS	
t_{CLCX}	Clock low time	450	-	-	nS	
t_{CLCH}	Clock rise time	-	-	50	nS	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	50	nS	High (90%) to low level (10%) fall time
Du_{E_LXT}	Duty cycle	30	-	70	%	
V_{IH}	LXT input pin input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	X32_IN should be set as Schmitt Trigger Mode
V_{IL}	LXT input pin input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Notes:

1. Guaranteed by design, not tested in production

Table 8.4-8 External 32.768 kHz Low Speed Clock Input Signal

8.4.6 PLL Characteristics

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
f_{PLL_in}	PLL input clock	4	-	24	MHz	
f_{PLL_OUT}	PLL multiplier output clock	16	-	120	MHz	
f_{PLL_REF}	PLL reference clock	4	-	8	MHz	
f_{PLL_VCO}	PLL voltage controlled oscillator	64	-	120	MHz	
T_L	PLL locking time	-	-	100	µS	
Jitter[*2]	Cycle-to-cycle Jitter	-	-	500	pS	
I_{DD}	Power consumption	-	1	2	mA	V_{DD}=5.5V @ f_{PLL_VCO} = 100 MHz

Notes:

1. Guaranteed by characterization, not tested in production
2. Guaranteed by design, not tested in production

Table 8.4-9 PLL Characteristics

8.4.7 I/O AC Characteristics

Symbol	Parameter	Typ.	Max[*1].	Unit	Test Conditions[*2]
$t_{f(IO)out}$	Output high (90%) to low level (10%) fall time (Normal Slew Rate)	7.06	11.745	nS	C_L = 30 pF, V_{DD} >= 4.5 V
		4.85	8.807		C_L = 10 pF, V_{DD} >= 4.5 V
		11.44	19.96		C_L = 30 pF, V_{DD} >= 2.7 V
		8.53	14.399		C_L = 10 pF, V_{DD} >= 2.7 V
		13.33	21.921		C_L = 30 pF, V_{DD} >= 2.5 V
		9.69	15.932		C_L = 10 pF, V_{DD} >= 2.5 V
	Output high (90%) to low level (10%) fall time (High Slew Rate)	4.46	7.785		C_L = 30 pF, V_{DD} >= 4.5 V
		2.81	4.76		C_L = 10 pF, V_{DD} >= 4.5 V
		6.79	12.257		C_L = 30 pF, V_{DD} >= 2.7 V
		4.42	7.817		C_L = 10 pF, V_{DD} >= 2.7 V
		7.51	13.287		C_L = 30 pF, V_{DD} >= 2.5 V
		5	8.569		C_L = 10 pF, V_{DD} >= 2.5 V
$t_{r(IO)out}$	Output low (10%) to high level (90%) rise time (Normal Slew Rate)	6.57	11.88	nS	C_L = 30 pF, V_{DD} >= 4.5 V
		4.04	7.742		C_L = 10 pF, V_{DD} >= 4.5 V
		10.96	19.128		C_L = 30 pF, V_{DD} >= 2.7 V
		6.83	12.18		C_L = 10 pF, V_{DD} >= 2.7 V
		12.2	21.363		C_L = 30 pF, V_{DD} >= 2.5 V
		7.76	13.352		C_L = 10 pF, V_{DD} >= 2.5 V
	Output low (10%) to high level (90%) rise time (High Slew Rate)	5.17	9.151	nS	C_L = 30 pF, V_{DD} >= 4.5 V
		2.77	5.109		C_L = 10 pF, V_{DD} >= 4.5 V
		8.3	14.602		C_L = 30 pF, V_{DD} >= 2.7 V
		4.66	7.891		C_L = 10 pF, V_{DD} >= 2.7 V
		9.42	15.941		C_L = 30 pF, V_{DD} >= 2.5 V
		5.24	8.617		C_L = 10 pF, V_{DD} >= 2.5 V
Symbol	**Parameter**	**Typ.**	**Min[*1].**	**Unit**	**Test Conditions[*2]**

$f_{max(IO)out}$[*3]	I/O maximum frequency (Normal Slew Rate)	48.91	28.2	MHz	C_L = 30 pF, V_{DD} >= 4.5 V
		74.99	40.3		C_L = 10 pF, V_{DD} >= 4.5 V
		29.76	17.1		C_L = 30 pF, V_{DD} >= 2.7 V
		43.4	25.1		C_L = 10 pF, V_{DD} >= 2.7 V
		26.11	15.4		C_L = 30 pF, V_{DD} >= 2.5 V
		38.2	22.8		C_L = 10 pF, V_{DD} >= 2.5 V
	I/O maximum frequency (High Slew Rate)	69.23	39.4	MHz	C_L = 30 pF, V_{DD} >= 4.5 V
		119.47	67.6		C_L = 10 pF, V_{DD} >= 4.5 V
		44.18	24.8		C_L = 30 pF, V_{DD} >= 2.7 V
		73.42	42.4		C_L = 10 pF, V_{DD} >= 2.7 V
		39.38	22.8		C_L = 30 pF, V_{DD} >= 2.5 V
		65.10	38.8		C_L = 10 pF, V_{DD} >= 2.5 V
I_{DIO}[*4]	I/O dynamic current consumption	2.77	-	mA	C_L = 30 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 24 MHz
		1.19	-		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 24 MHz
		0.69	-		C_L = 30 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 6 MHz
		0.3	-		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 6 MHz

Notes:

1. Guaranteed by characterization result, not tested in production.
2. C_L is a external capacitive load to simulate PCB and device loading.
3. The maximum frequency is defined by $f_{max} = \frac{2}{3 \times (t_f + t_r)}$.
4. The I/O dynamic current consumption is defined by $I_{DIO} = V_{DD} \times f_{IO} \times (C_{IO} + C_L)$

Table 8.4-10 I/O AC Characteristics

8.5 Analog Characteristics

8.5.1 LDO

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	Power supply	2.5	-	5.5	V	
V_{LDO}	Output voltage	-	1.8	-	V	
T_A	Temperature	-40	-	105	℃	

Notes:

1. It is recommended a 0.1μF bypass capacitor is connected between VDD and the closest V_{SS} pin of the device.
2. For ensuring power stability, a 1μF capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device.
3. V_{LDO} is only used to supply internal power.

8.5.2 Reset and Power Control Block Characteristics

The parameters in below table are derived from tests performed under ambient temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{POR}[*1]	POR operating current	-	10	20	μA	AV_{DD} = 3.3V
I_{LVR}[*1]	LVR operating current	-	1	4.5		AV_{DD} = 3.3V
I_{BOD}[*1]	BOD operating current	-	10	25.2		AV_{DD} = 3,3V, Normal mode
		-	1	2.4		AV_{DD} = 3.3V, Low Power mode
V_{POR}	POR reset voltage(Falling edge)	2.10	2.20	2.30	V	
	POR reset voltage(Rising edge)	2.15	2.25	2.35		
V_{LVR}	LVR reset voltage(Falling edge)	2.25	2.35	2.45		
	LVR reset voltage(Rising edge)	2.30	2.40	2.50		
V_{BOD}	BOD brown-out detect voltage (Falling edge)	2.30	2.40	2.50		BODVL = 0
		2.60	2.70	2.80		BODVL = 1
		3.60	3.70	3.80		BODVL = 2
		4.20	4.40	4.60		BODVL = 3
	BOD brown-out detect voltage (Rising edge)	2.38	2.48	2.58		BODVL = 0
		2.68	2.78	2.88		BODVL = 1
		3.68	3.78	3.88		BODVL = 2
		4.28	4.48	4.68		BODVL = 3
T_{LVR_SU}[*1]	LVR startup time	-	50	65	μS	-
T_{LVR_RE}[*1]	LVR respond time	-	2	5		-
T_{BOD_SU}[*1]	BOD startup time	-	260.4	306.4		-
T_{BOD_RE}[*1]	BOD respond time	-	2	2.5		Normal mode

		-	-	3862		Low Power mode
R_{VDDR}[*1]	V_{DD} rise time rate	10	-	-	µS/V	POR Enabled
R_{VDDF}[*1]	V_{DD} fall time rate	10	-	-		POR Enabled
		100	-	-		LVR Enabled
		10	-	-		BOD Enabled, Normal mode

Notes:

1. Guaranteed by characterization, not tested in production.
2. Design for specified applcaiton.

Table 8.5-1 Reset and Power Control Unit

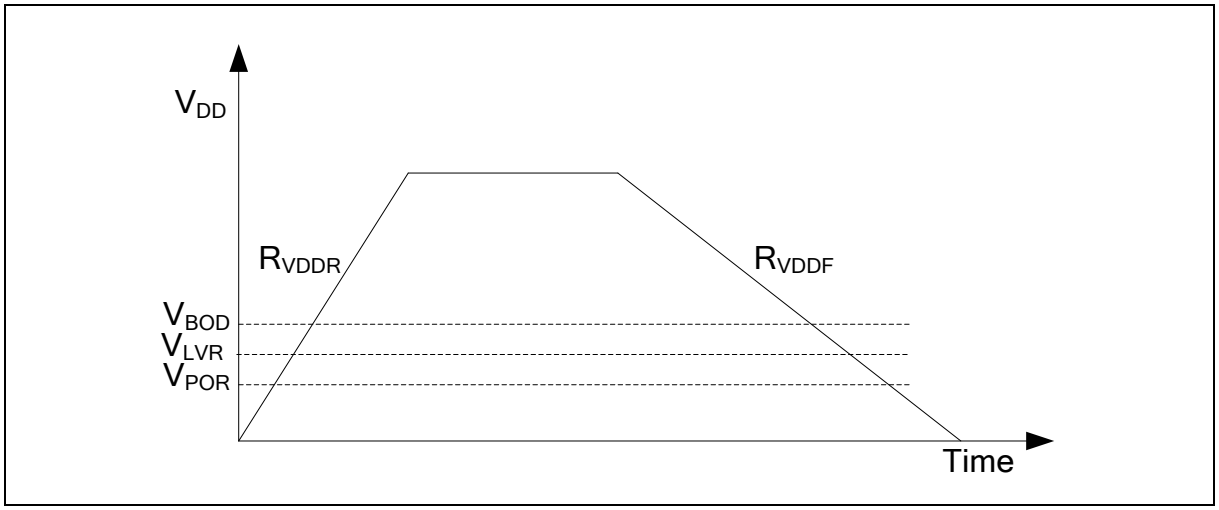


Figure 8.5-1 Power Ramp Up/Down Condition

8.5.3 12-bit SAR Analog To Digital Converter (ADC)

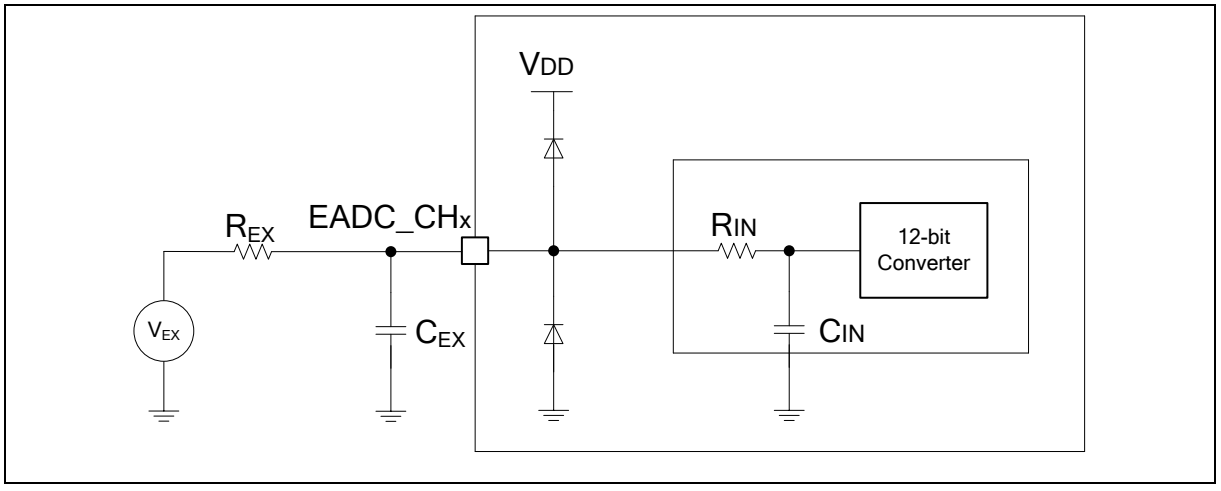
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
AV_{DD}	Analog operating voltage	2.5	-	5.5	V	$V_{DD} = AV_{DD}$
V_{REF}	Reference voltage	2.5	-	AV_{DD}	V	AV_{DD}-V_{REF} < 2.5V
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
I_{ADC}[*1]	ADC Operating current (AV_{DD} + V_{REF} current)	-	168	TBD	µA	$AV_{DD} = V_{DD} = V_{REF}$ = 5.0 V F_{ADC} = 36 MHz T_{CONV} = 19 * T_{ADC} 25℃
N_R	Resolution	12			Bit	
F_{ADC}[*1] $1/T_{ADC}$	ADC Clock frequency	4	-	36	MHz	2.7V < AV_{DD} < 5.5V
		TBD	-	33	MHz	2.5V < AV_{DD} < 5.5V

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_{SMP}	Sampling Time	1	-	256	$1/F_{ADC}$	T_{SMP} = (EXTSMPT(EADC_SCTLx[31:24]) + 1) * T_{ADC}
T_{CONV}	Conversion time	19	-	274	$1/F_{ADC}$	$T_{CONV} = T_{SMP} + 18 * T_{ADC}$
F_{SPS}[*1]	Sampling Rate	TBD	-	1895	kSPS	$F_{SPS} = F_{ADC} / T_{CONV}$
T_{EN}	Enable to ready time	1	-	-	$1/ F_{ADC}$	
INL[*1]	Integral Non-Linearity Error	-3.7	-	3.3	LSB	$V_{REF} = AV_{DD}$
DNL[*1]	Differential Non-Linearity Error	-1	-	3.8	LSB	$V_{REF} = AV_{DD}$
E_G[*1]	Gain error	-4	-	4	LSB	$V_{REF} = AV_{DD}$
E_O[*1]$_T$	Offset error	-4	-	4	LSB	$V_{REF} = AV_{DD}$
E_A[*1]	Absolute Error	-4	-	4	LSB	$V_{REF} = AV_{DD}$
ENOB[*1]	Effective number of bits	-	10	-	bits	F_{ADC} = 36 MHz $AV_{DD} = V_{DD} = V_{REF}$ = 3.3 V Input Frequency = 20 kHz T_A = 25 °C
SINAD[*1]	Signal-to-noise and distortion ratio	-	62.02	-	dB	
SNR[*1]	Signal-to-noise ratio	-	62.12	-		
THD[*1]	Total harmonic distortion	-	-74.63	-		
C_{IN}[*1]	Internal Capacitance	-	3.6	-	pF	
R_{IN}[*1]	Internal Switch Resistance	-	-	0.85	kΩ	
R_{EX}[*1]	External input impedance	-	-	TBD	kΩ	

Notes:

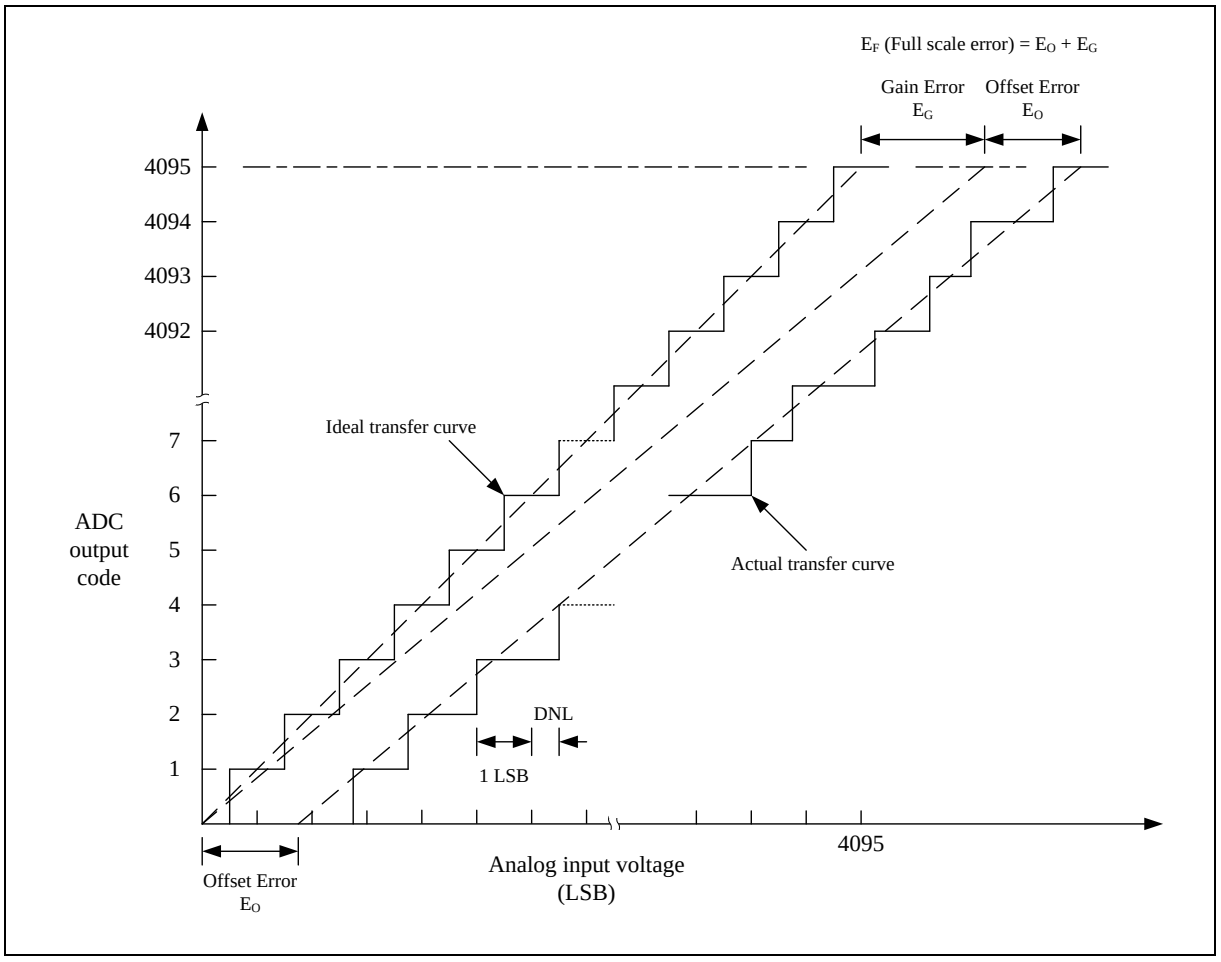
1. Guaranteed by characterization result, not tested in production.
2. R_{EX} max formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resoluton) and k is the number of sampling clocks (T_{SMP}). C_{EX} represents the capacitance of PCB and pad and is combined with R_{EX} into a low-pass filter. Once the R_{EX} and C_{EX} values are too large, it is possible to filter the real signal and reduce the ADC accuracy.

$$R_{EX} = \frac{k}{f_{ADC} \times C_{IN} \times \ln(2^{N+2})} - R_{IN}$$



Note: Injection current is a important topic of ADC accuracy. Injecting current on any analog input pins should be avoided to protect the conversion being performed on another analog input. It is

recommended to add Schottky diodes (pin to ground and pin to power) to analog pins which may potentially inject currents.



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

8.5.4 Digital to Analog Converter (DAC)

The maximum values are obtained for V_{DD} = 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Analog supply voltage	2.5	-	5.5	V	
N_R	Resolution		8		bit	
V_{REF}	Reference supply voltage	2.4	-	AV_{DD}	V	$V_{REF} \le AV_{DD}$
DNL[*2]	Differential non-linearity error	-	±0.4	-	LSB	No Loading
INL[*2]	Integral non-linearity error	-	±0.5	-	LSB	No Loading
OE[*2]	Offset Error	-	±0.5	-	LSB	No Loading
GE[*2]	Gain Error	-	±0.5	-	LSB	No Loading
AE[*2]	Absolute Error	-	-	±1	LSB	No Loading
		-	-	±2	LSB	AV_{DD} = V_{REF} = 3.072 ~ 5.5V and R_{LOAD} = 4M ohm
		-	-	±3	LSB	AV_{DD} = V_{REF} = 3.072 ~ 5.5V and R_{LOAD} = 2M ohm
-	Monotonic		8-bit guaranteed		-	
V_O[*1]	Output Voltage	1*LSB	-	V_{REF} - 1*LSB	V	
R_{LOAD}[*2] [*3]	Resistive load	5	-	-	kΩ	
R_O[*2]	Output impedance	-	6.4	-	kΩ	
C_{LOAD}[*2] [*4]	Capacitive load	-	-	35	pF	-
I_{DAC_AVDD}[*2]	DAC operating current on AV_{DD} supply	-	10	-	μA	AV_{DD} = 5.5V, no load
I_{DAC_VREF}[*2]	DAC operating current on V_{REF} supply	-	-	1000	μA	AV_{DD} = 5.5V, no load
T_B[*2]	Settling Time	-	4	4.5	μS	Full scale: for a 8-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value +/-1 LSB, $C_{LOAD} \le$ 35pF, No R_{LOAD}

Note:

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production.
3. Resistive load between DACOUT and AV_{SS}.
4. Capacitive load at DACOUT pin.

8.5.5 Analog Comparator Controller (ACMP)

The maximum values are obtained for V_{DD} = 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
AV_{DD}	Analog supply voltage	2.5	-	5.5	V	$V_{DD} = AV_{DD}$
T_A	Temperature	-40	-	105	℃	
I_{ACMP}[*2]	ACMP operating current	-	75	150	μA	
V_{CM}[*2]	Input common mode voltage range	0	1/2 AV_{DD}	AV_{DD}		
V_{DI}[*2]	Differential input voltage sensitivity	30	-	-	mV	(20mV+10mV offset)
V_{offset}[*2]	Input offset voltage	-	±10	±20	mV	
V_{hys}[*2]	Hysteresis window	-	0	-	mV	HYSSEL = 000
		10	20	40		HYSSEL = 010
		20	40	70		HYSSEL = 100
A_v[*1]	DC voltage Gain	43	70	-	dB	
T_d[*2]	Propagation delay	-	120	200	nS	
T_{Setup}[*2]	Setup time	-	-	5	μS	
A_{CRV}[*2]	CRV output voltage	-1.6	-	1.6	%	AV_{DD} x (CRVCTL/63)
I_{DD_CRV}[*2]	Operating current	-	50	100	μA	

Notes:

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production

Table 8.5-2 ACMP Characteristics

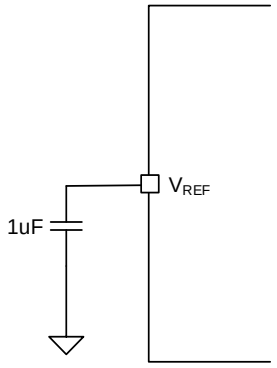
8.5.6 Internal Voltage Reference

The maximum values are obtained for V_{DD} = 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{REF_INT}	Internal reference voltage	2.017	2.048	2.079	V	AV_{DD} >= 2.5 V
		2.521	2.560	2.599		AV_{DD} >= 2.9 V
		3.026	3.072	3.118		AV_{DD} >= 3.4 V
		4.034	4.096	4.158		AV_{DD} >= 4.5 V
T_s[*1]	Stable time	-	0.5	0.8	mS	C_L =4.7 uF, V_{REF} initial=0, Preload is enabled.
		-	9.3	13	mS	C_L =4.7 uF, V_{REF} initial=5.5, Preload is enabled.
		-	24	180	mS	C_L =1 uF, V_{REF} initial=0, Preload is enabled.
		-	2	2.6	mS	C_L =1 uF, V_{REF} initial=5.5, Preload is enabled.
I_{VREF_INT}[*1]	V_{REF_INT} operating current	-	-	1	mA	
I_{VREF_LOAD}[*1]	V_{REF_INT} output loading current	-	-	1.5	mA	

Note:

1. Guaranteed by characterization, not tested in production



Note: V_{REF_INT} is only supported while package includes V_{REF} pin with external capacitor.

Figure 8.5-2 Typical connection with internal voltage reference

8.5.7 Temperature Sensor

The maximum values are obtained for V_{DD} = 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{TEMP_OS}[*1]	Temperature sensor offset voltage	735	749	755	mV	T_A = 0°C
T_C[*1]	Temperature Coefficient	-1.55	-1.698	-1.75	mV/°C	
T_S[*2]	Stable time	-	-	2	µS	
T_{TEMP_ADC}[*1]	ADC sampling time when reading the temperature	-	10	15	µS	
I_{TEMP}[*1]	Temperature sensor operating current	-	16	30	µA	

Note:

1. Guaranteed by characterization, not tested in production
2. Guaranteed by design, not tested in production
3. V_{TEMP} (mV) = T_C (mV/°C) x Temperature (°C) + V_{TEMP_OS} (mV)

8.6 Communications Characteristics

8.6.1 SPI Dynamic Characteristics

Symbol	Parameter	Specificaitons[*1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} 1/ T_{SPICLK}	SPI clock frequency	-	-	32	MHz	4.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	25		2.7 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	25		2.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			nS	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			nS	
t_{DS}	Data input setup time	0	-	-	nS	
t_{DH}	Data input hold time	4.7	-	-	nS	
t_V	Data output valid time	-	-	2	nS	4.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	2	nS	2.7 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	2	nS	2.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF

Note:

1. Guaranteed by design.

Table 8.6-1 SPI Master Mode Characteristics

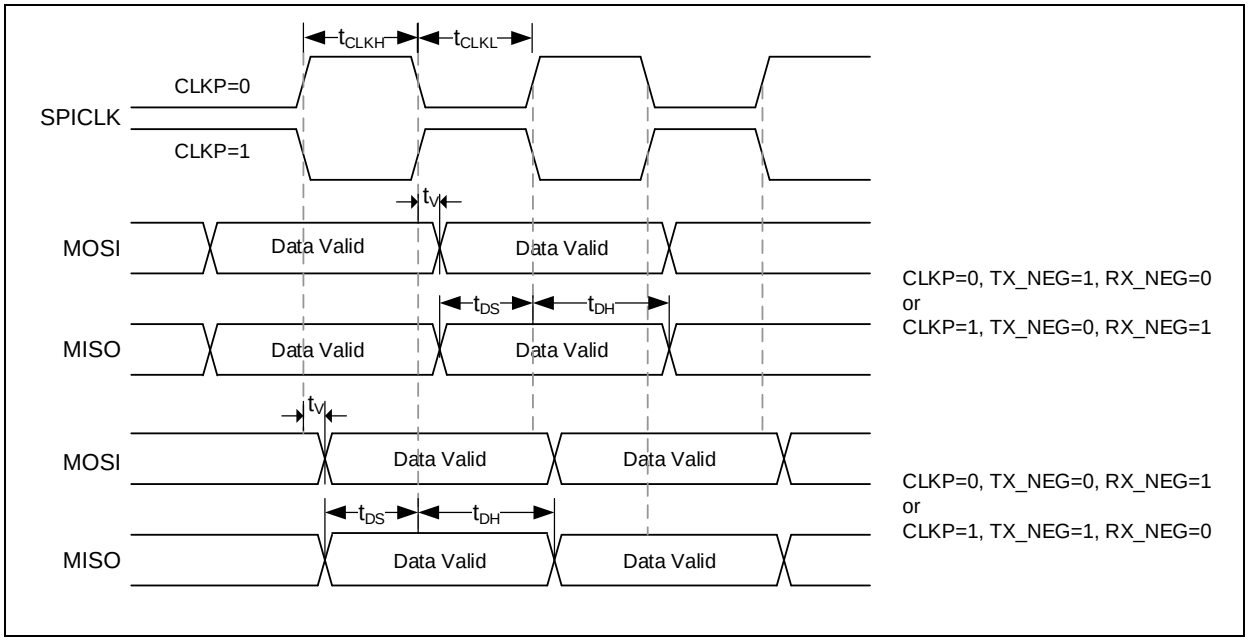


Figure 8.6-1 SPI Master Mode Timing Diagram

Symbol	Parameter	Specificaitons[*1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	18	MHz	4.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	15		2.7 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	14		2.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			nS	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			nS	
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	nS	4.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		1 T_{SPICLK} + 3ns	-	-		2.7 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		1 T_{SPICLK} + 3ns	-	-		2.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	nS	
t_{DS}	Data input setup time	1	-	-	nS	
t_{DH}	Data input hold time	6	-	-	nS	
t_V	Data output valid time	-	-	26	nS	4.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	32		2.7 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	34		2.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF

Note:

1. Guaranteed by design.

Table 8.6-2 SPI Slave Mode Characteristics

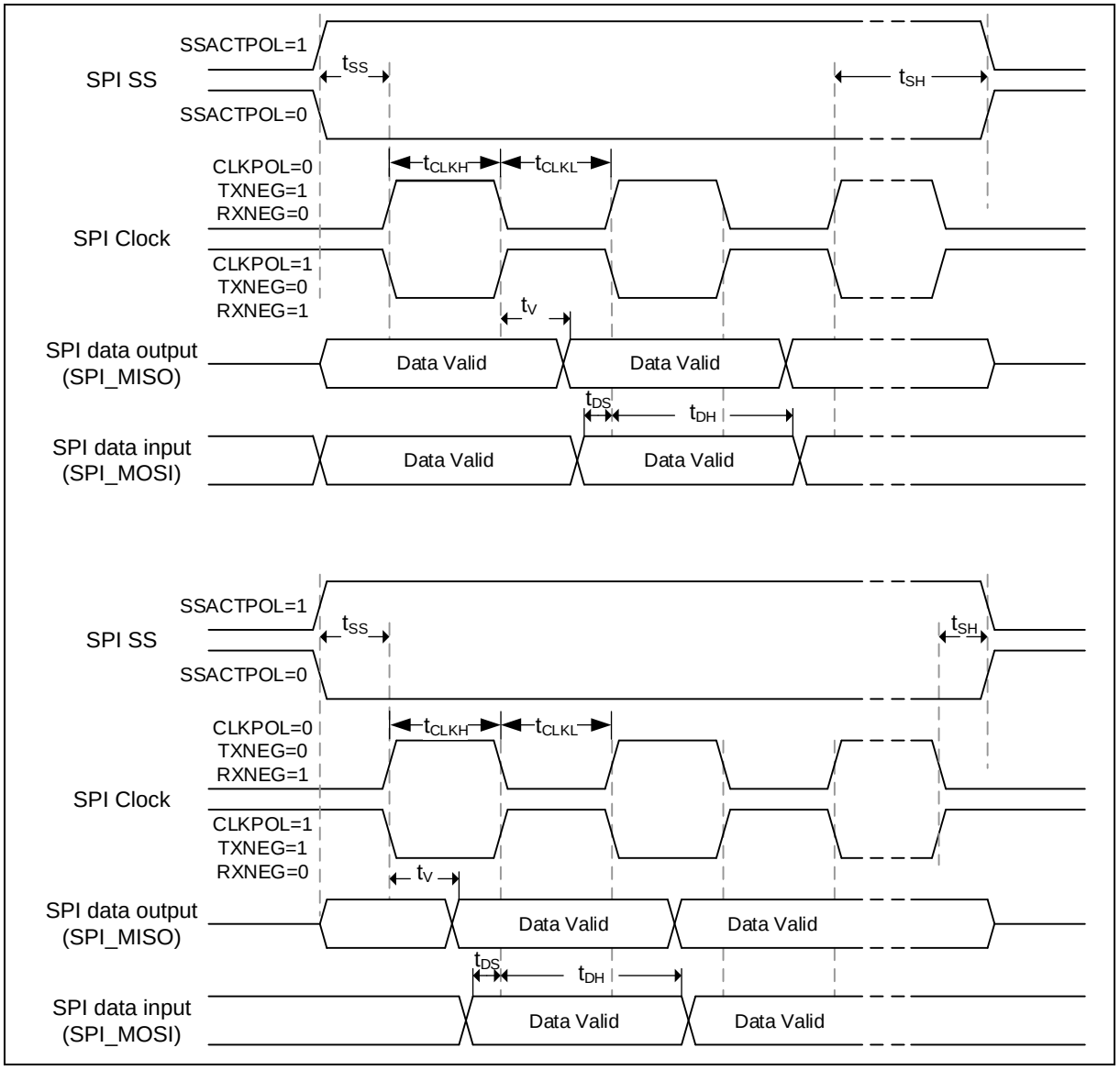


Figure 8.6-2 SPI Slave Mode Timing Diagram

8.6.2 SPI - I²S Dynamic Characteristics

Symbol	Parameter	Min [*1]	Max [*1]	Unit	Test Conditions
$t_{w(CKH)}$	I²S clock high time	80	-	nS	Master f_{PCLK} = 48 MHz, data: 24 bits, audio frequency = 128 kHz
$t_{w(CKL)}$	I²S clock low time	80	-		
$t_{v(WS)}$	WS valid time	0	6		Master mode
$t_{h(WS)}$	WS hold time	0	-		Master mode
$t_{su(WS)}$	WS setup time	16	-		Slave mode
$t_{h(WS)}$	WS hold time	0	-		Slave mode
$DuCy_{(SCK)}$	I²S slave input clock duty cycle	35	65	%	Slave mode
$t_{su(SD\_MR)}$	Data input setup time	2	-	nS	Master receiver
$t_{su(SD\_SR)}$		0	-		Slave receiver
$t_{h(SD\_MR)}$	Data input hold time	5	-		Master receiver
$t_{h(SD\_SR)}$		6	-		Slave receiver
$t_{v(SD\_ST)}$	Data output valid time	-	30		Slave transmitter (after enable edge)
$t_{h(SD\_ST)}$	Data output hold time	4	-		Slave transmitter (after enable edge)
$t_{v(SD\_MT)}$	Data output valid time	-	4		Master transmitter (after enable edge)
$t_{h(SD\_MT)}$	Data output hold time	0	-		Master transmitter (after enable edge)

Note:

1. Guaranteed by design.

Table 8.6-3 I²S Characteristics

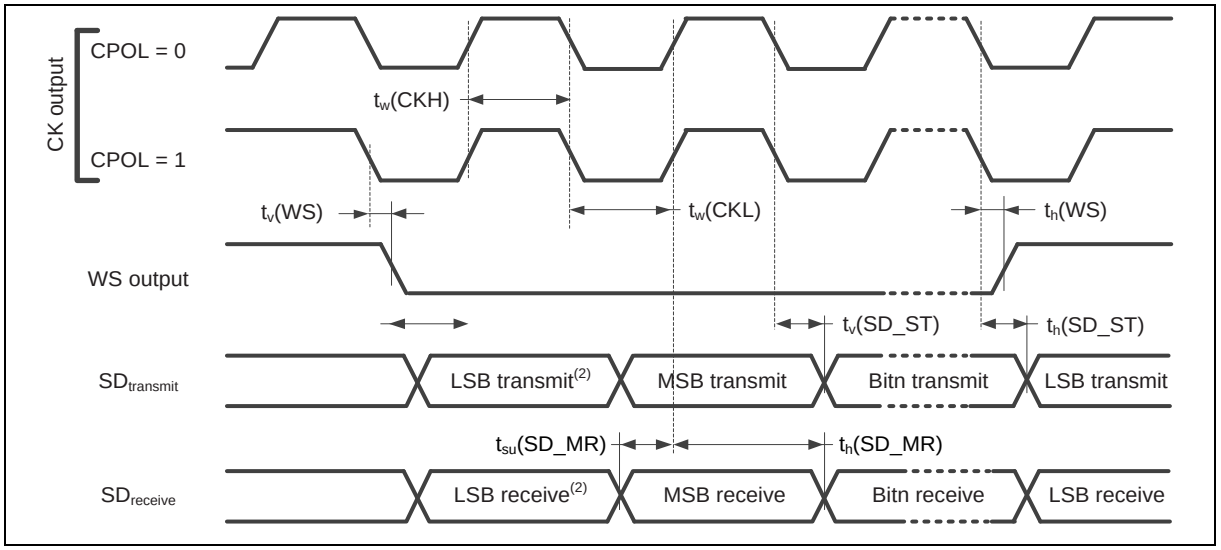


Figure 8.6-3 I²S Master Mode Timing Diagram

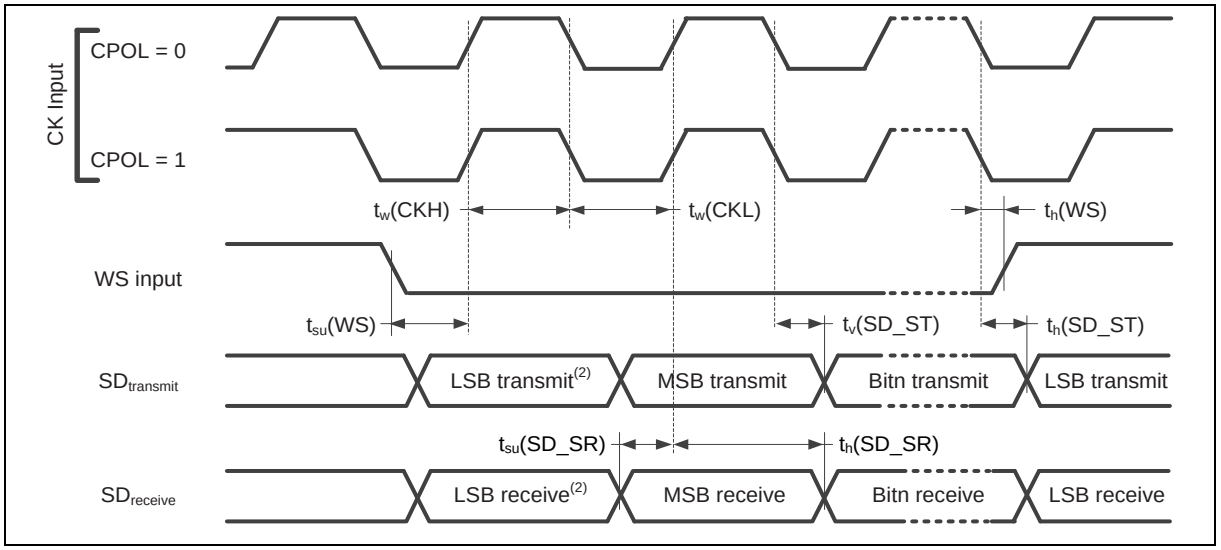


Figure 8.6-4 I²S Slave Mode Timing Diagram

8.6.3 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	μS
t_{HIGH}	SCL high period	4	-	0.6	-	μS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	μS
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	μS
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	μS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	μS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	μS
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Notes:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I²C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-4 I²C Characteristics

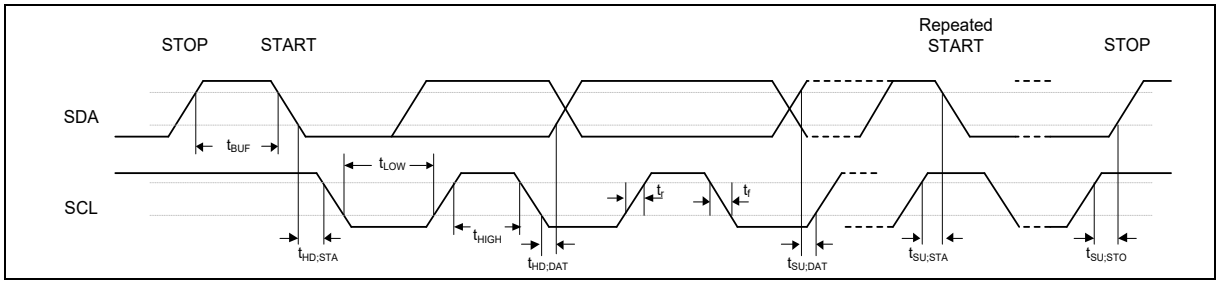


Figure 8.6-5 I²C Timing Diagram

8.7 Flash DC Electrical Characteristics

The devices are shipped to customers with the Flash memory erased.

Symbol	Parameter	Min[3]	Typ	Max	Unit	Test Condition
V_{FLA}[1]	Supply voltage	-	1.8	-	V	T_A = 25℃
T_{ERASE}	Page erase time	-	25	-	mS	
$T_{MASS\ ERASE}$	Mass erase time	-	127	-	mS	
$T_{BANK\ ERASE}$	Bank erase time	-	127	-	mS	
T_{PROG}	Program time	-	98	-	μS	
I_{DD2}	Program current	-	10	-	mA	
I_{DD3}	Erase current	-	12	-	mA	
N_{ENDUR}	Cycling Endurance	20,000	-	-	cycles[2]	T_J = -40℃~125℃
T_{RET}	Data retention	65	-	-	year	20 kcycle[2], T_J = 55℃
		10	-	-		20 kcycle[2], T_J = 85℃
		4	-	-		20 kcycle[2], T_J = 125℃

Notes:

1. V_{FLA} is source from chip internal LDO output voltage.
2. Number of program/erase cycles. The flash data can only be programmed once at the same address after flash erase.
3. Guaranteed by design.

8.8 Data Flash DC Electrical Characteristics

The devices are shipped to customers with the Data Flash memory erased.

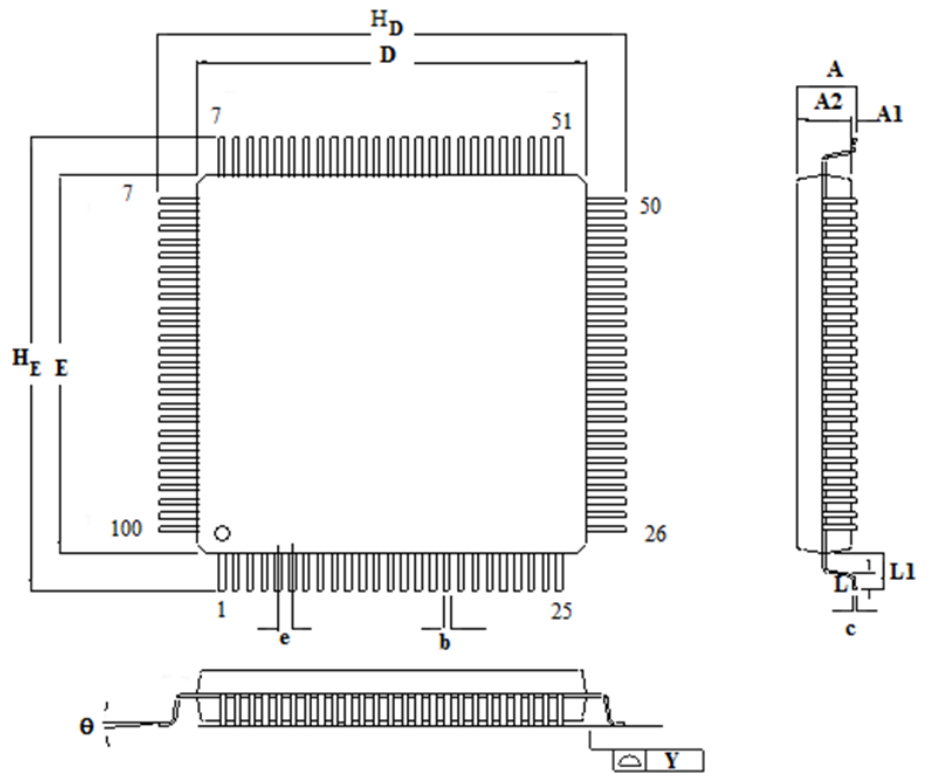
Symbol	Parameter	Min[3]	Typ	Max	Unit	Test Condition
V_{FLA}[1]	Supply voltage	-	1.8	-	V	T_A = 25℃
T_{ERASE}	Page erase time	-	21	-	mS	
$T_{MASS\ ERASE}$	Mass erase time	-	23	-	mS	
T_{PROG}	Program time	-	300	-	μS	
I_{DD2}	Program current	-	8	-	mA	
I_{DD3}	Erase current	-	12	-	mA	
N_{ENDUR}	Cycling Endurance	20,000	-	-	cycles[2]	T_J = -40℃~125℃
T_{RET}	Data retention	65	-	-	year	20 kcycle[2], T_J = 55℃
		10	-	-		20 kcycle[2], T_J = 85℃
		4	-	-		20 kcycle[2], T_J = 125℃

Notes:

1. V_{FLA} is source from chip internal LDO output voltage.
2. Number of program/erase cycles. The flash data can only be programmed once at the same address after flash erase.
3. Guaranteed by design.

9 PACKAGE DIMENSIONS

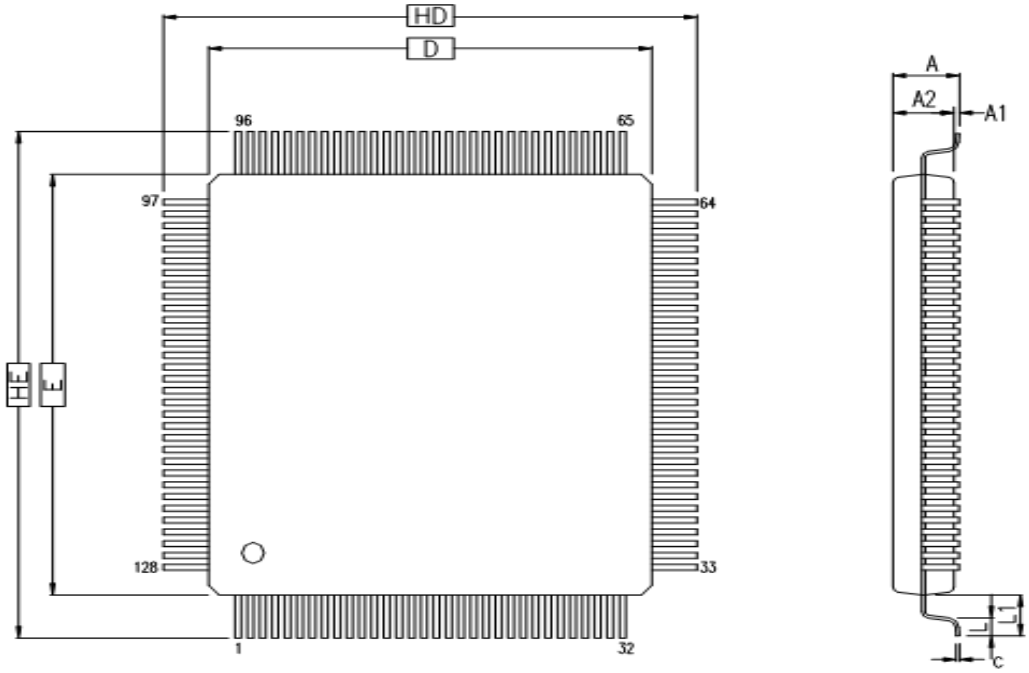
9.1 LQFP 100L (14x14x1.4 mm^3 footprint 2.0 mm)



Controlling Dimension : Millimeters

SYMBOLS	MIN.	NOM.	MAX.
A	-	-	1.60
A1	0.05	-	-
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.10	0.15	0.20
D	13.90	14.00	14.10
E	13.90	14.00	14.10
e	-	0.50	-
HD	15.80	16.00	16.20
HE	15.80	16.00	16.20
L	0.45	0.60	0.75
L1	-	1	-
y	-	-	0.10
θ	0°	-	7°

9.2 LQFP 128L (14x14x1.4 mm^3 footprint 2.0 mm)



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
y	-	-	0.1	-	-	0.004

10 ABBREVIATIONS

10.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
CCAP	Camera Capture Interface
DAP	Debug Access Port
DES	Data Encryption Standard
EADC	Enhanced Analog-to-Digital Converter
EBI	External Bus Interface
EMAC	Ethernet MAC Controller
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	12 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access

PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
QEI	Quadrature Encoder Interface
SD	Secure Digital
SPI	Serial Peripheral Interface
SPS	Samples per Second
TDES	Triple Data Encryption Standard
TK	Touch Key
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 10.1-1 List of Abbreviations

11 REVISION HISTORY

Date	Revision	Description
2020.09.15	1.00	1. Initial version.
2021.05.15	1.10	1. Added section 6.7 PDMA Controller (PDMA).
2021.06.15	1.20	1. Updated cover page. 2. Updated chapter 1 GENERAL DESCRIPTION. 3. Updated section 3.2 NuMicro® M471V/M471K Selection Guide. 4. Updated section 3.3 NuMicro® M471V/M471K Naming Rule. 5. Updated section 5.1 NuMicro® M471V/M471K Block Diagram.

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