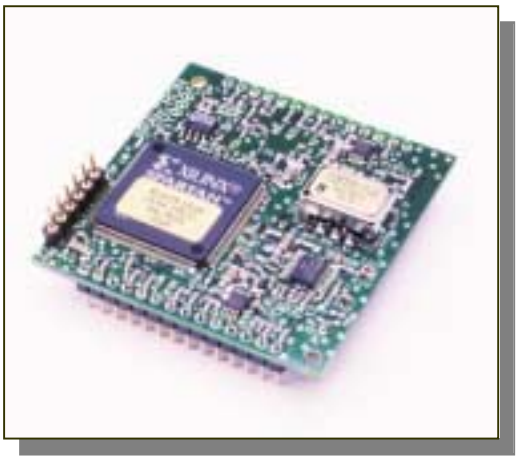
SY05-HF

Date: May 20, 2002



• INTRODUCTION

The SY05-HF is a high frequency clock that has been designed to be use at high speed Line Interface Cards in telecommunication products mainly related to STN-n or OC-n.

• FEATURES

√ A high frequency clock intended to be used at line cards for OC3 and OC12 (STM3 and STM12).

√ Along with SY0001 or SY0010 provides complete timing solution.

√ Provides very low jitter output signal.

√ Performs hitless switching between two reference signals.

√ Supports four timing modes: (1) Free-run, (2) Locked to Reference 1 (3) Locked to Reference 2, and (4) Loop back timing.

√ Accepts reference inputs from two clock sources – **8KHz~77.76MHz**

√ Provides up to 4 LVPECL outputs and two LVCMOS outputs **up to 777.6 MHz**. (or alternatively 5 LVPECL outputs)

√ Manual or Automatic selection between operating modes.

√ Alarm and status signals.

√ Complies with ITU-T Recommendations G.813, ETSI-ETS 300 462-4 and Bellcore GR-1244-CORE for Stratum 3 and 3E applications.

√ Small dimensions of 1.80 x 1.80 x 0.429 inch. (Without Metal Cover)

• APPLICATION

The SY05-HF high frequency clock can be used in ATM, SDH, PDH, and SONET networks devices. It is designed for manufacturers of network equipment, especially Access Switches, Core Switches, Cross Connects, Digital Multiplexers-Exchangers, and SDH/SONET equipment. The SY05-HF is a timing solution for Line Interface Cards.

RALTRON ELECTRONICS CORP. ▪ 10651 N.W.19th St ▪ Florida 33172 ▪ U.S.A.
Tel: 305 593-6033 ▪ Fax: 305-594-3973 ▪ e-mail: sales@raltron.com ▪ Internet: http://www.raltron.com

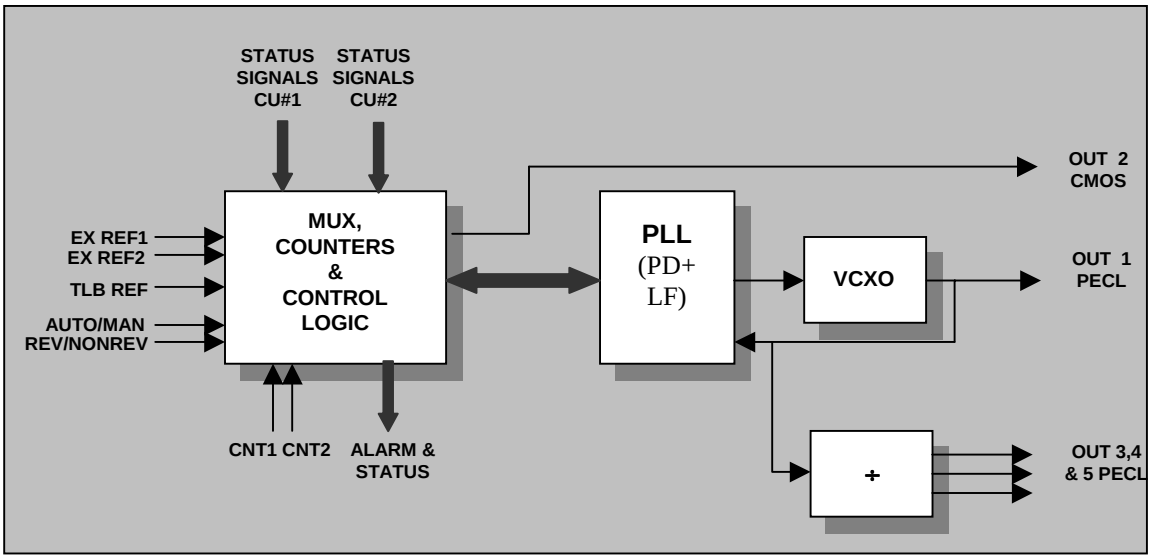


Figure 1. - The functional block diagram of SY05-HF

- **DESCRIPTION**

The SY05-HF synchronization module is a high frequency PLL that performs hitless switching plus additional features necessary for timing at high-speed Line Interface Cards. The functional block diagram is shown in figure 1. The SY05-HF receives two reference signals, usually 19.44MHz and using PLL synthesizer generates a high frequency signal necessary for transceivers or framers. The PLL that is complemented by high-speed logic that provide processing, switching between the timing modes, alarm and status messages and etc. A high quality VCXO provides very low jitter at the output. The additional outputs are provided using a divider.

The module supports two operating modes: AUTO mode is the mode where all switching are done automatically and MANUAL mode is where unit will switch according to the two external control pins CON1 and CON2.

CON1	CON2	Operational mode
0	0	Free-run (Unlocked)
1	0	Locked to EX REF 1
0	1	Locked to EX REF 2
1	1	Locked to TLB REF

The module operates in the following four timing modes: 1) Free-run, 2) Locked to EX REF1, 3) Locked to EX REF2 and 4) Locked to TBL REF. Free-run it a mode the unit is unlocked to either of the inputs. The accuracy of the output frequencies in this mode is equal to the accuracy of free running VCXO. Locked to EX REF 1 is the mode where the output of the module is phase locked to input reference 1. Locked to EX REF 2 is the mode where the output of the module is phase locked to input reference 2, Locked to TBL REF is the mode where is the output of the module is phase locked to the signal used in Time Loop-back operation.

- **SPECIFICATIONS**

General Specifications	Mechanical	1.82" (D) x 1.82" (W) x 0.518" (H) 1.8" (D) x 1.8" (W) x 0.429" (H)	Metal Box Module on PCB
	Power Supply Current Supply Operating Temperature Humidity Internal Oscillators	+3.3VDC 200mA max -40°C to 80°C 5% to 95% non-condensing VCXO or SAW	
Input Signals	Number of Inputs	2	
	Input reference frequency Signal Level	8KHz~77.76MHz HCMOS 3.3V / 5V I/O tolerant	
	Time Reference characteristics		As output of SY0001/SY0010
Output Signal	Number of Outputs	6/5	
	Output 1	51.84MHz~777.600MHz	.
	Signal type	Low Voltage differential PECL	
	Duty Cycle @ Output 1	50/50% ±5%	
	Output 2	Buffered Input/Synch Out 1	
	Signal type	HCMOS 3.3V / 5V I/O tolerant	Low Voltage differential PECL (in cases of Synch Out 1)
	Duty Cycle @ Output 2	50/50% ±5%	
	Output 3	Out 1 Divide by 2	
	Signal type	Low Voltage differential PECL	
	Duty Cycle @ Output 3	50/50% ±5%	
	Output 4	Out 1 Divid by 4	
	Signal type	Low Voltage differential PECL	
	Duty Cycle @ Output 4	50/50% ±5%	
	Output 5	Out 1 divid by 8	
	Duty Cycle @ Output 5	Low Voltage differential PECL	
	Signal Type	50/50% ±5%	
	Output 6	Buffered Input/Synch Out 1 (Complimentary)	Low Voltage differential PECL (in cases of Synch Out 1 - Complimentary)
	Signal type	HCMOS 3.3V / 5V I/O tolerant	
	Duty Cycle @ Output 6	50/50% ±5%	
Signal Quality Performance	Jitter Tolerance		Bellcore: GR-1244-R4-4, ITU-T: G.812
	Phase Transient Tolerance		Bellcore: GR-1244-R4-7
	Jitter Generation and Transfer		Bellcore: GR-1244-R5-7, ITU-T: G.812
Frequency Output Performance	Pull-In Range	±50ppm	
	MTIE		Bellcore: GR-1244-R5-5, ITU-T: G.812
	TDEV		Bellcore: GR-1244-R5-4, ITU-T: G.812
	Jitter @ OUT 1	<1ps RMS	Within the BW 10kHz to 20MHz
	Phase Transient MTIE Mask		GR1244 R5-14
Stability	Free run	±50ppm	Over operating temperature range

- **PIN ASSIGNMENT**

On the picture below it is shown the pin-out for the SY05-HF. For other pin-out requirement please contact the Raltron.

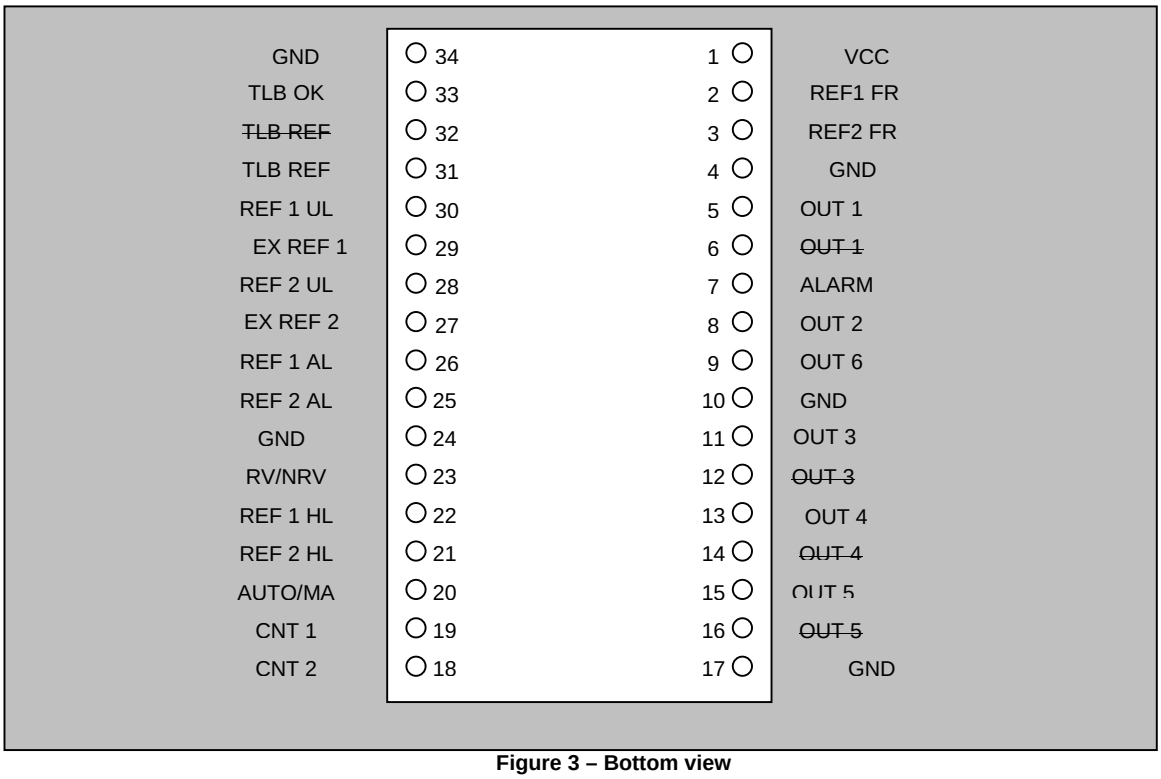


Figure 3 – Bottom view

Pin #	Name	Description	Signal Technology	VL			VH/ DC Voltage		
				Min	Typ	Max	Min	Typ	Max
1	+Vcc	Positive Voltage Supply	DC	-----	-----	-----	4.75** (3.135)	5.0** (3.3)	5.25** (3.465)
2	REF1 FR	Reference 1 Freerun Input -> the signal High (“1” logic) FREERUN comes from Clock Unit 1	DC	0	0.25 ** (0.15)	0.5** (0.3)	4.5** (2.97)	5.0** (3.3)	5.25** (3.465)
3	REF2 FR	Reference 2 Freerun Input -> the signal High (“1” logic) FREERUN comes from Clock Unit 2	DC	0	0.25 ** (0.15)	0.5** (0.3)	4.5** (2.97)	5.0** (3.3)	5.25** (3.465)
4	GND	Ground	-----	-----	-----	----	------	------	------
5	OUT 1	Synchronized Output 1 -> the output of the synchronized signal.	LV/PECL	Vcc-1.680	Vcc-1.620	Vcc-1.56	Vcc-1.085	Vcc-1.025	Vcc-0.88
6	~~OUT 1~~	Synchronized Complementary Output 1 -> the output of the synchronized signal.	LV/PECL	Vcc-1.680	Vcc-1.620	Vcc-1.56	Vcc-1.085	Vcc-1.025	Vcc-0.88
7	ALARM	Alarm signal out -> the output is high when the module is unlocked (“1” logic)	DC	0	0.25 (0.15)	0.5 (0.3)	4.5 (2.97)	5.0 (3.3)	5.25 (3.465)
8	OUT 2	Buffered reference or synchronized signal Output 2 -> a buffered external reference Signal (LVCMOS) or a buffered synchronized local oscillator signal. (LVPECL)	HCMOS (3.3 Tolerable) LV/PECL	0 ----- Vcc-1.680	0.5** (0.3) Vcc-1.620	4.5** Vcc-1.56	(2.97) Vcc-1.085	---- Vcc-1.025	---- Vcc-0.88
9	OUT 6	Buffered reference or synchronized complimentary signal Output 6 -> a buffered external reference Signal (LVCMOS) or a buffered synchronized local oscillator signal. (LVPECL- complimentary).	HCMOS (3.3 Tolerable) LV/PECL	0 ----- Vcc-1.180	0.5** (0.3) Vcc-1.135	4.5** Vcc-0.975	(2.97) Vcc-1.085	---- Vcc-1.025	---- Vcc-0.880
10	GND	Ground	-----	-----	-----	----	------	------	------
11	OUT 3	Divider Output 3 -> the output of the synchronized signal divided by 2;	LV/PECL	Vcc-1.680	Vcc-1.620	Vcc-1.56	Vcc-1.085	Vcc-1.025	Vcc-0.88
12	~~OUT 3~~	Complementary Divider Output 3 -> the output of the synchronized signal divided by 2	LV/PECL	Vcc-1.680	Vcc-1.620	Vcc-1.56	Vcc-1.085	Vcc-1.025	Vcc-0.88
13	OUT 4	Divider Output 4 -> the output of the synchronized signal divided by 4.	LV/PECL	Vcc-1.680	Vcc-1.620	Vcc-1.56	Vcc-1.085	Vcc-1.025	Vcc-0.88
14	~~OUT 4~~	Complementary Divider Output 4 -> the output of the synchronized signal divided by 4. –	LV/PECL	Vcc-1.680	Vcc-1.620	Vcc-1.56	Vcc-1.085	Vcc-1.025	Vcc-0.88
15	OUT 5	Divider Output 5 -> the output of the synchronized signal divided by 8;	LV/PECL	Vcc-1.680	Vcc-1.620	Vcc-1.56	Vcc-1.085	Vcc-1.025	Vcc-0.88
16	~~OUT 5~~	Complementary Divider Output 5 -> the output of the synchronized signal divided by 8;	LV/PECL	Vcc-1.680	Vcc-1.620	Vcc-1.56	Vcc-1.085	Vcc-1.025	Vcc-0.88
17	GND	Ground	-----	-----	-----	----	------	------	------
18	CNT 2	Control Input 2 -> the external input for selecting mode of the unit – see table.	DC	0	0.25 ** (0.15)	0.5** (0.3)	4.5** (2.97)	5.0** (3.3)	5.25** (3.465)
19	CNT 1	Control Input 1 -> the external input for selecting mode of the unit – see table.	DC	0	0.25 ** (0.15)	0.5** (0.3)	4.5** (2.97)	5.0** (3.3)	5.25** (3.465)
20	AUTO/MAN	Auto/Manual configuration input -> selection input for operating mode Man=”0” ; Auto = “1”	DC	0	0.25 ** (0.15)	0.5** (0.3)	4.5** (2.97)	5.0** (3.3)	5.25** (3.465)
21	REF2 HL	Reference 2 Holdover Input -> the signal High (“1” logic) HOLDOVER comes from Clock Unit 2	DC	0	0.25 ** (0.15)	0.5** (0.3)	4.5** (2.97)	5.0** (3.3)	5.25** (3.465)
22	REF1 HL	Reference 1 Holdover Input -> the signal High (“1” logic) HOLDOVER comes from Clock Unit 1	DC	0	0.25 ** (0.15)	0.5** (0.3)	4.5** (2.97)	5.0** (3.3)	5.25** (3.465)
23	RV/NRV	Revert / Non revert input-> selection input for revert feature Revertive-“1” ; Non-Revertive = “0”	DC	0	0.25 ** (0.15)	0.5** (0.3)	4.5** (2.97)	5.0** (3.3)	5.25** (3.465)
24	GND	Ground	-----	-----	-----	----	------	------	------
25	REF2 AL	Reference 2 Alarm Input -> the signal High (“1” logic) ALARM OUT comes from Clock Unit 2	DC	0	0	0.25 ** (0.15)	0.5** (0.3)	4.5** (2.97)	5.0** (3.3)
26	REF1 AL	Reference 1 Alarm Input -> the signal High (“1” logic) ALARM OUT comes from Clock Unit 1	DC	0	0	0.25 ** (0.15)	0.5** (0.3)	4.5** (2.97)	5.0** (3.3)
27	EX REF 2	External Reference 2 Input -> the input signal from reference 2	HCMOS (3.3 Tolerable)	0	-----	0.5** (0.3)	4.5** (2.97)	----	----
28	REF2 UL	Reference 2 Unlocked Input -> the signal High (“1” logic) PLL UNLOCK comes from Clock Unit 2	DC	0	0.25 ** (0.15)	0.5** (0.3)	4.5** (2.97)	5.0** (3.3)	5.25** (3.465)
29	EX REF 1	External Reference 1 Input -> the input signal from reference 1	HCMOS (3.3 Tolerable)	0	-----	0.5** (0.3)	4.5** (2.97)	----	----
30	REF1 UL	Reference 1 Unlocked Input -> the signal High (“1” logic) PLL UNLOCK comes from Clock Unit 1	DC	0	0.25 ** (0.15)	0.5** (0.3)	4.5** (2.97)	5.0** (3.3)	5.25** (3.465)
31	TLB REF	Time Loop back Reference Input -> the input from time loopback	LV/PECL	Vcc-1.680	Vcc-1.620	Vcc-1.56	Vcc-1.085	Vcc-1.025	Vcc-0.88
32	~~TLB REF~~	Time Loop back Complementary Input -> the complementary input from time loopback	LV/PECL	Vcc-1.680	Vcc-1.620	Vcc-1.56	Vcc-1.085	Vcc-1.025	Vcc-0.88
33	TLB OK	Time Loop back OK (nput -> When high (“1” logic) the loop back reference is valid for use	DC	0	0.25 ** (0.15)	0.5** (0.3)	4.5** (2.97)	5.0** (3.3)	5.25** (3.465)
34	GND	Ground	-----	-----	-----	----	------	------	------

For other pin-out configurations contact the factory!

**** Indicates corresponding values to Vcc=5V

- **ORDERING INFORMATION**

Please contact factory with input/output options for P/N assiagnment.

- **MECHANICAL DIMENSIONS**

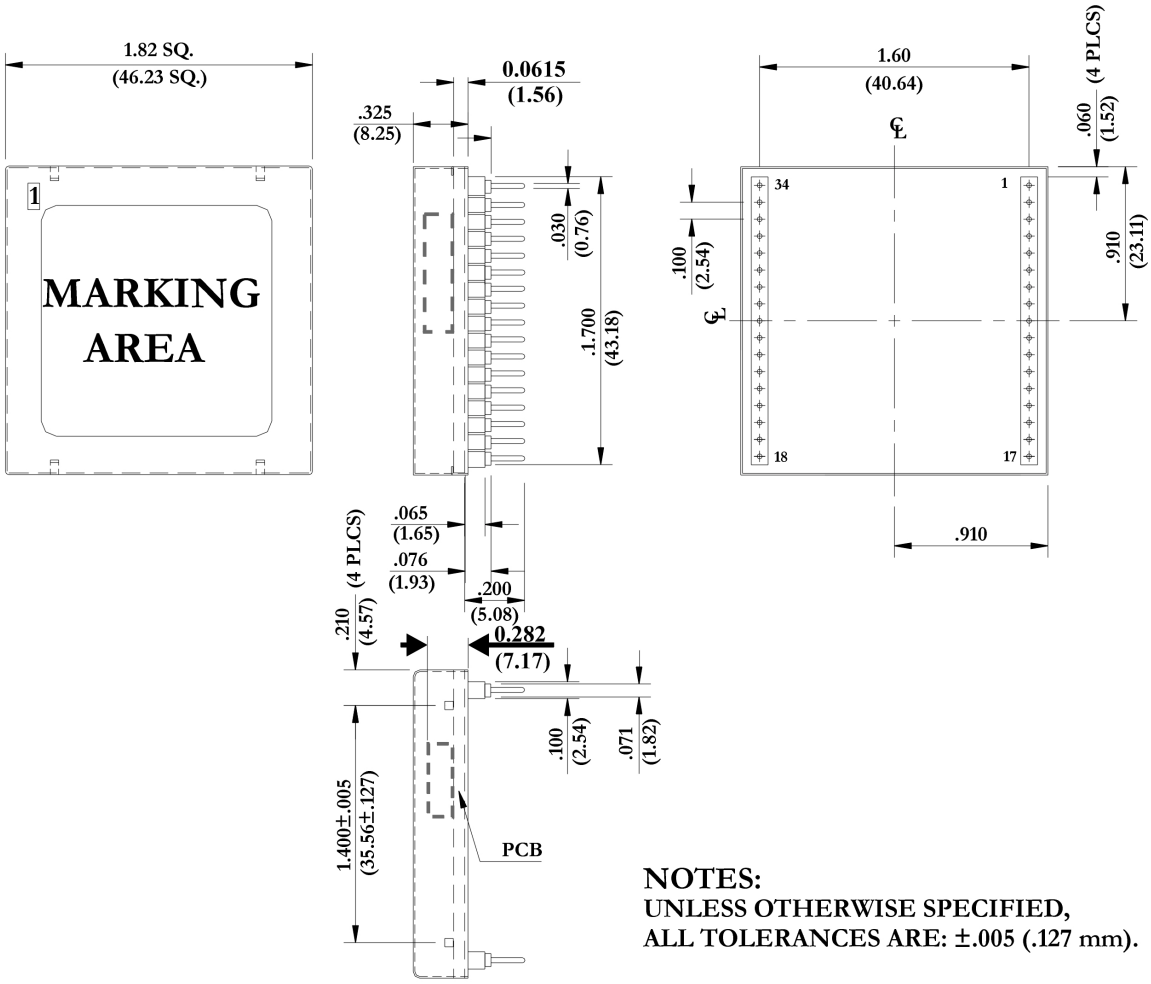


Figure 4 – The mechanical dimensions.

Figure 4 shows the mechanical dimension of the SY05-HF-HF module. The module can be supplied in two different types of packaging:

- ✓ Metal box
- ✓ Module without packaging

The dimensions shown on the picture are valid for first and second type of packaging, the actual dimensions for the first type are 1.82 x 1.82 x 0.518" keeping the pin-out dimensions the same for all of three. The label on the module shows part number, factory name, week and year of production.