

## 9X14 PECL J-LEAD CLOCK- PB FREE COMPLIANT (SEE PAGE TWO FOR PART NUMBERING SCHEME)

### ■ APPROVALS

RALTRON	CUSTOMER
Eng. approval, date: RONEN 3/20/03	Name (please print):
Sales approval, date:	Title (please print):
Created by, date: RONEN 3/20/03	Signature, date:
Revision:	

### ■ MECHANICAL SPECIFICATION

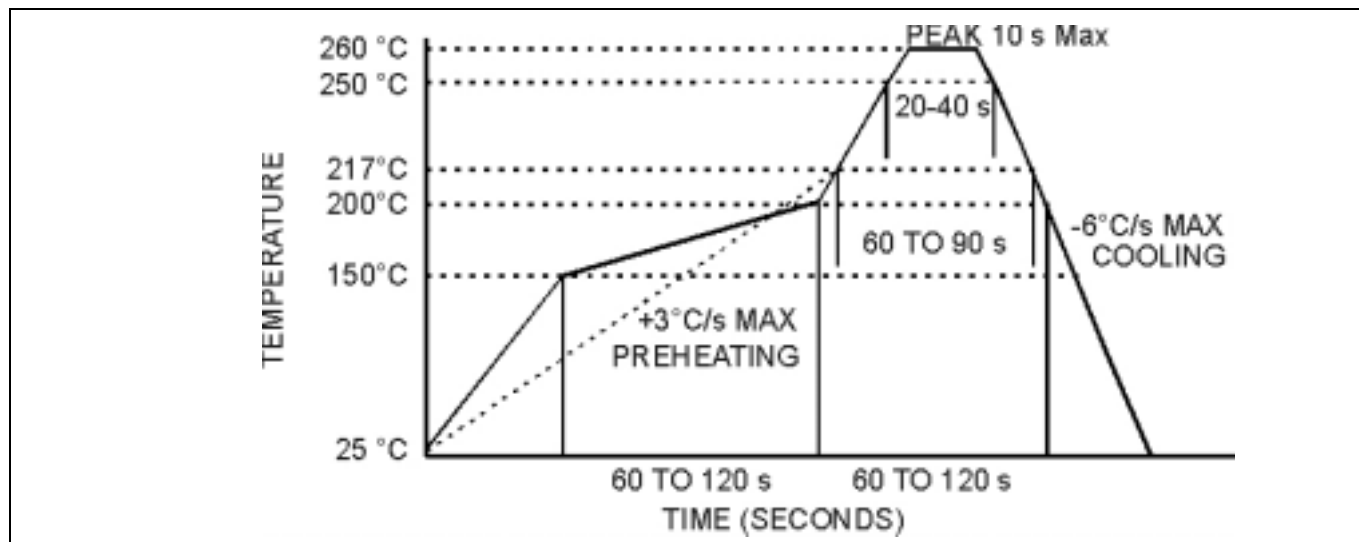
6 pin Version	4 pin Version	OUTLINE TOLERANCE: ±0.015" / 0.4mm (Unless otherwise specified)
		<p><b>PIN FUNCTIONS (6 pins):</b>                      [1] NC OR COMP. OUTPUT                      [2] EN / DIS OR NC                      [3] CASE / GROUND                      [4] OUTPUT                      [5] COMP. OUTPUT OR NC                      [6] SUPPLY VOLTAGE</p> <p><b>PIN FUNCTIONS (4 pins):</b>                      [1] E / D OR N/C OR COMP. OUT                      [2] CASE / GROUND                      [3] OUTPUT                      [4] SUPPLY VOLTAGE</p> <p><b>MARKING (EXAMPLE):</b>                      CE8950A-LZ                      155.520-T-C-EL                      RAL D/C</p>

### ■ ELECTRICAL SPECIFICATION

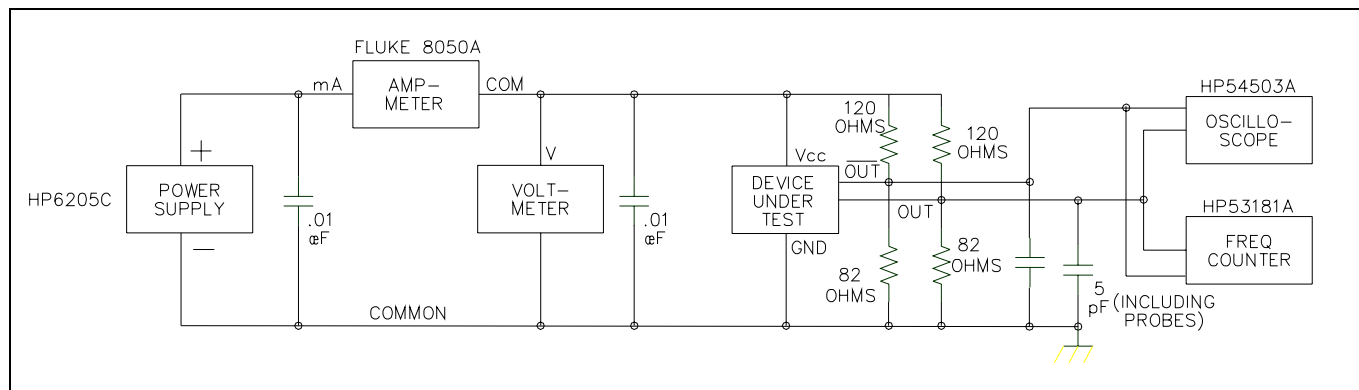
PARAMETER	SYMBOL	CONDITIONS	VALUE		UNIT
Frequency, nom	fo	-	70.000~250.0		MHz
Supply voltage, nom.	Vcc	Vcc±5%	3.3VDC	5.0VDC	V
Supply current, max. (excluding load)	Is	Vcc=+3.3VDC/+5.0VDC Ta=+25°C, 50Ω to Vcc-2.0VDC load	100		mA
PECL output level	VOH / VOL	Vcc=+3.3VDC/+5.0VDC load=50Ω to Vcc-2.0VDC	2.275 / 1.68	3.975/3.38	V
Duty cycle	DC	load=50Ω to Vcc-2.0VDC / @50%Vcc, Ta=+25°C	40...60 OR 45...55		%
Rise- / fall time, max.	tr / tf	20%~80% Vout, 80%~20% Vout, max	0.100...1.0 (see note A)		ns
Jitter, rms, max.	J	1σ, Fj=12KHz...20MHz	1.0		ps
Overall freq. stability, max.	Δf/fc	Including operating temperature, ±5% load & supply variations, calibration @+25°C, and 10 year aging	SEE PART NUMBER GENERATION TABLE		ppm
Enable option	En	Pin 2=Low, Vcc-1.620 (max.)	Enabled		-
Disable option	Dis	Pin 2=High, Vcc-1.025 (min.)	Pin 4 will assume a fixed level of logic "0", and pin 5 will assume a fixed level of logic "1"		-
Operating temperature range	Ta	-	SEE PART NUMBER GENERATION TABLE		°C
Storage temperature range	T(stg)	-	-55...+90		°C
Absolute voltage range	Vcc(abs)	Non-destructive, DC	-0.5...+7.0		V

3/20/03 marketing-rfq, clock

NOTE A: RISE AND FALL TIME VALUES (tr/tf) ARE FREQUENCY DEPENDENT.



■ ELECTRICAL TEST DIAGRAM FOR 3.3V PECL CLOCK WITH COMP. OUTPUT



■ PART NUMBER GENERATION

SERIES	OVERALL STABILITY	REV	TEMP. RANGE (°C)	FREQUENCY (MHz)	OPTIONS	SUFFIX	PIN SUFIX OPTION
CO88: 5.0V PECL, NO EN/DIS CO89: 3.3V PECL, NO EN/DIS CE88: 5.0V PECL, EN/DIS CE89: 3.3V PECL, EN/DIS	50: ±50ppm 00: ±100ppm	A	LV: 0...+50 LZ: 0...+70 HZ: -20...+70 D3: -40...+85	70.000...250.0	T: 45...55 DUTY C: COMP. OUTPUT C1: COMP. OUTPUT PIN 1 (See Note 3)	EL (See note 2)	4: 4 PINS

NOTE:

5/13/02rketing-rfq, vxco

- Variations from standard specification are available, please contact factory.
- EL is added at the end of the part number for all PECL clocks with enable/disable option.
- C1 suffix to be applied only when using the 6 pins package version

PART NUMBER EXAMPLE: CE8950A-LZ-155.520-T-C-EL