ARM® Cortex®-M0

32-bit Microcontroller

NuMicro® Family
NUC122 Series
Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

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1 GENERAL DESCRIPTION

The NuMicro® NUC122 Series are 32-bit microcontrollers with Cortex®-M0 core runs up to 72 MHz, up to 64 K-byte embedded flash, 8 K-byte embedded SRAM, and 4 K-byte loader ROM for the In System Program (ISP) function. It also integrates Timers, Watchdog Timer, RTC, UART, SPI, I^2C, PWM Timer, GPIO, USB 2.0 Full Speed Device, Low Voltage Reset Controller and Brownout Detector.

Product Line	UART	SPI	I^2C	USB	LIN	CAN	PS/2	I^2S
NUC122	•	•	•	•			•	

Table 1-1 Connectivity Support Table

2 FEATURES

2.1 NuMicro® NUC122 Series Features – USB Line

- ARM® Cortex®-M0 core
  - Runs up to 72 MHz
  - One 24-bit system timer
  - Supports low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-levels of priority
  - Serial Wire Debug supports with 2 watchpoints/4 breakpoints
- Built-in LDO for wide operating voltage ranges from 2.5V to 5.5V
- Flash Memory
  - 32 K/64 K bytes Flash for program code
  - 4 KB flash for ISP loader
  - Supports In-System Program (ISP) application code update
  - 512 byte page erase for flash
  - 4 KB data flash
  - Supports 2 wire ICP update through SWD/ICE interface
  - Supports fast parallel programming mode by external programmer
- SRAM Memory
  - 4 K/8 K bytes embedded SRAM
- Clock Control
  - Flexible selection for different applications
  - Built-in 22.1184 MHz high speed OSC for system operation
    - Trimmed to ± 1 % at +25 ℃ and V_{DD} = 5 V
    - Trimmed to ± 3 % at -40 ℃ ~ +85 ℃ and V_{DD} = 2.5 V ~ 5.5 V
  - Built-in 10 kHz low speed OSC for Watchdog Timer and Wake-up operation
  - Supports one PLL, up to 72 MHz, for high performance system operation
  - External 4~24 MHz high speed crystal input for USB and precise timing operation
  - External 32.768 kHz low speed crystal input for RTC function and low power system operation
- GPIO
  - Four I/O modes:
    - Quasi bi-direction
    - Push-pull output
    - Open-drain output
    - Input only with high impendence
  - TTL/Schmitt trigger input selectable
  - I/O pin configured as interrupt source with edge/level setting
  - High driver and high sink I/O mode support
- Timer
  - Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
  - Independent clock source for each timer
  - Provides one-shot, periodic, toggle and continuous counting operation modes
  - Supports event counting function
- Watchdog Timer
  - Multiple clock sources
  - 8 selectable time out period from 1.6 ms ~ 26.0 sec (depending on clock source)
  - Wake-up from Power-down or Idle mode

- Interrupt or reset selectable on watchdog time-out

- RTC
  - Supports software compensation by setting frequency compensate register (FCR)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition
  - Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
  - Support wake-up function
- PWM/Capture
  - Up to two built-in 16-bit PWM generators providing four PWM outputs or two complementary paired PWM outputs
  - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit prescaler and one Dead-Zone generator for complementary paired PWM
  - Up to four 16-bit digital capture timers (shared with PWM timers) providing four rising/falling capture inputs
  - Supports Capture interrupt
- UART
  - Up to two UART controllers
  - UART ports with flow control (TXD, RXD, CTS and RTS)
  - UART ports with 14-byte FIFO for standard device
  - Supports IrDA (SIR) function
  - Supports RS-485 9-bit mode and direction control
  - Programmable baud-rate generator (up to 1/16 system clock)
- SPI
  - Up to two sets of SPI controllers
  - Master up to 24 MHz, and Slave up to 12 MHz (chip working at 5V)
  - Supports SPI Master/Slave mode
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 1 to 32 bits
  - MSB or LSB first data transfer
  - Rx and Tx on both rising or falling edge of serial clock independently
  - Two slave/device select lines in Master mode, and 1 slave/device select line in Slave mode
  - Supports Byte Suspend mode in 32-bit transmission
- I^2C
  - One set of I^2C device
  - Master/Slave mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allow versatile rate control
  - Supports multiple address recognition (four slave address with mask option)
- PS/2 Device Controller
  - Host communication inhibit and request to send detection

  - Reception frame error detection
  - Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
  - Double buffer for data reception
  - S/W override bus
- USB 2.0 Full-Speed Device
  - One set of USB 2.0 FS Device 12 Mbps
  - On-chip USB Transceiver
  - Provides 1 interrupt source with 4 interrupt events
  - Supports Control, Bulk In/Out, Interrupt and Isochronous transfers
  - Auto suspend function when no bus signaling for 3 ms
  - Provides 6 programmable endpoints
  - Includes 512 Bytes internal SRAM as USB buffer
  - Provides remote wake-up capability
- Brown-out detector
  - With 4 levels: 4.5 V/3.8 V/2.7 V/2.2 V
  - Support Brown-out Interrupt and Reset option
- Low Voltage Reset
  - Threshold voltage levels: 2.0 V
- Operating Temperature: -40 ℃~85 ℃
- Packages:
  - All Green package (RoHS)
  - LQFP 64-pin (7x7mm)
  - LQFP 48-pin
  - QFN 33-pin

3 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~20 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
QEI	Quadrature Encoder Interface
SD	Secure Digital
SPI	Serial Peripheral Interface

SPS	Samples per Second
TDES	Triple Data Encryption Standard
TK	Touch Key
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 3-1 List of Abbreviations

4 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.1 NuMicro® NUC122 Series Naming Rule

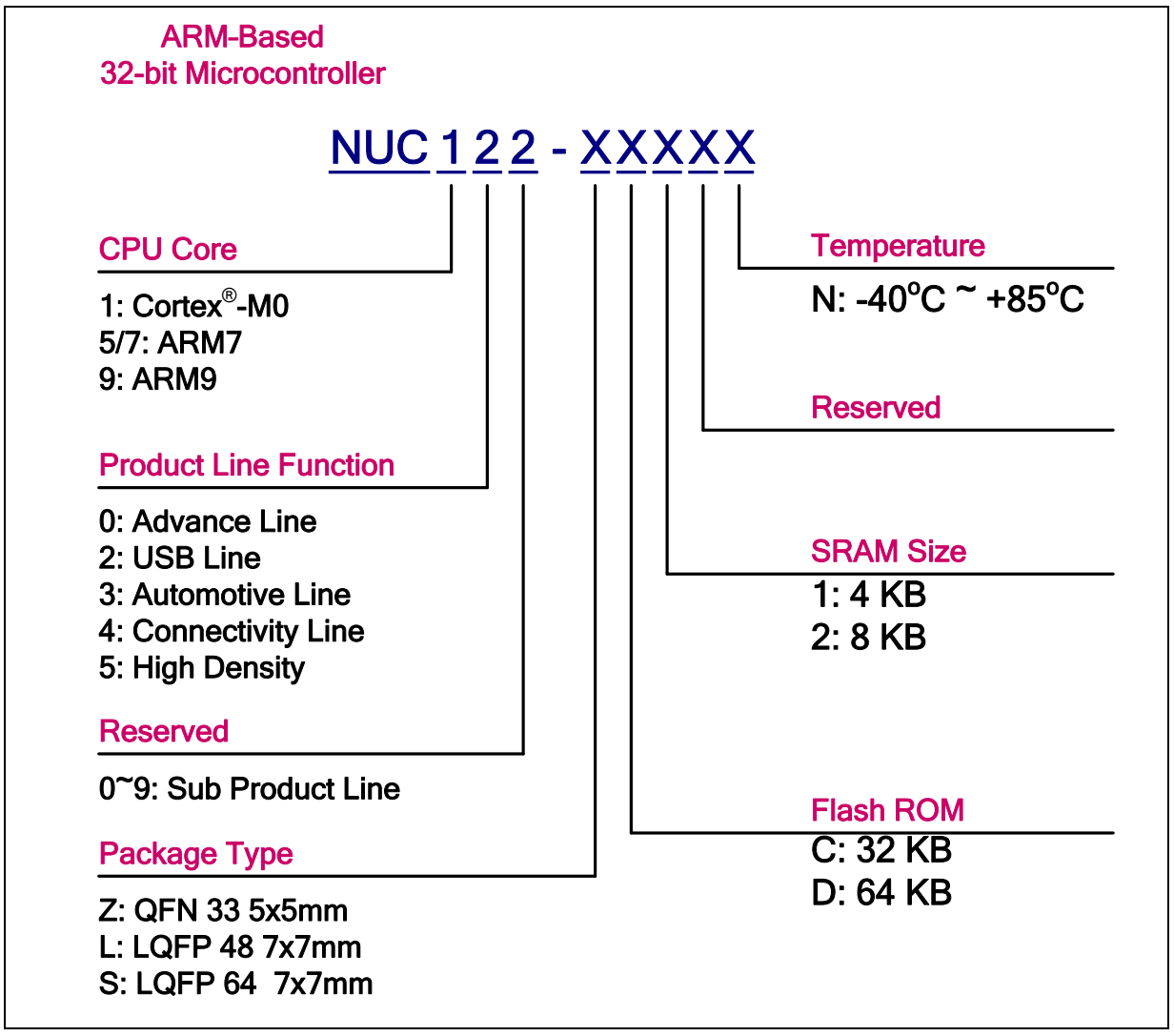


Figure 4-1 NuMicro® NUC122 Series Selection Code

4.2 PARTS INFORMATION LIST AND PIN CONFIGURATION

4.2.1 NuMicro® NUC122 Series Selection Guide

Part Number	Flash (KB)	SRAM (KB)	ISP ROM (KB)	I/O	Timer	Connectivity						I^2S	Comp.	PWM	ADC	RTC	EBI	ISP\ICP\IAP	Package
						UART	SPI	I^2C	USB	LIN	PS/2								
NUC122ZC1DN	32	4	4	Up to 18	4x32-bit	1	2	1	1	-	-	-	-	-	-	-	-	v	QFN33
NUC122ZD2DN	64	8	4	Up to 18	4x32-bit	1	2	1	1	-	-	-	-	-	-	-	-	v	QFN33
NUC122LC1DN	32	4	4	Up to 32	4x32-bit	2	2	1	1	-	1	-	-	4	-	v	-	v	LQFP48
NUC122LD2DN	64	8	4	Up to 32	4x32-bit	2	2	1	1	-	1	-	-	4	-	v	-	v	LQFP48
NUC122SC1DN	32	4	4	Up to 43	4x32-bit	2	2	1	1	-	1	-	-	4	-	v	-	v	LQFP64*
NUC122SD2DN	64	8	4	Up to 43	4x32-bit	2	2	1	1	-	1	-	-	4	-	v	-	v	LQFP64*

LQFP64* : 7x7mm

4.3 NuMicro® NUC122 Series Pin Configuration

4.3.1 NuMicro® NUC122 Series Pin Diagram

4.3.1.1 NuMicro® NUC122 LQFP 64 pin

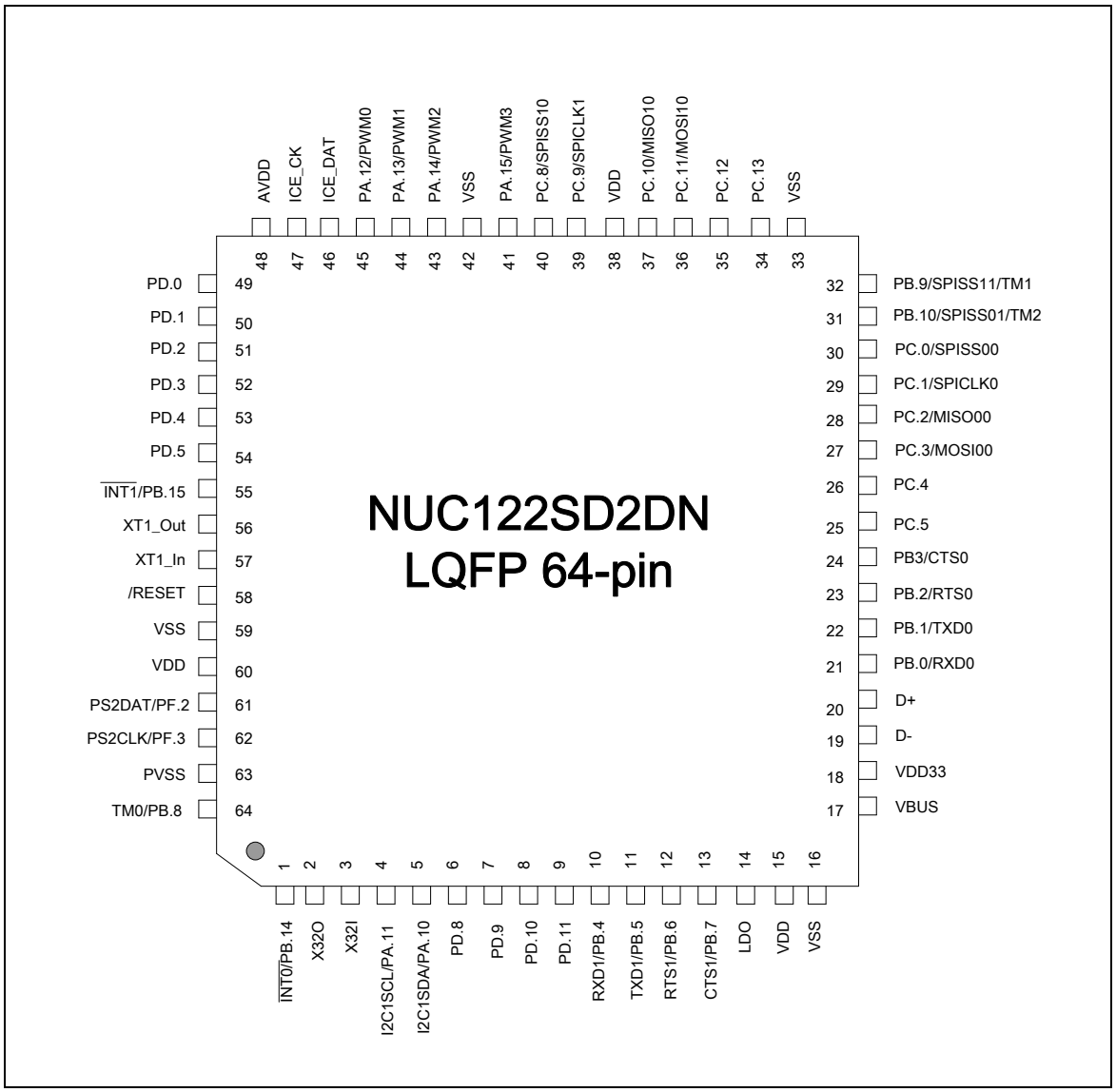


Figure 4-2 NuMicro® NUC122 LQFP 64-pin Diagram

4.3.1.2 NuMicro® NUC122 LQFP 48 pin

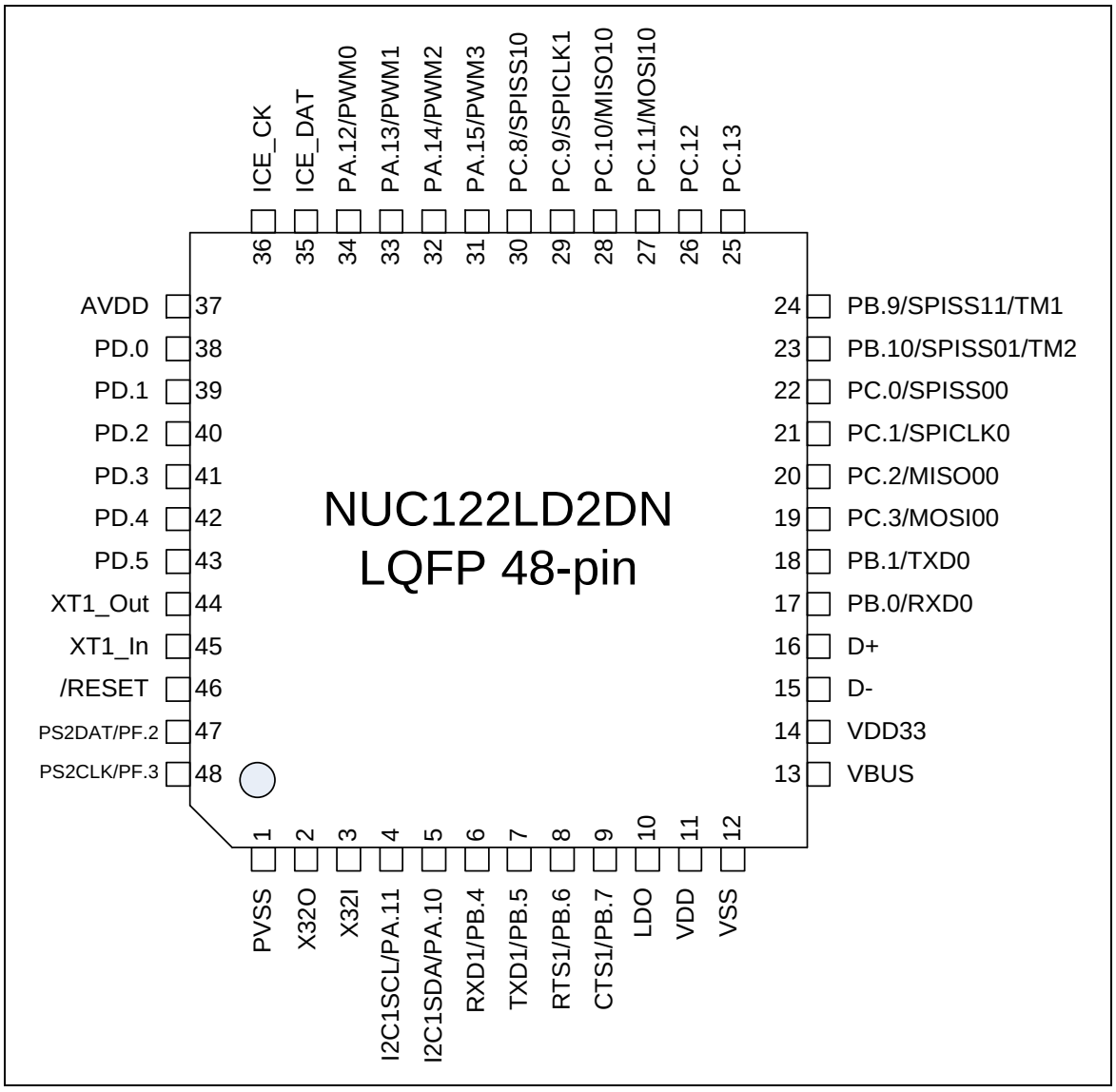


Figure 4-3 NuMicro® NUC122 LQFP 48-pin Diagram

4.3.1.3 NuMicro® NUC122 QFN 33 pin

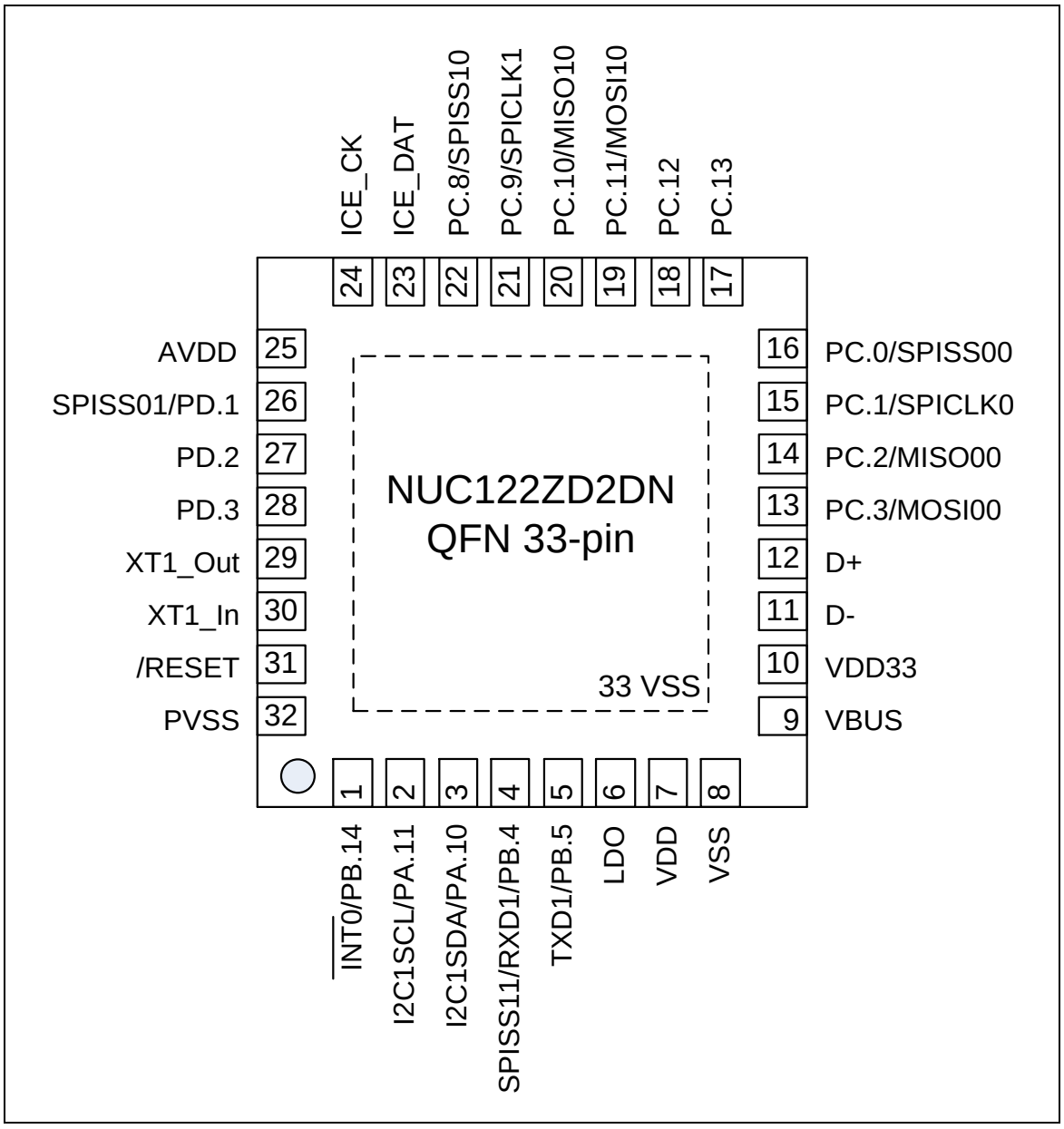


Figure 4-4 NuMicro® NUC122 QFN 33-pin Diagram

4.4 Pin Description

4.4.1 NuMicro® NUC122 Series Pin Description

Pin No.			Pin Name	Pin Type	Description
LQFP 64	LQFP 48	QFN 33			
1		1	PB.14	I/O	General purpose input/output digital pin
			/INT0	I	/INT0: External interrupt1 input pin
2	2		X32O	O	32.768 KHz low speed crystal output pin
3	3		X32I	I	32.768 KHz low speed crystal input pin
4	4	2	PA.11	I/O	General purpose input/output digital pin
			I2C1SCL	I/O	I2C1SCL: I^2C1 clock pin
5	5	3	PA.10	I/O	General purpose input/output digital pin
			I2C1SDA	I/O	I2C1SDA: I^2C1 data input/output pin
6			PD.8	I/O	General purpose input/output digital pin
7			PD.9	I/O	General purpose input/output digital pin
8			PD.10	I/O	General purpose input/output digital pin
9			PD.11	I/O	General purpose input/output digital pin
10	6	4	PB.4	I/O	General purpose input/output digital pin
			RXD1	I	RXD1: Data receiver input pin for UART1
			SPISS11	I/O	SPISS11: SPI1 2nd slave select pin (for QFN33 only)
11	7	5	PB.5	I/O	General purpose input/output digital pin
			TXD1	O	TXD1: Data transmitter output pin for UART1
12	8		PB.6	I/O	General purpose input/output digital pin
			RTS1	O	RTS1: Request to Send output pin for UART1
13	9		PB.7	I/O	General purpose input/output digital pin
			CTS1	I	CTS1: Clear to Send input pin for UART1
14	10	6	LDO	P	LDO output pin
15	11	7	VDD	P	Power supply for I/O ports and LDO source for internal PLL and digital function
16	12	8	VSS	P	Ground
17	13	9	VBUS	P	POWER SUPPLY: From USB Host or HUB.
18	14	10	VDD33	P	Internal Power Regulator Output 3.3 V Decoupling Pin

Pin No.			Pin Name	Pin Type	Description
LQFP 64	LQFP 48	QFN 33			
19	15	11	D-	**USB**	USB Differential Signal D-
20	16	12	D+	**USB**	USB Differential Signal D+
21	17		PB.0	**I/O**	General purpose input/output digital pin
			RXD0	**I**	RXD0: Data Receiver input pin for UART0
22	18		PB.1	**I/O**	General purpose input/output digital pin
			TXD0	**O**	TXD0: Data transmitter output pin for UART0
23			PB.2	**I/O**	General purpose input/output digital pin
			RTS0	**O**	RTS0: Request to Send output pin for UART0
24			PB.3	**I/O**	General purpose input/output digital pin
			CTS0	**I**	CTS0: Clear to Send input pin for UART0
25			PC.5	**I/O**	General purpose input/output digital pin
26			PC.4	**I/O**	General purpose input/output digital pin
27	19	13	PC.3	**I/O**	General purpose input/output digital pin
			MOSI00	**O**	MOSI00: SPI0 MOSI (Master Out, Slave In) pin
28	20	14	PC.2	**I/O**	General purpose input/output digital pin
			MISO00	**I**	MISO00: SPI0 MISO (Master In, Slave Out) pin
29	21	15	PC.1	**I/O**	General purpose input/output digital pin
			SPICLK0	**I/O**	SPICLK0: SPI0 serial clock pin
30	22	16	PC.0	**I/O**	General purpose input/output digital pin
			SPISS00	**I/O**	SPISS00: SPI0 slave select pin
31	23		PB.10	**I/O**	General purpose input/output digital pin
			TM2	**O**	TM2: Timer2 external counter input
			SPISS01	**I/O**	SPISS01: SPI0 2nd slave select pin
32	24		PB.9	**I/O**	General purpose input/output digital pin
			TM1	**O**	TM1: Timer1 external counter input
			SPISS11	**I/O**	SPISS11: SPI1 2nd slave select pin
33			VSS	**P**	Ground
34	25	17	PC.13	**I/O**	General purpose input/output digital pin
35	26	18	PC.12	**I/O**	General purpose input/output digital pin
36	27	19	PC.11	**I/O**	General purpose input/output digital pin

Pin No.			Pin Name	Pin Type	Description
LQFP 64	LQFP 48	QFN 33			
			MOSI10	O	MOSI10: SPI1 MOSI (Master Out, Slave In) pin
37	28	20	PC.10	I/O	General purpose input/output digital pin
			MISO10	I	MISO10: SPI1 MISO (Master In, Slave Out) pin
38			VDD	P	Power supply for I/O ports
39	29	21	PC.9	I/O	General purpose input/output digital pin
			SPICLK1	I/O	SPICLK1: SPI1 serial clock pin
40	30	22	PC.8	I/O	General purpose input/output digital pin
			SPISS10	I/O	SPISS10: SPI1 slave select pin
41	31		PA.15	I/O	General purpose input/output digital pin
			PWM3	O	PWM3: PWM output pin
42			VSS	P	Ground
43	32		PA.14	I/O	General purpose input/output digital pin
			PWM2	O	PWM2: PWM output pin
44	33		PA.13	I/O	General purpose input/output digital pin
			PWM1	O	PWM1: PWM output pin
45	34		PA.12	I/O	General purpose input/output digital pin
			PWM0	O	PWM0: PWM output pin
46	35	23	ICE_DAT	I/O	Serial Wired Debugger Data pin
47	36	24	ICE_CK	I	Serial Wired Debugger Clock pin
48	37	25	AVDD	AP	Power supply for internal analog circuit
49	38		PD.0	I/O	General purpose input/output digital pin
50	39	26	PD.1	I/O	General purpose input/output digital pin
			SPISS01	I/O	SPISS01: SPI0 2nd slave select pin (for QFN33 only)
51	40	27	PD.2	I/O	General purpose input/output digital pin
52	41	28	PD.3	I/O	General purpose input/output digital pin
53	42		PD.4	I/O	General purpose input/output digital pin
54	43		PD.5	I/O	General purpose input/output digital pin
55			PB.15	I/O	General purpose input/output digital pin
			/INT1	I	/INT1: External interrupt 1 input pin
56	44	29	XT1_OUT	O	Crystal output pin

Pin No.			Pin Name	Pin Type	Description
LQFP 64	LQFP 48	QFN 33			
57	45	30	XT1_IN	**I**	Crystal input pin
58	46	31	/RESET	**I**	External reset input: Low active, set this pin low reset chip to initial state. With internal pull-up.
59		33	VSS	**P**	Ground
60			VDD	**P**	Power supply for I/O ports
61	47		PF.2	**I/O**	General purpose input/output digital pin
			PS2DAT	**I/O**	PS/2 data pin
62	48		PF.3	**I/O**	General purpose input/output digital pin
			PS2CLK	**I/O**	PS/2 clock pin
63	1	32	PVSS	**P**	PLL Ground
64			PB.8	**I/O**	General purpose input/output digital pin
			TM0	**O**	TM0: Timer0 external counter input

Note: Pin Type I = Digital Input, O = Digital Output; AI = Analog Input; P = Power Pin; AP = Analog Power

5 BLOCK DIAGRAM

5.1 NuMicro® NUC122 Series Block Diagram

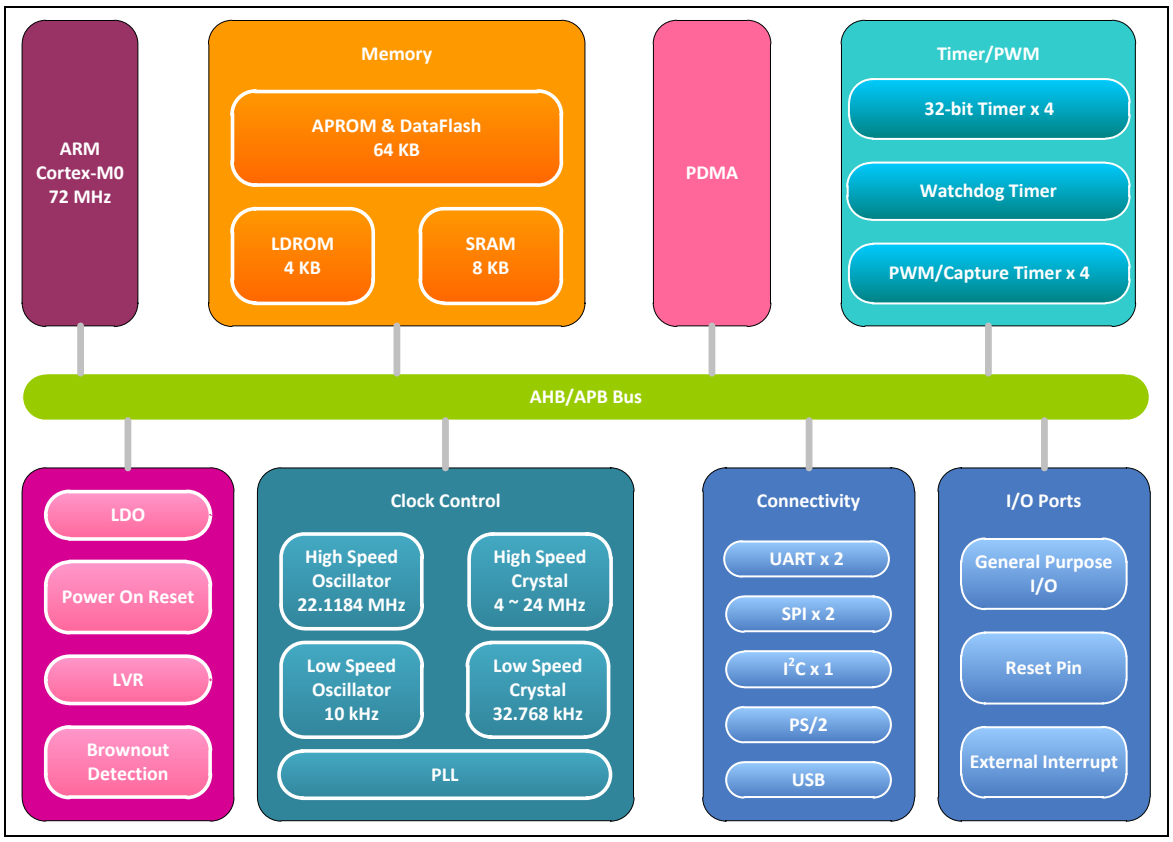


Figure 5-1 NuMicro® NUC122 Series Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM® Cortex®-M0 Core

The Cortex®-M0 processor, a configurable, multistage, 32-bit RISC processor, has an AMBA AHB-Lite interface and includes an NVIC component. The processor has optional hardware debug functionality, can execute Thumb code, and is compatible with other Cortex®-M profile processors. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. Figure 6-1 shows the functional controller of processor.

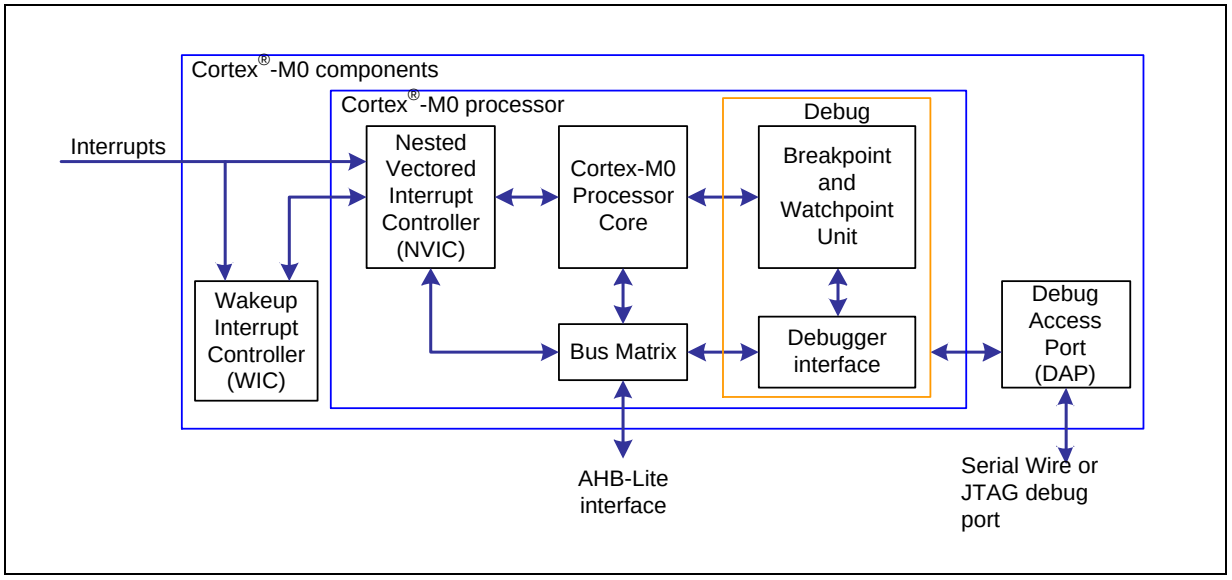


Figure 6-1 Functional Controller Diagram

The implemented device provides the following components and features:

- A low gate count processor that features:
  - The ARM® v6-M Thumb® instruction set
  - Thumb-2 technology
  - ARM® v6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - The system interface supports little-endian data accesses
  - The ability to have deterministic, fixed-latency, and interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the ARM® v6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low power sleep mode entry using Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or the return from interrupt sleep-on-exit feature
- NVIC that features:
  - 32 external interrupt inputs, each with four levels of priority
  - Dedicated Non-maskable Interrupt (NMI) input.

  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC), and provides Ultra-low Power Sleep mode support.
- Debug support
  - Four hardware breakpoints.
  - Two watchpoints.
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling.
  - Single step and vector catch capabilities.
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory.
  - Single 32-bit slave port that supports the DAP (Debug Access Port).

6.2 System Manager

6.2.1 Overview

System management includes these following sections:

- System Resets
- System Memory Map
- System management registers for Part Number ID, chip reset and on-chip controllers reset, multi-functional pin control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the below listed events. For these reset event flags can be read by RSTSRC register.

- Power-On Reset
- Low level on the /RESET pin
- Watchdog Timer Time-Out Reset
- Low Voltage Reset
- Brown-out Detector Reset
- CPU Reset
- System Reset

Both System Reset and Power-On Reset can reset the whole chip including all peripherals. The difference between System Reset and Power-On Reset is external Crystal circuit and ISPCON.BS bit. System Reset doesn't reset external Crystal circuit and ISPCON.BS bit, but Power-On Reset does.

6.2.3 System Power Distribution

In this chip, the power distribution is divided into three segments.

- Analog power from AV_{DD} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.8 V power for digital operation and I/O pins.
- USB transceiver power from V_{BUS} offers the power for operating the USB transceiver.

The outputs of internal voltage regulators, LDO and V_{DD33}, require an external 1 uF capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}). Figure 6-2 shows the power distribution of NuMicro® NUC122 Series.

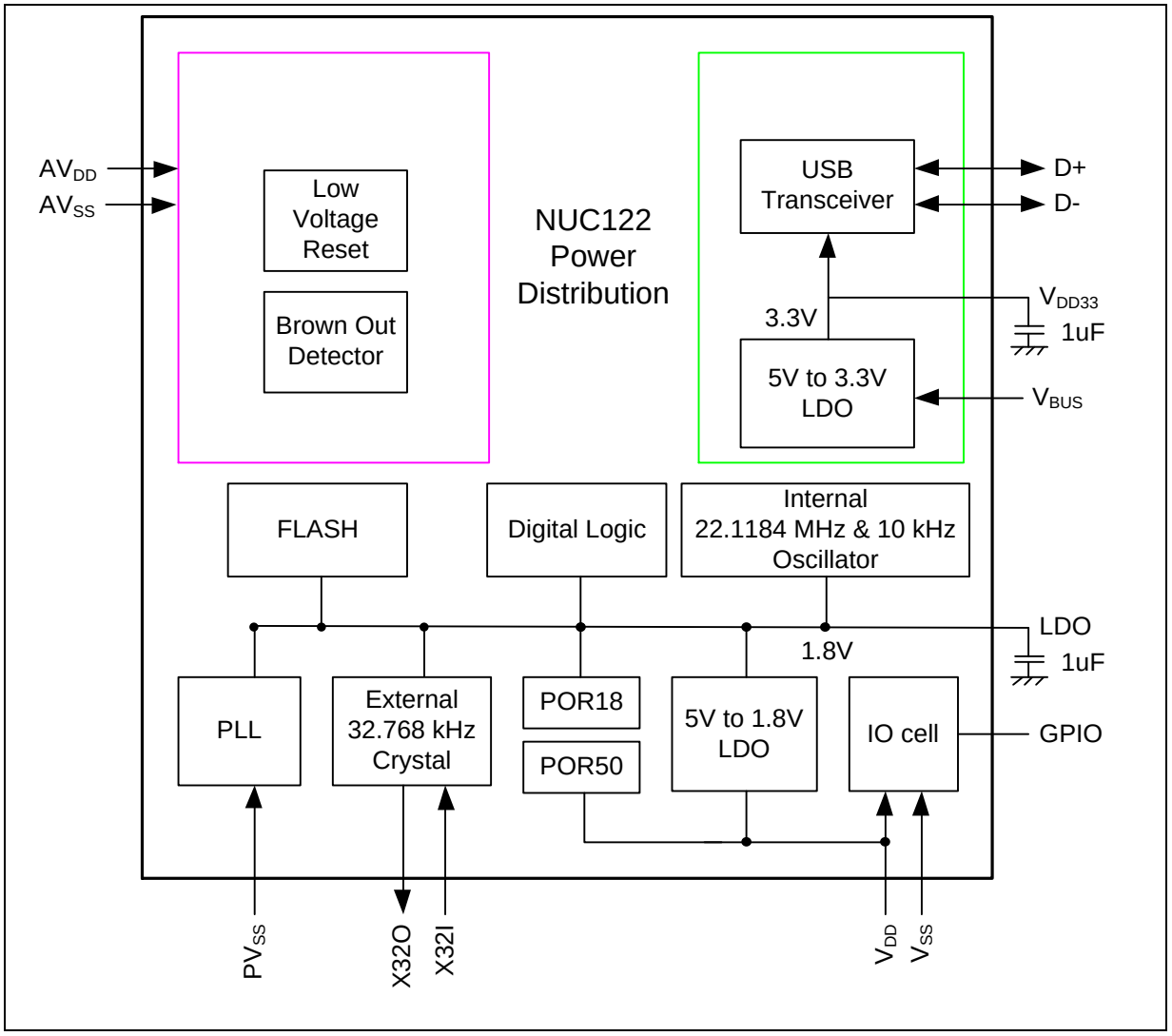


Figure 6-2 NuMicro® NUC122 Series Power Distribution Diagram

6.2.4 System Memory Map

The NuMicro® NUC122 Series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6-1. The detailed register definition, memory space, and programming detailed will be described in the following sections for each on-chip peripherals. The NuMicro® NUC122 Series only supports little-endian data format.

Address Space	Token	Controllers
Flash & SRAM Memory Space		
0x0000_0000 – 0x0000_FFFF	FLASH_BA	FLASH Memory Space (64KB)
0x2000_0000 – 0x2000_1FFF	SRAM_BA	SRAM Memory Space (8KB)
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	GCR_BA	System Global Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
APB1 Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4000_8000 – 0x4000_BFFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with Master/Slave Function Control Registers
0x4003_4000 – 0x4003_7FFF	SPI1_BA	SPI1 with Master/Slave Function Control Registers
0x4004_0000 – 0x4004_3FFF	PWMA_BA	PWM0/1/2/3 Control Registers
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x4006_0000 – 0x4006_3FFF	USBD_BA	USB 2.0 FS Device Controller Registers
APB2 Controllers Space (0x4010_0000 ~ 0x401F_FFFF)		
0x4010_0000 – 0x4010_3FFF	PS2_BA	PS/2 Interface Control Registers
0x4011_0000 – 0x4011_3FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4012_0000 – 0x4012_3FFF	I2C1_BA	I^2C1 Interface Control Registers
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		

0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6-1 Address Space Assignments for On-Chip Controllers

6.2.5 System Timer (SysTick)

The Cortex®-M0 includes an integrated system timer, SysTick. SysTick provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used in several different ways, for example:

- An RTOS tick timer which fires at a programmable rate (for example 100 Hz) and invokes a SysTick routine.
- A high speed alarm timer using Core clock.
- A variable rate alarm or signal timer – the duration range dependent on the reference clock used and the dynamic range of the counter.
- A simple counter. Software can use this to measure time to completion and time used.
- An internal clock source control based on missing/meeting durations. The COUNTFLAG bit-field in the control and status register can be used to determine if an action completed within a set duration, as part of a dynamic clock management control loop.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the documents “ARM® Cortex®-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.2.6 Nested Vectored Interrupt Controller (NVIC)

Cortex®-M0 provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)". It is closely coupled to the processor kernel and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Dynamic priority changing
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in "Handler Mode". This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When any interrupts is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0~R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the documents "ARM® Cortex®-M0 Technical Reference Manual" and "ARM® v6-M Architecture Reference Manual".

6.2.6.1 Exception Model and System Interrupt Map

Table 6-2 lists the exception model supported by NuMicro® NUC122 Series. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as "0" and the lowest priority is denoted as "3". The default priority of all the user-configurable interrupts is "0". Note that priority "0" is treated as the fourth priority on the system, after three system exceptions "Reset", "NMI" and "Hard Fault".

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 6-2 Exception Model

Vector Number	Interrupt Number (Bit in Interrupt Registers)	Interrupt Name	Source IP	Interrupt description
0 ~ 15	-	-	-	System exceptions
16	0	**BOD_OUT**	Brownout	Brownout low voltage detected interrupt
17	1	**WDT_INT**	WDT	Watchdog Timer interrupt
18	2	**EINT0**	GPIO	External signal interrupt from PB.14 pin
19	3	**EINT1**	GPIO	External signal interrupt from PB.15 pin
20	4	**GPAB_INT**	GPIO	External signal interrupt from PA[15:0]/PB[13:0]
21	5	**GPCD_INT**	GPIO	External interrupt from PC[15:0]/PD[15:0]
22	6	**PWMA_INT**	PWM0~3	PWM0, PWM1, PWM2 and PWM3 interrupt
23	7	**Reserved**	Reserved	Reserved
24	8	**TMR0_INT**	TMR0	Timer 0 interrupt
25	9	**TMR1_INT**	TMR1	Timer 1 interrupt
26	10	**TMR2_INT**	TMR2	Timer 2 interrupt
27	11	**TMR3_INT**	TMR3	Timer 3 interrupt
28	12	**UART0_INT**	UART0	UART0 interrupt
29	13	**UART1_INT**	UART1	UART1 interrupt

30	14	**SPI0_INT**	SPI0	SPI0 interrupt
31	15	**SPI1_INT**	SPI1	SPI1 interrupt
32	16	**Reserved**	Reserved	Reserved
33	17	**Reserved**	Reserved	Reserved
34	18	**Reserved**	Reserved	Reserved
35	19	**I2C1_INT**	I2C1	I2C1 interrupt
36	20	**Reserved**	Reserved	Reserved
37	21	**Reserved**	Reserved	Reserved
38	22	**Reserved**	Reserved	Reserved
39	23	**USB_INT**	USBD	USB 2.0 FS Device interrupt
40	24	**PS2_INT**	PS/2	PS/2 interrupt
41	25	**Reserved**	Reserved	Reserved
42	26	**Reserved**	Reserved	Reserved
43	27	**Reserved**	Reserved	Reserved
44	28	**PWRWU_INT**	CLKC	Power-down Wake-up interrupt
45	29	**Reserved**	Reserved	Reserved
46	30	**Reserved**	Reserved	Reserved
47	31	**RTC_INT**	RTC	Real time clock interrupt

Table 6-3 System Interrupt Map

6.2.6.2 Vector Table

When any interrupts is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For ARM® v6-M, the vector table base address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Vector Table Word Offset	Description
0	SP_main – The Main stack pointer
Vector Number	Exception Entry Pointer using that Vector Number

Table 6-4 Vector Table Format

6.2.6.3 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates the clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip will not enter power-down mode until CPU sets the power-down enable bit (PWR_DOWN_EN) and Cortex®-M0 core executes the WFI instruction. After that, chip enters power-down mode and wait for wake-up interrupt source triggered to leave power-down mode. In the power-down mode, the clock controller turns off the external 4~24 MHz high speed crystal and internal 22.1184 MHz high speed oscillator to reduce the overall system power consumption. Figure 6-3 shows the overview of the clock source control.

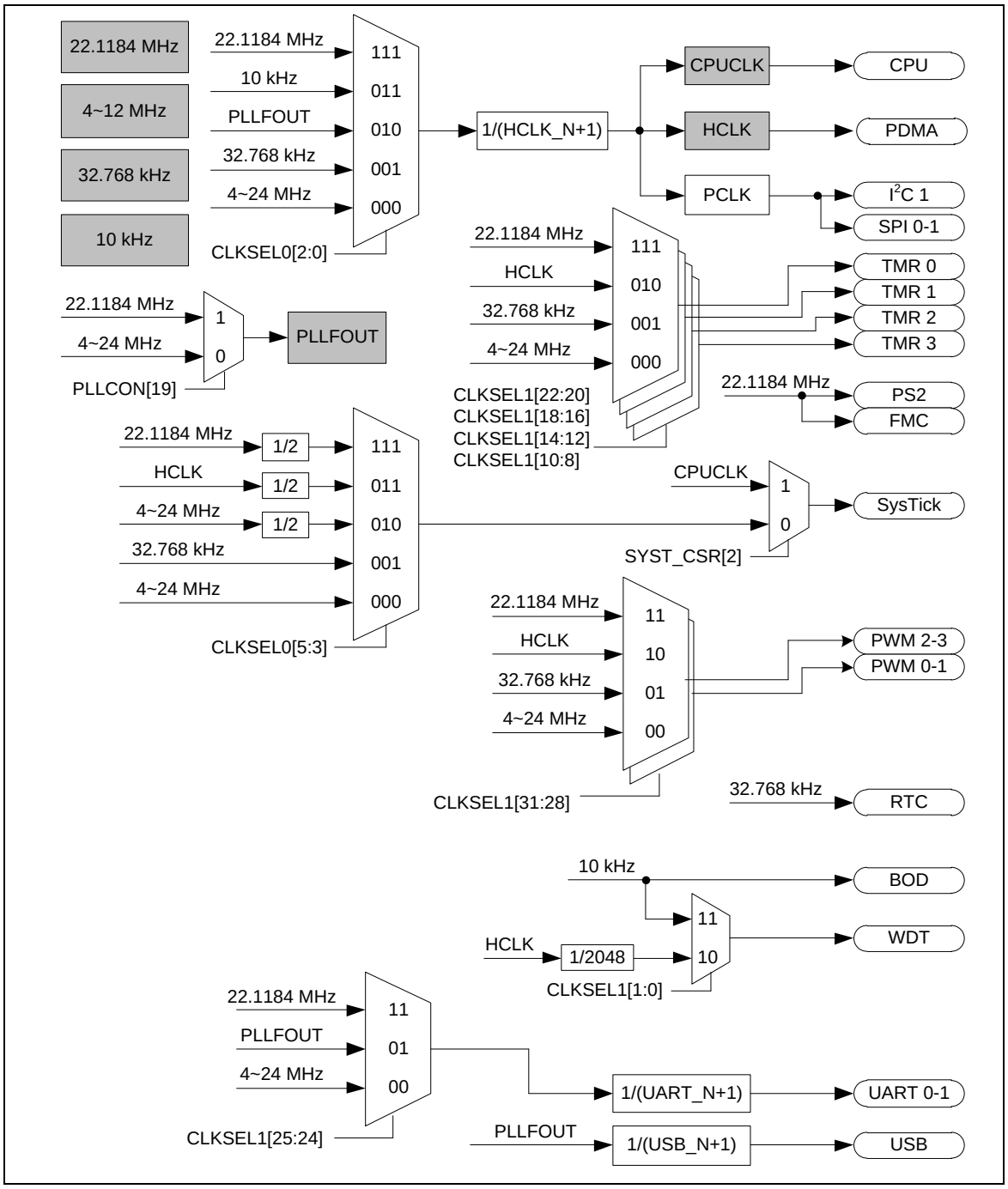


Figure 6-3 Clock Generator Global View Diagram

6.3.2 Clock Generator

The clock generator consists of 5 clock sources which are listed as below:

- One external 32.768 kHz low speed crystal
- One external 4~24 MHz high speed crystal
- One programmable PLL FOUT (PLL source consists of external 4~24 MHz high speed crystal and internal 22.1184 MHz high speed oscillator)
- One internal 22.1184 MHz high speed oscillator
- One internal 10 kHz low speed oscillator

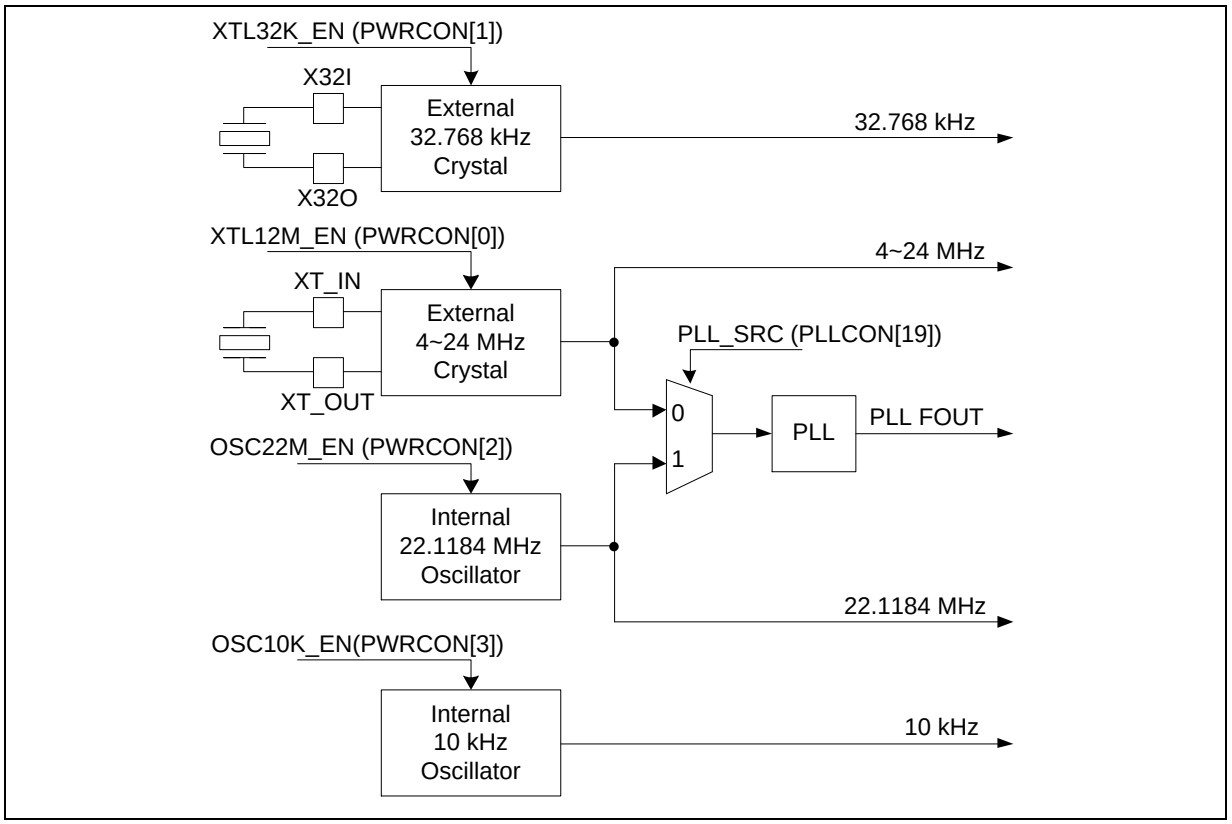


Figure 6-4 Clock Generator Block Diagram

6.3.3 System Clock and SysTick Clock

The system clock has 5 clock sources which were generated from clock generator block. The clock source switch depends on the register HCLK_S (CLKSEL0[2:0]). The block diagram is shown in Figure 6-5.

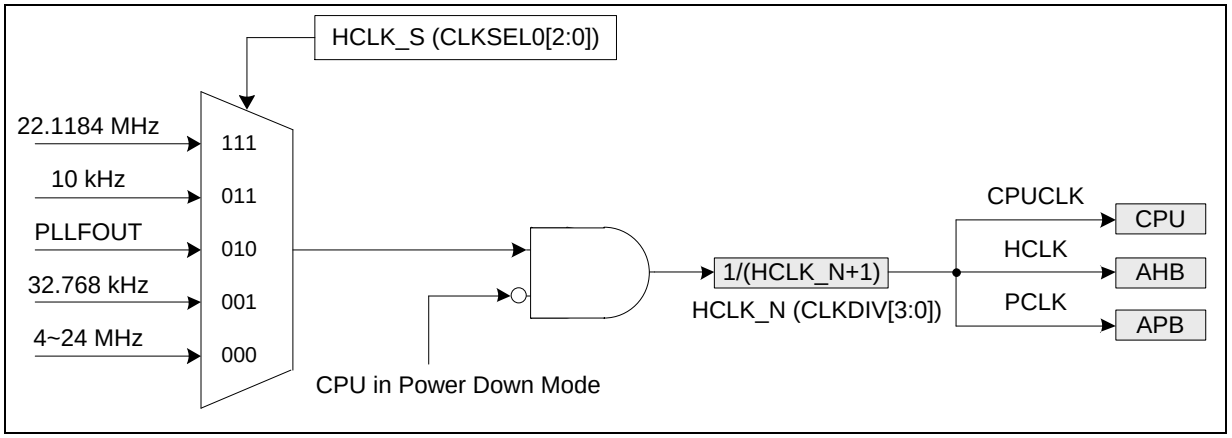


Figure 6-5 System Clock Block Diagram

The clock source of SysTick in Cortex®-M0 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLK_S (CLKSEL0[5:3]. The block diagram is shown in Figure 6-6.

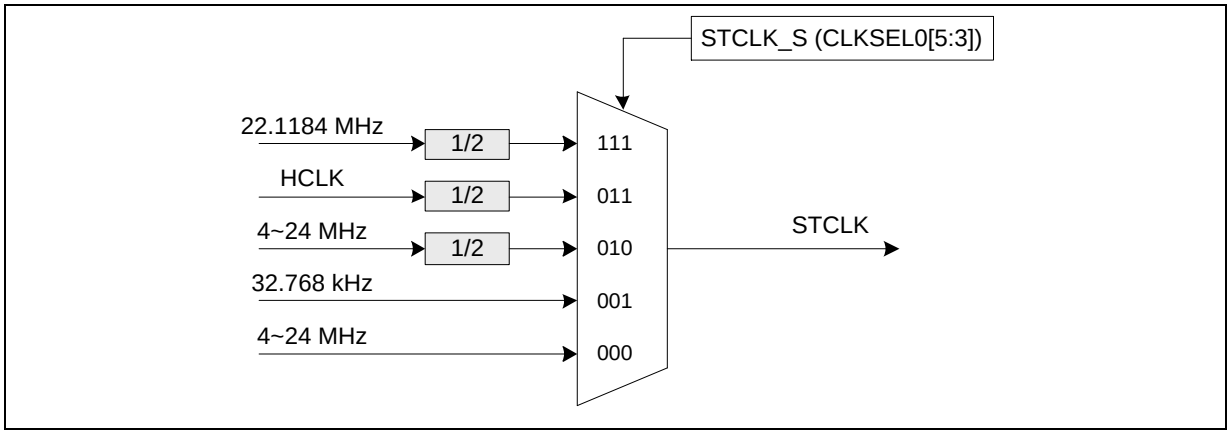


Figure 6-6 SysTick Clock Control Block Diagram

6.3.4 Peripherals Clock

The peripherals clock had different clock source switch setting depending on different peripherals. Please refer to the CLKSEL1 and CLKSEL2 register description in TRM.

6.3.5 Power-down Mode Clock

When chip enters into Power-down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripherals clock are still active in Power-down mode.

The clocks kept active are listed below:

- Clock Generator
  - Internal 10 kHz low speed oscillator clock
  - External 32.768 kHz low speed crystal clock
- Peripherals Clock (When WDT adopts 10 KHz low speed as clock source and RTC adopts 32.768 kHz low speed as clock source)

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

The NuMicro® NUC122 Series equips with 32 K/64 K bytes on-chip embedded Flash for application program memory (APROM) that can be updated through ISP procedure. In System Programming (ISP) function enables user to update program memory when chip is soldered on PCB. After chip power on, Cortex®-M0 CPU fetches code from APROM or LDROM decided by boot select (CBS) in Config0. By the way, NuMicro® NUC122 Series also provides additional DATA Flash for user to store some application dependent data before chip power off. For 32 K/64 K bytes APROM device, the data flash is fixed at 4K bytes.

6.4.2 Features

- Run up to 72 MHz with zero wait state for continuous address read access
- 32 K/64 K bytes application program memory (APROM)
- 4 KB in system programming (ISP) loader program memory (LDROM)
- Fixed 4KB data flash with 512 bytes page erase unit
- In System Program (ISP) to update on chip Flash

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

The NuMicro® NUC122 Series has up to 43 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 43 pins are arranged in 5 ports named with GPIOA, GPIOB, GPIOC, GPIOD and GPIOF. Each port equips maximum 16 pins. Each of the 43 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as input, output, open-drain or quasi-bidirectional mode. After reset, the I/O type of all pins stay in quasi-bidirectional mode and port data register GPIOx_DOUT[15:0] resets to 0x0000_FFFF. Each I/O pin equips a very weakly individual pull-up resistor which is about 110 kΩ ~ 300 kΩ for V_{DD} is from 5.5 V to 2.5 V.

6.5.2 Features

- Four I/O modes:
  - Quasi bi-direction
  - Push-Pull output
  - Open-Drain output
  - Input only with high impendence
- TTL/Schmitt trigger input selectable
- I/O pin configured as interrupt source with edge/level setting
- Supports High Driver and High Sink I/O mode

6.6 I²C Serial Interface Controller (Master/Slave) (I²C)

6.6.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

6.6.2 Features

- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter requesting the I2C interrupt if the I2C bus hangs up and timer-out counter overflows
- External pull-up needed for high output
- Programmable clocks allow versatile rate control
- Supports 7-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)

6.7 PS/2 Device Controller (PS2D)

6.7.1 Overview

PS/2 device controller provides basic timing control for PS/2 communication. All communication between the device and the host is managed through the CLK and DATA pins. Unlike PS/2 keyboard or mouse device controller, the received/transmit code needs to be translated as meaningful code by firmware. The device controller generates the CLK signal after receiving a request to send, but host has ultimate control over communication. DATA sent from the host to the device is read on the rising edge and DATA sent from device to the host is change after rising edge. A 16 bytes FIFO is used to reduce CPU intervention. Software can select 1 to 16 bytes for a continuous transmission.

6.7.2 Features

- Host communication inhibit and request to send detection
- Reception frame error detection
- Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
- Double buffer for data reception
- S/W override bus

6.8 PWM Generator and Capture Timer (PWM)

6.8.1 Overview

The NuMicro® NUC122 Series has one set of PWM group supporting a total of 2 sets of PWM generators that can be configured as 4 independent PWM outputs, PWM0~PWM3, or as 2 complementary PWM pairs, (PWM0, PWM1) and (PWM2, PWM3) with 2 programmable dead-zone generators. PWM output function can be alternated to capture function.

Each PWM generator has one 8-bit prescaler, one clock divider with 5 divided frequencies (1, 1/2, 1/4, 1/8, 1/16), two PWM Timers including two clock selectors, two 16-bit PWM down-counters for PWM period control, two 16-bit comparators for PWM duty control and one dead-zone generator. The PWM generators provide eight independent PWM interrupt flags which are set by hardware when the corresponding PWM period down counter reaches zero.

Each PWM interrupt source with its corresponding enable bit can cause CPU to request PWM interrupt. The PWM generators can be configured as one-shot mode to produce only one PWM cycle signal or auto-reload mode to output PWM waveform continuously.

6.8.2 Features

PWM function:

- PWM group has two PWM generators. Each PWM generator supports one 8-bit prescaler, one clock divider, two PWM-timers (down counter), one dead-zone generator and two PWM outputs.
- Up to 16-bit resolution
- PWM Interrupt request synchronized with PWM period
- One-shot or Auto-reload mode PWM
- One PWM group (PWMA) to support 4 PWM channels or 2 PWM paired channels

Capture function:

- Timing control logic shared with PWM generators
- Supports 4 Capture input channels shared with 4 PWM output channels
- Each channel supports one rising latch register (CRLR), one falling latch register (CFLR) and Capture interrupt flag (CAPIFx)

6.9 Real Time Clock (RTC)

6.9.1 Overview

Real Time Clock (RTC) controller provides user the real time and calendar message. The clock source of RTC is from an external 32.768 kHz low speed crystal connected at pins X32I and X32O (refer to pin Description) or from an external 32.768 kHz low speed oscillator output fed at pin X32I. The RTC controller provides the time message (second, minute, hour) in Time Loading Register (TLR) as well as calendar message (day, month, year) in Calendar Loading Register (CLR). The data message is expressed in BCD format. It also offers alarm function that user can preset the alarm time in Time Alarm Register (TAR) and alarm calendar in Calendar Alarm Register (CAR).

The RTC controller supports periodic Time Tick and Alarm Match interrupts. The periodic interrupt has 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second which are selected by TTR (TTR[2:0]). When RTC counter in TLR and CLR is equal to alarm setting time registers TAR and CAR, the alarm interrupt flag (RIIR.AIF) is set and the alarm interrupt is requested if the alarm interrupt is enabled (RIER.AIER=1). Both RTC Time Tick and Alarm Match can cause chip wake-up from Power-down mode if wake-up function is enabled (TWKE (TTR[3])=1).

6.9.2 Features

- Supports time counter (second, minute, hour) and calendar counter (day, month, year) for time check
- Alarm register (second, minute, hour, day, month, year)
- Selectable 12-hour or 24-hour mode
- Leap year compensation automatically
- Day of week counter
- Frequency compensate register (FCR)
- All time and calendar message expressed in BCD code
- Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
- Supports RTC Time Tick and Alarm Match interrupt
- Supports wake-up chip from Power-down mode

6.10 Serial Peripheral Interface (SPI)

6.10.1 Overview

The Serial Peripheral Interface (SPI) is a synchronous serial data communication protocol which operates in full duplex mode. Devices communicate in Master/Slave mode with 4-wire bi-direction interface. The NuMicro® NUC122 Series contains two sets of SPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each set of SPI controller can be set as a master that can drive up to 2 external peripheral slave devices; it can also be configured as a slave device controlled by an off-chip master device.

6.10.2 Features

- Up to two sets of SPI controller
- Supports Master or Slave mode operation
- Configurable bit length up to 32-bit of a transfer word and configurable word numbers up to 2 of a transaction, so the maximum bit length is 64-bit for each data transfer
- Provides burst mode operation, transmit/receive transferred up to two times word transaction in one transfer
- Supports MSB or LSB first transfer
- Two device/slave select lines in Master mode, and 1 device/slave select line in Slave mode
- Supports byte reorder function
- Supports byte or word suspend mode
- Variable output serial clock frequency in Master mode
- Supports two programmable serial clock frequencies in Master mode

6.11 Timer Controller (TMR)

6.11.1 Overview

The timer controller includes four 32-bit timers, TIMER0~TIMER3, which allows user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, event counting, interval measurement, clock generation, and delay timing. The timer can generate an interrupt signal upon timeout, or provide the current value during operation.

NuMicro® NUC122 Series also supports toggle mode, continuous counting mode and event counting function.

6.11.2 Features

- 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle and continuous counting operation modes
- Time out period = (Period of timer clock input) * (8-bit pre-scale counter + 1) * (24-bit TCMP)
- Maximum counting cycle time = (1 / T MHz) * (2^8) * (2^{24}), T is the period of timer clock
- 24-bit timer value is readable through TDR (Timer Data Register)
- Supports event counting function to count the event from external pin

6.12 UART Interface Controller (UART)

6.12.1 Overview

The NuMicro® NUC122 Series provides up to two channels of Universal Asynchronous Receiver/Transmitters (UART). UART0 and UART1 perform Normal Speed UART. Besides, Both of UART0 and UART1 also support flow control function.

6.12.2 Features

- Full duplex, asynchronous communications
- Separates receive/transmit 14 bytes entry FIFO for data payloads
- Supports hardware auto flow control/flow control function (CTS, RTS) and programmable RTS flow control trigger level
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports CTS wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting UA_TOR [DLY] register
- Supports break error, frame error, parity error and receive/transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8-bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - Supports 3-/16-bit duration for normal mode
- Supports RS-485 function mode.
  - Supports RS-485 9-bit mode
  - Supports hardware or software direct enable control provided by RTS pin

6.13 USB Device Controller (USB)

6.13.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and support control/bulk/interrupt/ isochronous transfer types.

In this device controller, there are two main interfaces: the APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 512 bytes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SIE. Users need to set the effective starting address of SRAM for each endpoint buffer through “buffer segmentation register (USB_BUFSEGx)”.

There are 6 endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of ENDPOINT CONTROL is also used to manage the data sequential synchronization, endpoint states, current start address, transaction status, and data buffer status for each endpoint.

There are four different interrupt events in this controller. They are the wake-up function, device plug-in or plug-out event, USB events, like IN ACK, OUT ACK etc, and BUS events, like suspend and resume, etc. Any event will cause an interrupt, and user just needs to check the related event flags in interrupt event status register (USB_INTSTS) to acknowledge what kind of interrupt occurring, and then check the related USB Endpoint Status Register (USB_EPSTS) to acknowledge what kind of event occurring in this endpoint.

A software-disable function is also supported for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables DRVSE0 bit (USB_DRVSE0), the USB controller will force the output of USB_DP and USB_DM to level low and its function is disabled. After disable the DRVSE0 bit, host will enumerate the USB device again.

For more information on the Universal Serial Bus, please refer to *Universal Serial Bus Specification Revision 1.1.*

6.13.2 Features

- Compliant with USB 2.0 Full-Speed specification
- Provides 1 interrupt vector with 4 different interrupt events (WAKEUP, FLDET, USB and BUS)
- Supports Control/Bulk/Interrupt/Isochronous transfer types
- Supports suspend function when no bus activity existing for 3 ms
- Provides 6 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 512 bytes buffer size
- Provides remote wake-up capability

6.14 Watchdog Timer (WDT)

6.14.1 Overview

The purpose of Watchdog Timer (WDT) is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

6.14.2 Features

- 18-bit free running up counter for WDT time-out interval
- Selectable time-out interval (2^4 ~ 2^{18}) and the time-out interval is 1.6 ms ~ 26.214 s if WDT_CLK = 10 kHz.
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026、130、18 or 3 WDT_CLK reset delay period
- Supports to force WDT enabled after chip powered on or reset by setting CWDTEN in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as 10 kHz.

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
$V_{DD} - V_{SS}$	DC Power Supply	-0.3	+7.0	V
V_{IN}	Input Voltage	V_{SS}-0.3	V_{DD}+0.3	V
$1/t_{CLCL}$	Oscillator Frequency	4	24	MHz
T_A	Operating Temperature	-40	+85	°C
T_{ST}	Storage Temperature	-55	+150	°C
I_{DD}	Maximum Current into V_{DD}	-	120	mA
I_{SS}	Maximum Current out of V_{SS}		120	mA
I_{IO}	Maximum Current sunk by a I/O pin		35	mA
	Maximum Current sourced by a I/O pin		35	mA
	Maximum Current sunk by total I/O pins		100	mA
	Maximum Current sourced by total I/O pins		100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affect the lift and reliability of the device.

7.2 DC Electrical Characteristics

7.2.1 DC Electrical Characteristics

(V_{DD}-V_{SS} = 3.3 V, T_A = 25 °C, F_{OSC} = 72 MHz unless otherwise specified.)

PARAMETER	SYM	SPECIFICATIONS				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
Operation voltage	V_{DD}	2.5		5.5	V	V_{DD} = 2.5 V - 5.5 V up to 72 MHz
Power Ground	V_{SS} AV_{SS}	-0.3		+0.3	V	
LDO Output Voltage	V_{LDO}	1.62	1.8	1.98	V	V_{DD} > 2.5 V
Analog Operating Voltage	AV_{DD}	V_{DD}			V	
Operating Current Normal Run Mode at 72 MHz	I_{DD1}		25		mA	V_{DD} = 5.5 V at 72 MHz, All IP and PLL Enabled, XTAL=12 MHz
	I_{DD2}		16		mA	V_{DD} = 5.5 V at 72 MHz, All IP Disabled and PLL Enabled, XTAL=12 MHz
	I_{DD3}		24		mA	V_{DD} = 3 V at 72 MHz, All IP and PLL Enabled, XTAL = 12 MHz
	I_{DD4}		15.5		mA	V_{DD} = 3 V at 72 MHz, All IP Disabled and PLL Enabled, XTAL=12 MHz
Operating Current Normal Run Mode at 60 MHz	I_{DD5}		21.5		mA	V_{DD} = 5.5 V at 60 MHz, All IP and PLL Enabled, XTAL=12 MHz
	I_{DD6}		14		mA	V_{DD} = 5.5 V at 60 MHz, All IP Disabled and PLL Enabled, XTAL=12 MHz
	I_{DD7}		20.5		mA	V_{DD} = 3 V at 60 MHz, All IP and PLL Enabled, XTAL = 12 MHz
	I_{DD8}		13.5		mA	V_{DD} = 3 V at 60 MHz, All IP Disabled and PLL Enabled, XTAL=12 MHz
Operating Current Normal Run Mode at 22.1184 MHz	I_{DD9}		10		mA	V_{DD} = 5.5 V at 22.1184 MHz, All IP Enabled and PLL Disabled,
	I_{DD10}		7		mA	V_{DD} = 5.5 V at 22.1184 MHz, All IP and PLL Disabled,

PARAMETER	SYM	SPECIFICATIONS				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
	I_{DD11}		9.5		mA	V_{DD} = 3 V at 22.1184 MHz, All IP Enabled and PLL Disabled
	I_{DD12}		6.5		mA	V_{DD} = 3 V at 22.1184 MHz, All IP and PLL Disabled,
Operating Current Normal Run Mode at 12 MHz	I_{DD13}		6.5		mA	V_{DD} = 5.5 V at 12 MHz, All IP Enabled and PLL Disabled, XTAL=12 MHz
	I_{DD14}		5		mA	V_{DD} = 5.5 V at 12 MHz, All IP and PLL Disabled, XTAL = 12 MHz
	I_{DD15}		6		mA	V_{DD} = 3 V at 12 MHz, All IP Enabled and PLL Disabled, XTAL= 12 MHz
	I_{DD16}		4.5		mA	V_{DD} = 3 V at 12 MHz, All IP and PLL Disabled, XTAL = 12 MHz
Operating Current Normal Run Mode at 4 MHz	I_{DD17}		3		mA	V_{DD} = 5 V at 4 MHz, All IP Enabled and PLL Disabled, XTAL = 4 MHz
	I_{DD18}		2.5		mA	V_{DD} = 5 V at 4 MHz, All IP and PLL Disabled, XTAL = 4 MHz
	I_{DD19}		2.5		mA	V_{DD} = 3 V at 4 MHz, All IP Enabled and PLL Disabled, XTAL = 4 MHz
	I_{DD20}		2		mA	V_{DD} = 3 V at 4 MHz, All IP and PLL Disabled, XTAL = 4 MHz
Operating Current Idle Mode at 72 MHz	I_{IDLE1}		18.5		mA	V_{DD}= 5.5 V at 72 MHz, All IP and PLL Enabled, XTAL = 12 MHz
	I_{IDLE2}		10		mA	VDD = 5.5 V at 72 MHz, All IP Disabled and PLL Enabled, XTAL = 12 MHz
	I_{IDLE3}		17		mA	V_{DD} = 3 V at 72 MHz, All IP and PLL Enabled, XTAL = 12 MHz
	I_{IDLE4}		9		mA	V_{DD} = 3 V at 72 MHz, All IP Disabled and PLL Enabled, XTAL=12 MHz
Operating Current Idle Mode	I_{IDLE5}		16		mA	V_{DD}= 5.5 V at 60 MHz, All IP and PLL Enabled, XTAL = 12 MHz

PARAMETER	SYM	SPECIFICATIONS				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
at 60 MHz	I_{IDLE6}		8.5		mA	VDD = 5.5 V at 60 MHz, All IP Disabled and PLL Enabled, XTAL = 12 MHz
	I_{IDLE7}		14.5		mA	V_{DD} = 3 V at 60 MHz, All IP and PLL Enabled, XTAL = 12 MHz
	I_{IDLE8}		7.7		mA	V_{DD} = 3 V at 60 MHz, All IP Disabled and PLL Enabled, XTAL=12 MHz
Operating Current Idle Mode at 22.1184 MHz	I_{IDLE9}		6		mA	V_{DD} = 5.5 V at 22.1184 MHz, All IP Enabled and PLL Disabled,
	I_{IDLE10}		3		mA	V_{DD} = 5.5 V at 22.1184 MHz, All IP and PLL Disabled,
	I_{IDLE11}		5.2		mA	V_{DD} = 3 V at 22.1184 MHz, All IP Enabled and PLL Disabled
	I_{IDLE12}		2.5		mA	V_{DD} = 3 V at 22.1184 MHz, All IP and PLL Disabled,
Operating Current Idle Mode at 12 MHz	I_{IDLE13}		3.7		mA	V_{DD} = 5.5 V at 12 MHz, All IP Enabled and PLL Disabled, XTAL = 12 MHz
	I_{IDLE14}		2		mA	V_{DD} = 5.5 V at 12 MHz, All IP and PLL Disabled, XTAL = 12 MHz
	I_{IDLE15}		3.2		mA	V_{DD} = 3 V at 12 MHz, All IP Enabled and PLL Disabled, XTAL=12 MHz
	I_{IDLE16}		1.8		mA	V_{DD} = 3 V at 12 MHz, All IP and PLL Disabled, XTAL = 12 MHz
Operating Current Idle Mode at 4 MHz	I_{IDLE17}		2		mA	V_{DD} = 5 V at 4 MHz, All IP Enabled and PLL Disabled, XTAL = 4 MHz
	I_{IDLE18}		1.3		mA	V_{DD} = 5 V at 4 MHz, All IP and PLL Disabled, XTAL = 4 MHz
	I_{IDLE19}		1.6		mA	V_{DD} = 3 V at 4 MHz, All IP Enabled and PLL Disabled, XTAL = 4 MHz
	I_{IDLE20}		1.1		mA	V_{DD} = 3 V at 4 MHz, All IP and PLL Disabled, XTAL = 4 MHz
Standby Current	I_{PWD1}		9.7		µA	V_{DD} = 5.5 V, RTC OFF, No load when BOV function Disabled

PARAMETER	SYM	SPECIFICATIONS				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
Power-down mode	I_{PWD2}		8.7		μA	V_{DD} = 3.3 V, RTC OFF, No load when BOV function Disabled
	I_{PWD3}		11		μA	V_{DD} = 5.5 V, RTC run , No load when BOV function Disabled
	I_{PWD4}		10		μA	V_{DD} = 3.3 V, RTC run , No load when BOV function Disabled
Input Current PA, PB, PC, PD,and PF (Quasi-bidirectional mode)	I_{IN1}	-65	-50		μA	V_{DD} = 5.5 V, V_{IN} = 0V or V_{IN} = V_{DD}
Input Current at /RESET[1]	I_{IN2}	-55	-45	-30	μA	V_{DD} = 3.3 V, V_{IN} = 0.45V
Input Leakage Current PA, PB, PC, PD and PF	I_{LK}	-2	-	+2	μA	V_{DD} = 5.5 V, 0 < V_{IN} < V_{DD}
Logic 1 to 0 Transition Current PA~PD (Quasi-bidirectional mode)	I_{TL} [3]	-650	-	-200	μA	V_{DD} = 5.5 V, V_{IN} < 2.0V
Input Low Voltage PA, PB, PC, PD and PF (TTL input)	V_{IL1}	-0.2	-	0.8	V	V_{DD} = 4.5 V
		-0.2	-	0.6		V_{DD} = 2.5 V
Input High Voltage PA, PB, PC, PD and PF (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5 V
		1.5	-	V_{DD} +0.2		V_{DD} = 3.0 V
Input Low Voltage PA, PB, PC, PD and PF (Schmitt input)	V_{IL2}	-0.2	-	0.4 V_{DD}	V	
Input High Voltage PA, PB, PC, PD and PF (Schmitt input)	V_{IH2}	0.6 V_{DD}	-	V_{DD} +0.2	V	
Hysteresis voltage of PA~PD and PF (Schmitt input)	V_{HY}		0.2 V_{DD}		V	
Input Low Voltage XT1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5 V
		0	-	0.4		V_{DD} = 3.0 V
Input High Voltage XT1[*2]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5 V
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0 V
Input Low Voltage X32I[*2]	V_{IL4}	0	-	0.4	V	
Input High Voltage X32I[*2]	V_{IH4}	1.35		1.8	V	
Negative going threshold (Schmitt input), /RESET	V_{ILS}	-0.2	-	0.3 V_{DD}	V	
Positive going threshold (Schmitt input), /RESET	V_{IHS}	0.7 V_{DD}	-	V_{DD}+0.2	V	
Source Current PA, PB, PC, PD, and PF (Quasi-bidirectional Mode)	I_{SR11}	-300	-395	-450	μA	V_{DD} = 4.5 V, V_S = 2.4 V
	I_{SR12}	-50	-80	-90	μA	V_{DD} = 2.7 V, V_S = 2.2 V
	I_{SR12}	-40	-70	-80	μA	V_{DD} = 2.5 V, V_S = 2.0 V
Source Current PA, PB, PC, PD	I_{SR21}	-20	-24	-28	mA	V_{DD} = 4.5 V, V_S = 2.4 V

PARAMETER	SYM	SPECIFICATIONS				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
and PF(Push-pull Mode)	I_{SR22}	-4	-6	-8	mA	V_{DD} = 2.7 V, V_S = 2.2 V
	I_{SR22}	-3	-5	-7	mA	V_{DD} = 2.5 V, V_S = 2.0 V
Sink Current PA, PB, PC, PD and PF (Quasi-bidirectional and Push-pull Mode)	I_{SK1}	10	16	20	mA	V_{DD} = 4.5 V, V_S = 0.45 V
	I_{SK1}	7	10	13	mA	V_{DD} = 2.7 V, V_S = 0.45 V
	I_{SK1}	6	9	12	mA	V_{DD} = 2.5 V, V_S = 0.45 V
Brown-out voltage with BOV_VL [1:0] =00b	$V_{BO2.2}$	2.1	2.2	2.3	V	
Brown-out voltage with BOV_VL [1:0] =01b	$V_{BO2.7}$	2.6	2.7	2.8	V	
Brown-out voltage with BOV_VL [1:0] =10b	$V_{BO3.8}$	3.6	3.8	4.0	V	
Brown-out voltage with BOV_VL [1:0] =11b	$V_{BO4.5}$	4.3	4.5	4.7	V	
Hysteresis range of BOD voltage	V_{BH}	30	-	150	mV	V_{DD} = 2.5 V - 5.5 V
Band-gap voltage	V_{BG}	1.20	1.26	1.32	V	V_{DD} = 2.5 V - 5.5 V

Notes:

1. nRESET pin is a Schmitt trigger input.
2. Crystal Input is a CMOS input.
3. Pins of PA, PB, PC, PD and PF can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5 V, 5he transition current reaches its maximum value when V_{IN} approximates to 2V.

7.3 AC Electrical Characteristics

7.3.1 External 4~24 MHz High Speed Crystal Characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input clock frequency	External crystal	4	12	24	MHz
Temperature	-	-40	-	85	℃
V_{DD}	-	2.5	5	5.5	V
Operating current	12 MHz at V_{DD} = 5 V	-	1	-	mA

7.3.1.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	10~20 pF	10~20 pF	without

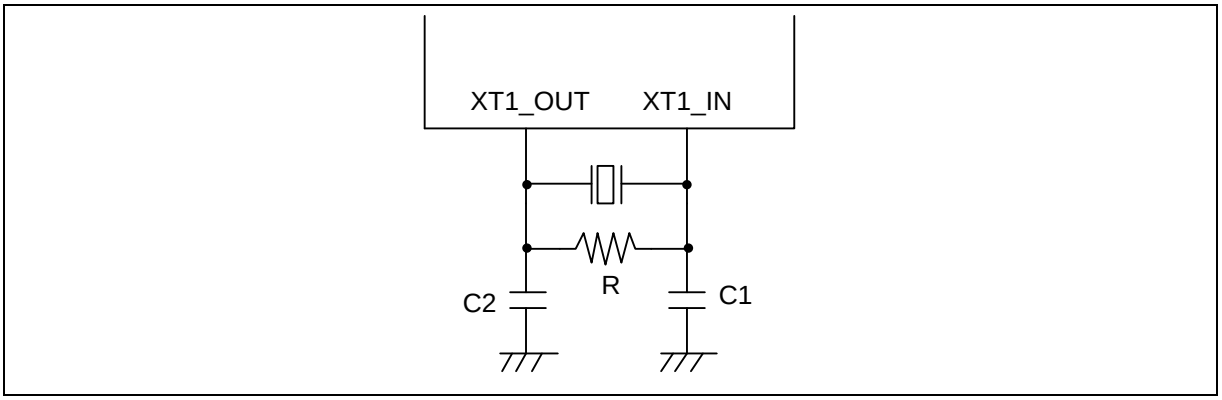
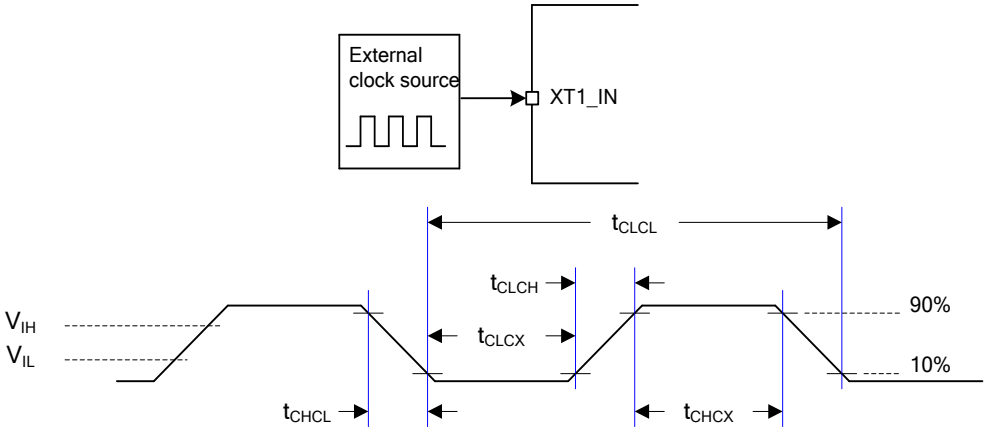


Figure 7-1 Typical Crystal Application Circuit

7.3.2 External 4~24 MHz High Speed Clock Input Signal Characteristics

For clock input mode the HXT oscillator is switched off and XT1_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{HXT_ext}	External user clock source frequency	1	-	24	MHz	
t_{CHCX}	Clock high time	10	-	-	ns	
t_{CLCX}	Clock low time	10	-	-	ns	
t_{CLCH}	Clock rise time	2	-	15	ns	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	2	-	15	ns	High (90%) to low level (10%) fall time
Du_{E_HXT}	Duty cycle	40	-	60	%	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
V_{IL}	Input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Note:

1. Guaranteed by characterization, not tested in production.

7.3.3 External 32.768 kHz Low Speed Crystal Characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input clock frequency	External crystal	-	32.768	-	kHz
Temperature	-	-40	-	85	℃
V_{DD}	-	2.5	-	5.5	V

7.3.3.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R
32.768 kHz	20 pF	20 pF	without

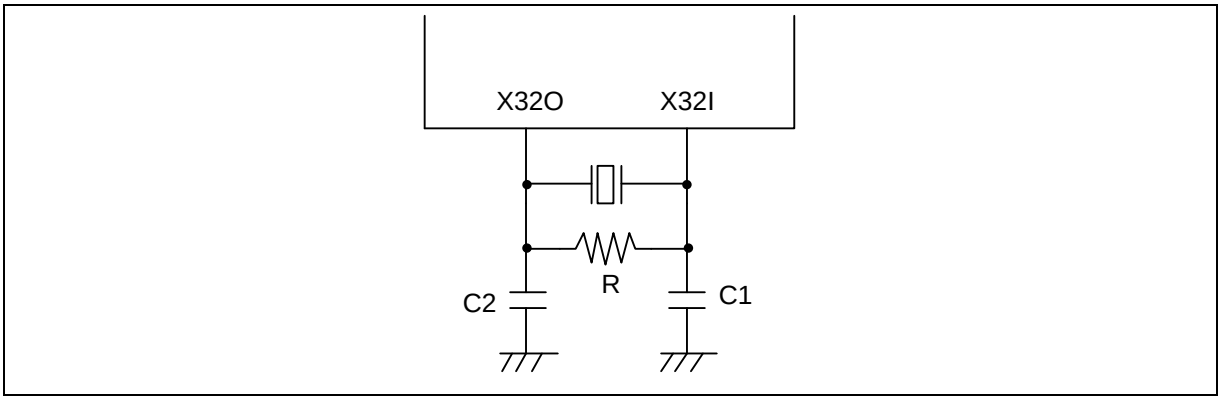
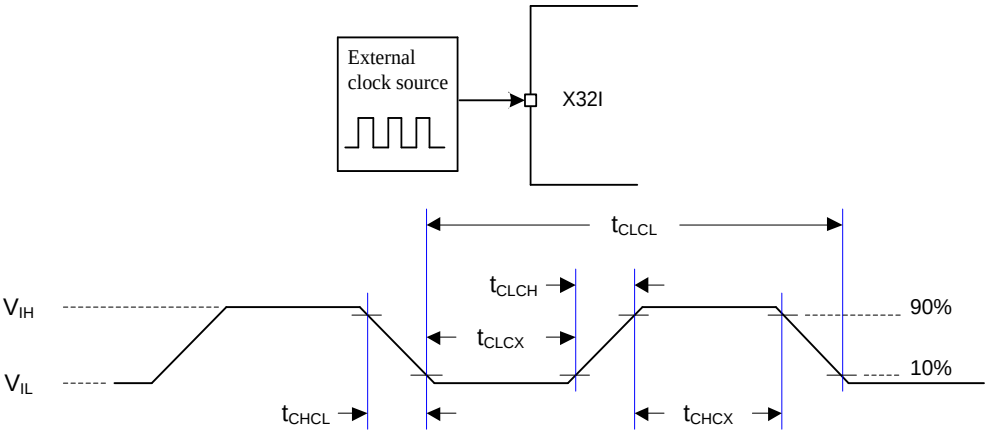


Figure 7-2 Typical Crystal Application Circuit

7.3.4 External 32.768 kHz Low Speed Clock Input Signal Characteristics

For clock input mode the LXT oscillator is switched off and X32I is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{LSE_ext}	External clock source frequency	-	32.768	-	kHz	
t_{CHCX}	Clock high time	450	-	-	ns	
t_{CLCX}	Clock low time	450	-	-	ns	
t_{CLCH}	Clock rise time	-	-	50	ns	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	50	ns	High (90%) to low level (10%) fall time
Du_{E_LXT}	Duty cycle	40	-	60	%	
Xin_VIH	LXT input pin input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
Xin_VIL	LXT input pin input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Note:

1. Guaranteed by design, not tested in production

7.3.5 Internal 22.1184 MHz High Speed Oscillator

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage[1]	-	2.5	-	5.5	V
Center Frequency	-	-	22.1184	-	MHz
Calibrated Internal Oscillator Frequency	+25 ℃; V_{DD} = 5 V	-1	-	+1	%
	-40 ℃ ~ +85 ℃; V_{DD} = 2.5 V ~ 5.5 V	-3	-	+3	%
Operation Current	V_{DD} = 5 V	-	500	-	uA

7.3.6 Internal 10 kHz Low Speed Oscillator

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage[1]	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	kHz
Calibrated Internal Oscillator Frequency	+25 ℃; V_{DD} = 5 V	-30	-	+30	%
	-40 ℃ ~ +85 ℃; V_{DD} = 2.5 V ~ 5.5 V	-50	-	+50	%

Note: Internal operation voltage comes from LDO.

7.4 Analog Characteristics

7.4.1 LDO and Power Management Specifications

PARAMETER	MIN	TYP	MAX	UNIT	NOTE
Input Voltage	2.5		5.5	V	V_{DD} input voltage
Output Voltage	1.62	1.8	1.98	V	V_{DD} > 2.5 V
Temperature	-40	25	85	℃	
Cbp	-	1	-	uF	Resr = 1Ω

Notes:

1. It is recommended that a 1 uF or higher capacitor and a 100 nF bypass capacitor are connected between V_{DD} and the closest V_{SS} pin of the device.

2. To ensure power stability, a 1 uF (Cbp) must be connected between LDO pin and the closest VSS pin of the device.

7.4.2 Low Voltage Reset Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operation voltage	-	1.7	-	5.5	V
Quiescent current	V_{DD} = 5.5 V	-	-	5	uA
Temperature	-	-40	25	85	℃
Threshold voltage		1.7	2.0	2.4	V
Hysteresis	-	0	0	0	V

7.4.3 Brown-out Detector Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operation voltage	-	2	-	5.5	V
Quiescent current	AV_{DD} = 5.5 V	-	-	125	μA
Temperature	-	-40	25	85	℃
Brown-out voltage	BOV_VL[1:0] = 11	4.3	4.5	4.7	V
	BOV_VL [1:0] = 10	3.6	3.8	4.0	V
	BOV_VL [1:0] = 01	2.6	2.7	2.8	V
	BOV_VL [1:0] = 00	2.1	2.2	2.3	V
Hysteresis	-	30	-	150	mV

7.4.4 Power-On Reset Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Temperature	-	-40	25	85	℃
Reset voltage	V+	-	2	-	V
Quiescent current	Vin>reset voltage	-	1	-	nA

7.4.5 USB PHY Specifications

7.4.5.1 USB DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input high (driven)		2.0			V
V_{IL}	Input low				0.8	V
V_{DI}	Differential input sensitivity	|PADP-PADM|	0.2			V
V_{CM}	Differential common-mode range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single-ended receiver threshold		0.8		2.0	V
	Receiver hysteresis			200		mV
V_{OL}	Output low (driven)		0		0.3	V
V_{OH}	Output high (driven)		2.8		3.6	V
V_{CRS}	Output signal cross voltage		1.3		2.0	V
R_{PU}	Pull-up resistor		1.425		1.575	kΩ
R_{PD}	Pull-down resistor		3.0		3.6	kΩ
V_{TRM}	Termination Voltage for upstream port pull up (RPU)			10		V
Z_{DRV}	Driver output resistance	Steady state drive*			20	Ω
C_{IN}	Transceiver capacitance	Pin to GND	2.0			pF

Note: Driver output resistance doesn't include series resistor resistance.

7.4.5.2 USB Full-Speed Driver Electrical Characteristics

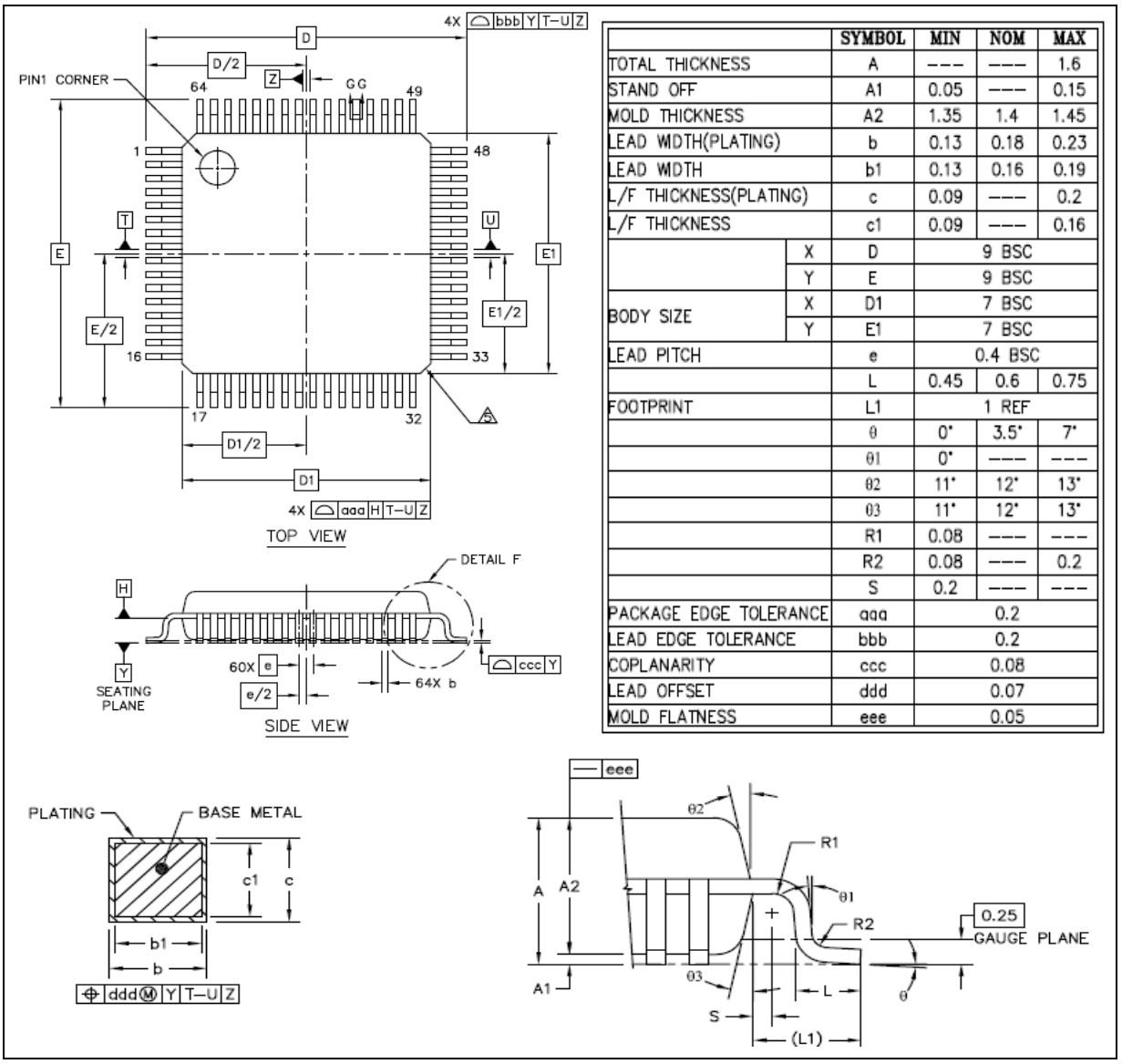
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
T_{FR}	Rising time	C_L = 50p	4		20	ns
T_{FF}	Falling time	C_L = 50p	4		20	ns
T_{FRFF}	Rising and falling time matching	$T_{FRFF} = T_{FR}/T_{FF}$	90		111.11	%

7.4.5.3 USB Power Dissipation

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDDREG} (Full Speed)	VDDD and VDDREG Supply Current (Steady State)	Standby		50		uA
		Input mode				uA
		Output mode				uA

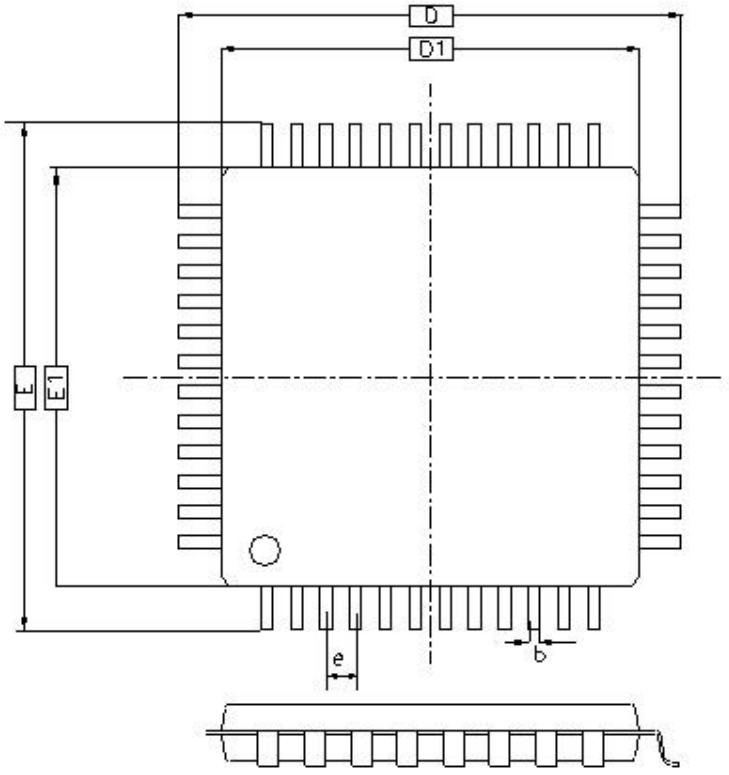
8 PACKAGE DIMENSIONS

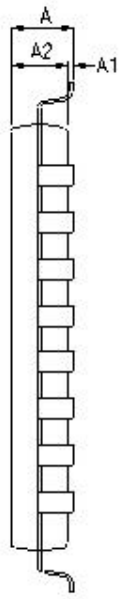
8.1 64L LQFP (7x7x1.4 mm footprint 2.0 mm)

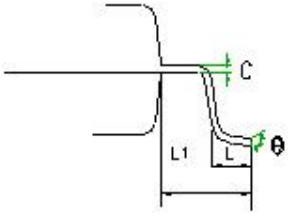


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

8.2 48L LQFP (7x7x1.4 mm footprint 2.0 mm)



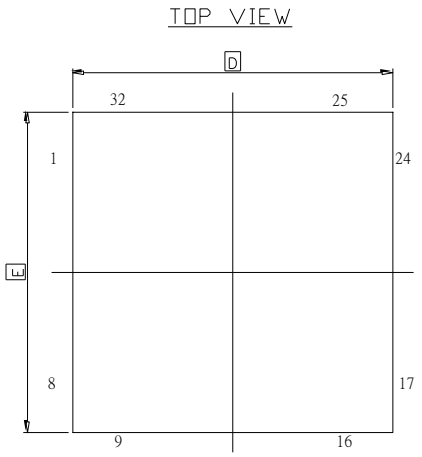


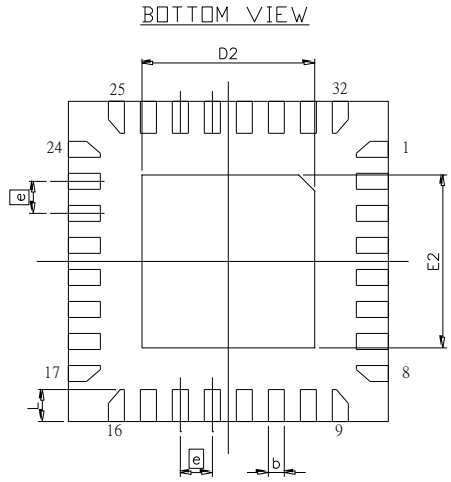


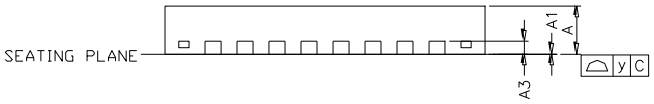
COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN	NOM.	MAX.	MIN	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D1	6.90	7.00	7.10	0.272	0.276	0.280
E1	6.90	7.00	7.10	0.272	0.276	0.280
e	0.35	0.50	0.65	0.014	0.020	0.280
D	8.9	9.00	9.10	0.350	0.354	0.358
E	8.9	9.00	9.10	0.350	0.354	0.358
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
C	0.09	—	0.20	0.0035	—	0.0079
θ	0°	—	7°	0°	—	7°
b	0.17	0.22	0.27	0.007	0.0087	0.011

8.3 33L QFN (5x5x0.8 mm)







SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0275	0.0295	0.0315
A1	0	0.02	0.05	0	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	5.00 BSC			0.197 BSC		
E	5.00 BSC			0.197 BSC		
e	0.50 BSC			0.0197 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
y	0.10			0.0039		
D2	3.20	3.40	3.60	0.124	0.138	0.142
E2	3.20	3.40	3.60	0.124	0.138	0.142

9 REVISION HISTORY

Date	Revision	Description
2020.01.21	2.00	Preliminary version.

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.