8-bit Microcontroller

KM101EF56/57/76 Series
Datasheet

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KM101EF56/57/76 Series

8-bit Single-chip Microcontroller

■ Overview

The KM101E series of 8-bit single-chip microcomputers (the memory expansion version of KM101C series) incorporate multiple types of peripheral functions. This chip series is well suited for camera, VCR, MD, TV, CD, LD, printer, telephone, home automation, pager, air conditioner, PPC, fax machine, music instrument and other applications.
This LSI brings to embedded microcomputer applications flexible, optimized hardware configurations and a simple efficient instruction set. KM101EF57 series has an internal 128 KB of ROM and 6 KB of RAM. Peripheral functions include 5 external interrupts, 29 internal interrupts including NMI, 12 timer counters, 4 types of serial interfaces, A/D converter, D/A converter, LCD driver, 2 types of watchdog timer, data automatic function and buzzer output. The system configuration is suitable for in camera, timer selector for VCR, CD player, or minicomponent.

With 5 oscillation systems (high-speed (internal frequency: 20 MHz), high-speed (crystal/ceramic frequency: max. 10 MHz) / low-speed (internal frequency: 30 kHz), low-speed (crystal/ceramic frequency: 32.768 kHz) and PLL: frequency multiplier of high frequency) contained on the chip, the system clock can be switched to high-speed frequency input (NORMAL mode), PLL input (PLL mode), or to low-speed frequency input (SLOW mode). The system clock is generated by dividing the oscillation clock or PLL clock. The best operation clock for the system can be selected by switching its frequency ratio by programming. High speed mode has the normal mode which is based on the clock dividing fpll, (fpll is generated by original oscillation and PLL), by 2 (fpll/2), and the double speed mode which is based on the clock not dividing fpll.

A machine cycle (minimum instruction execution time) in the normal mode is 200 ns when the original oscillation fosc is 10 MHz (PLL is not used). A machine cycle in the double speed mode, in which the CPU operates on the same clock as the external clock, is 100 ns when fosc is 10 MHz. A machine cycle in the PLL mode is 50 ns (maximum).

■ Product Summary

This datasheet describes the following model.

Model	ROM Size	RAM Size	Classification	Package
KM101EF76K	256 KB	10 KB	Flash EEPROM version	LQFP128-P-1818C
KM101EF57G	128 KB	6 KB		LQFP080-P-1414A TQFP080-P-1212F
KM101EF56K	256 KB	10 KB		QFP100-P-1818B

Note) DMOD internal pull-up resistor is in only Flash EEPROM version.
When using In-circuit Emulator, it is necessary to connect the pull-up resistor on the circuit board.

■ Features

- ROM / RAM capacity

  KM101EF76K: ROM 256 KB / RAM 10 KB
  KM101EF57G: ROM 128 KB / RAM 6 KB
  KM101EF56K: ROM 256 KB / RAM 10 KB

- Package:

  KM101EF76K: LQFP128-P-1818C (18 mm × 18 mm / 0.5 mm pitch)
  KM101EF57G: LQFP080-P-1414A (14 mm × 14 mm / 0.65 mm pitch)
  TQFP080-P-1212F (12 mm × 12 mm / 0.5 mm pitch)
  KM101EF56K: QFP100-P-1818B (18 mm × 18 mm / 0.65 mm pitch)

- Machine Cycle:

  High-speed mode
  0.05 µs / 20 MHz (2.7 V to 5.5 V)
  0.125 µs / 8 MHz (1.8 V to 5.5 V)
  Low-speed mode
  62.5 µs / 32 kHz (1.8 V to 5.5 V)

- Clock Gear Circuit:

  Internal system clock speed is changeable by selecting division ratio of oscillation clock. (Divided by 1, 2, 4, 16, 32, 64, 128)

- Oscillation Circuit: 4 types

  High-speed (Internal oscillation: frc), High-speed (crystal/ceramic: fosc),
  Low-speed (Internal oscillation: frcs), Low-speed (crystal/ceramic: fx)
  High-speed internal oscillation 20 MHz / 16 MHz (selectable)
  Low-speed internal oscillation 30 kHz

- Clock Multiplication Circuit:

  PLL circuit output clock (fpll) fosc multiplied by 2, 3, 4, 5, 6, 8, 10,1/2 × frc multiplied by 4, 5 enabled
  * When clock multiplication circuit is not used, fpll = fosc or fpll = frc
  * Selectable from high-speed clock for peripheral functions (fpll-div) fpll, fpll divided by 2, 4, 8, 16

- Memory bank

  Data memory space is expanded by the bank system.
  Bank for the source address / Bank for the destination address.

- Operation Mode

  NORMAL mode (high-speed mode)
  PLL mode
  SLOW mode (low-speed mode)
  HALT mode
  STOP mode
  and operation clock switching

- Operating Voltage

  1.8 V to 5.5 V

- Operating Ambient Temperature:

  –40°C to +85°C

■ Features (continued)

• Interrupts

Interrupts	KM101EF76K 36 sets	KM101EF57G 34 sets	KM101EF56K 36 sets
Overrun interrupt			
Non-maskable interrupt (NMI)	○	○	○
Timer interrupt			
Timer 0 interrupt	○	○	○
Timer 1 interrupt	○	○	○
Timer 2 interrupt	○	○	○
Timer 3 interrupt	○	○	○
Timer 4 interrupt	○	○	○
Timer 6 interrupt	○	○	○
Timer 7 interrupt	○	○	○
Time-base interrupt	○	○	○
Timer 7 compare register 2 match interrupt	○	○	○
Timer 8 interrupt	○	○	○
Timer 8 compare register 2 match interrupt	○	○	○
PWM overflow interrupt	○	○	○
PWM under flow interrupt	○	○	○
Timer 9 compare register 2 match interrupt	○	○	○
24H timer interrupt	○	○	○
Alarm match interrupt	○	○	○
Serial interrupt			
LIN interrupt	○	○	○
Serial 0 interrupt	○	○	○
Serial 0 UART reception interrupt	○	○	○
Serial 1 interrupt	○	○	○
Serial 1 UART reception interrupt	○	○	○
Serial 2 interrupt	○	○	○
Serial 2 UART reception interrupt	○	○	○
Serial 3 interrupt	○	—	○
Serial 3 UART reception interrupt	○	—	○
Serial 4 interrupt	○	○	○
Serial 4 stop condition interrupt	○	○	○
A/D interrupt			
A/D conversion interrupt	○	○	○
Data automatic transfer interrupt			
ATC1 interrupt	○	○	○
Low voltage detection interrupt			
Low voltage detection interrupt	○	○	○
External interrupt			
IRQ0 (Edge selection, noise filter connectable)	○	○	○
IRQ1 (Edge selection, noise filter connectable)	○	○	○
IRQ2 (Edge selection, both edge interrupt, noise filter connectable)	○	○	○
IRQ3 (Edge selection, both edge interrupt, noise filter connectable)	○	○	○
IRQ4 (Edge selection, both edge interrupt, noise filter connectable, KEY scan interrupt)	○	○	○

■ Features (continued)

- Timer Counter: 12 sets

General-purpose 8-bit timer × 5 sets
General-purpose 16-bit timer × 2 sets
General-purpose 16-bit timer × 2 sets
Motor control 16-bit timer × 1 set
8-bit free-run timer × 1 set
Time-base timer × 1 set
Baud rate timer × 1 set
24H timer × 1 set

Timer 0 (General-purpose 8-bit timer)
Square wave output (Timer pulse output), added pulse (2 bits) type PWM output can be output to large current pin TM0IOB, event count, simple pulse width measurement
Double-buffered compare register (×1)* Function in KM101EF76K and KM101EF56K
Clock source:
fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, timer A output
Real-time control:
Timer (PWM) output is controlled among the three values: "Fixed to High", "Fixed to Low", or "Hi-Z" at falling edge of external interrupt 0 (IRQ0)

Timer 1 (General-purpose 8-bit timer)
Square wave output (Timer pulse output), event count
16-bit cascade connection (connected with timer 0)
Double-buffered compare register (×1)* Function in KM101EF76K and KM101EF56K
Clock source:
fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, timer A output

Timer 2 (General-purpose 8-bit timer)
Square wave output (Timer pulse output), added pulse (2 bits) type PWM output can be output to large current pin TM2IOB, event count, simple pulse width measurement,
24-bit cascade connection (connected with timer 0, 1), timer synchronous output
Double-buffered compare register (×1)
Clock source:
fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, timer A output
Real-time control:
Timer (PWM) output is controlled among the three values: "Fixed to High", "Fixed to Low", or "Hi-Z" at falling edge of external interrupt 0 (IRQ0)

Timer 3 (General-purpose 8-bit timer)
Square wave output (Timer pulse output), event count
16-bit cascade connection (connected with timer 2), 32-bit cascade connection (connected with timer 0, 1, 2)
Double-buffered compare register (×1)
Clock source:
fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, timer A output

Timer 4 (General-purpose 8-bit timer)
Square wave output (Timer pulse output), added pulse (2bit) type PWM output, event count, simple pulse width measurement
Clock source:
fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, timer A output

■ Features (continued)

- Timer Counter (continued)

Timer 6 (8-bit free-run timer, time-base timer)

8-bit free-run timer

Clock source:

fpll-div, fpll-div/2^2, fpll-div/2^3, fpll-div/2^{12}, fpll-div/2^{13}, fs, fslow, fslow/2^2, fslow/2^3, fslow/2^{12}, fslow/2^{13}

Time-base timer

Interrupt generation cycle:

fpll-div/2^7, fpll-div/2^8, fpll-div/2^9, fpll-div/2^{10}, fpll-div/2^{13}, fpll-div/2^{15}, fslow/2^7, fslow/2^8, fslow/2^9, fslow/2^{10}, fslow/2^{13}, fslow/2^{15}

Timer 7 (General-purpose 16-bit timer)

Clock source:

fpll-div, fs, external clock, timer A output, serial 0 transfer clock output, timer 6 compare match cycle divided by 1, 2, 4, 16

Hardware configuration:

Double-buffered compare register (×2)

Double-buffered input capture register (×2)

Timer interrupt (×2 vector)

Timer function:

Square wave output (Timer pulse output), high-precision PWM output (cycle/duty continuous changeable) can be output to large current pin TM7IOB, timer synchronous output, event count, input capture function (both edges operable)

Real-time control:

Timer (PWM) output is controlled among the three values: "Fixed to High", "Fixed to Low", or "Hi-Z" at falling edge of external interrupt 0 (IRQ0)

Timer 8 (General-purpose 16-bit timer)

Clock source:

fpll-div, fs, external clock, timer A output, timer 6 compare match cycle divided by 1, 2, 4, 16

Hardware configuration:

Double-buffered compare register (×2)

Double-buffered input capture register (×1)

Timer interrupt (×2 vector)

Timer function:

Square wave output (Timer pulse output), high-precision PWM output (cycle/duty continuous changeable) can be output to large current pin TM8IOB, event count, pulse width measurement, input capture function (both edges operable)

32-bit cascade connection (connected with timer 7), 32-bit PWM output, input capture is available in 32-bit cascade

Timer 9 (Motor control 16-bit timer)

Clock source:

fpll-div, fs, external clock, Timer A output divided by 1, 2, 4, 16

Hardware configuration:

Double-buffered compare register (×2)

Timer interrupt (×3 vector)

Timer function:

Square wave output (Timer pulse output) can be changed to large current output, complementary

3-phase PWM output, triangle wave and saw tooth wave are supported, dead time insertion available, event count

Pin output control:

PWM output control is possible by external interrupt 0 to 4 (IRQ 0 to 4) ("Hi-z", output data fixed)

Timer A (baud rate timer)

Clock output for peripheral functions

Clock source:

fpll-div divided by 1/1, 2, 4, 8, 16, 32, and fs divided by 2, 4

■ Features (continued)

- Timer Counter (continued)

  24H timer

  Clock source (Usable frequency)

  fpll (4 MHz, 4.19 MHz, 5 MHz, 8 MHz, 8.38 MHz, 10 MHz, 16 MHz, 16.77 MHz, 20 MHz), fx (32.768 kHz), frc (20 MHz, 16 MHz), frcs (30 kHz)

  Hardware configuration:

  0.5 seconds counter, minute counter, hour counter

  Alarm compare register (in 0.5 seconds, in minutes, in hours) (×1)

  Timer interrupt (×2 vector)

  Timer function:

  Interval function (interrupts every 0.5 seconds, 1 second, 1 minute, 1 hour, 24 hours)

  Alarm function

- Watchdog timer

  Overrun detection cycle is selectable from $fs/2^{16}$, $fs/2^{18}$, $fs/2^{20}$

  Forced to reset inside LSI by hardware when a software processing error is detected twice

- Watchdog timer2

  Overrun detection cycle is selectable from $frcs/2^4$, $frcs/2^5$, $frcs/2^6$, $frcs/2^7$, $frcs/2^8$, $frcs/2^9$, $frcs/2^{10}$, $frcs/2^{11}$, $frcs/2^{12}$, $frcs/2^{13}$, $frcs/2^{14}$, $frcs/2^{15}$

  Forced to reset inside LSI by hardware when a software processing error is detected twice

- Synchronous output function (Timer synchronous output, interrupt synchronous output)

  Latch data is output from port 8 at the event timing of synchronous output signal of timer 1, timer 2, timer 7, or external interrupt2 (IRQ2)

- Buzzer Output

  Output frequency can be selected from $fpll\text{-}div/2^9$, $fpll\text{-}div/2^{10}$, $fpll\text{-}div/2^{11}$, $fpll\text{-}div/2^{12}$, $fpll\text{-}div/2^{13}$, $fpll\text{-}div/2^{14}$, $fslow/2^3$, $fslow/2^4$

- A/D converter

  KM101EF76K: 10-bit × 24 channels

  KM101EF57G: 10-bit × 12 channels

  KM101EF56K: 10-bit × 24 channels

- D/A converter

  KM101EF76K: 8-bit × 4 channels

  KM101EF57G: 8-bit × 2 channels

  KM101EF56K: 8-bit × 4 channels

- Data automatic transfer: 1 system

  Data is automatically transferred in all memory space

  External interrupt activation/internal event activation/software activation

  Max. 255 byte continuous transfer

  Serial continuous transmission and reception is supported

  Burst transfer function (Including interrupt emergency stop)

■ Features (continued)

- Serial interface

KM101EF76K: 5 systems
KM101EF57G: 4 systems
KM101EF56K: 5 systems

Serial interface 0 (Hardware LIN / Full duplex UART / Synchronous serial interface)
- Synchronous serial interface
  - Transfer clock source:
    - fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4, Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock
  - MSB/LSB first selectable, 1 to 8 bits of arbitrary transfer
  - Continuous transmission, continuous reception, continuous transmission and reception are available.
- Full duplex UART (Baud rate timer: selected from timer 0 to 4, or timer A)
  - Parity check, overrun error/framing error are detected
  - Transfer bits 7 to 8 are selectable
  - Hardware LIN
    - Synch Break generation, Wake-up detection, Synch Break detection, Synch Field measurement are available

Serial interface 1 (Full duplex UART / Synchronous serial interface)
- Synchronous serial interface
  - Transfer clock source:
    - fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4,Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock
  - MSB/LSB first selectable, 1 to 8 bits of arbitrary transfer
  - Continuous transmission, continuous reception, continuous transmission and reception are available.
- Full duplex UART (Baud rate timer: selected from timer 0 to 4, or timer A)
  - Parity check, overrun error/framing error are detected
  - Transfer bits 7 to 8 are selectable

Serial interface 2 (Full duplex UART / Synchronous serial interface)
- Synchronous serial interface
  - Transfer clock source:
    - fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4, Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock
  - MSB/LSB first selectable, 1 to 8 bits of arbitrary transfer
  - Continuous transmission, continuous reception, continuous transmission and reception are available.
- Full duplex UART (Baud rate timer: selected from timer 0 to 4, or timer A)
  - Parity check, overrun error/framing error are detected
  - Transfer bits 7 to 8 are selectable

Serial interface 3 (Full duplex UART / Synchronous serial interface) * Function in KM101EF76K and KM101EF56K
- Synchronous serial interface
  - Transfer clock source:
    - fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4, Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock
  - MSB/LSB first selectable, 1 to 8 bits of arbitrary transfer
  - Continuous transmission, continuous reception, continuous transmission and reception are available.
- Full duplex UART (Baud rate timer: selected from timer 0 to 4, or timer A)
  - Parity check, overrun error/framing error are detected
  - Transfer bits 7 to 8 are selectable

■ Features (continued)

- Serial interface (continued)

  Serial interface 4 (Multi master IIC / Synchronous serial interface)

  Synchronous serial interface

  Transfer clock source:

  fpll-div/2, fpll-div/4, fpll-div/8, fpll-div/32, fs/2, fs/4, Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock

  MSB/LSB first selectable, 1 to 8 bits of arbitrary transfer

  Continuous transmission, continuous reception, continuous transmission and reception are available.

  Multi master IIC

  7, 10-bit slave address is settable

  General call communication mode is supported

- Auto reset circuit

- Low voltage detection circuit

- Clock Monitoring Function

- LED driver: 8 sets

- LCD driver

  Segment output

  KM101EF76K: Max. 55 pins (SEG0 to SEG54)

  KM101EF57G: Max. 41 pins (SEG0 to SEG40)

  KM101EF56K: Max. 55 pins (SEG0 to SEG54)

  Segment output pins can be switched to I/O ports in 1 bit.

  * At reset, Segment outputs are input ports.

  Common output: 4 pins

  COM0 to 3 can be switched to I/O ports in 1 bit.

  Display mode selection

  Static

  1/2 duty, 1/2 bias

  1/3 duty, 1/3 bias

  1/4 duty, 1/3 bias

  LCD driver clock

  When the source clock is the main clock (fpll)

  $1/2^{18}$, $1/2^{17}$, $1/2^{16}$, $1/2^{15}$, $1/2^{14}$, $1/2^{13}$, $1/2^{12}$, $1/2^{11}$

  When the source clock is the sub clock (fslow)

  $1/2^{9}$, $1/2^{8}$, $1/2^{7}$, $1/2^{6}$

  Timer 0 to 4, Timer A output

  LCD power supply

  LCD power supply is separated from V_{DD5}. (can be used when $V_{LC1} \leq V_{DD5}$)

  External power supply voltage can be selectable. (Supply voltage is supplied from V_{LC1}, V_{LC2}, and V_{LC3})

  Internal dividing resistors (External power supply voltage is divided the voltage input to V_{LC1} by internal resistors.)

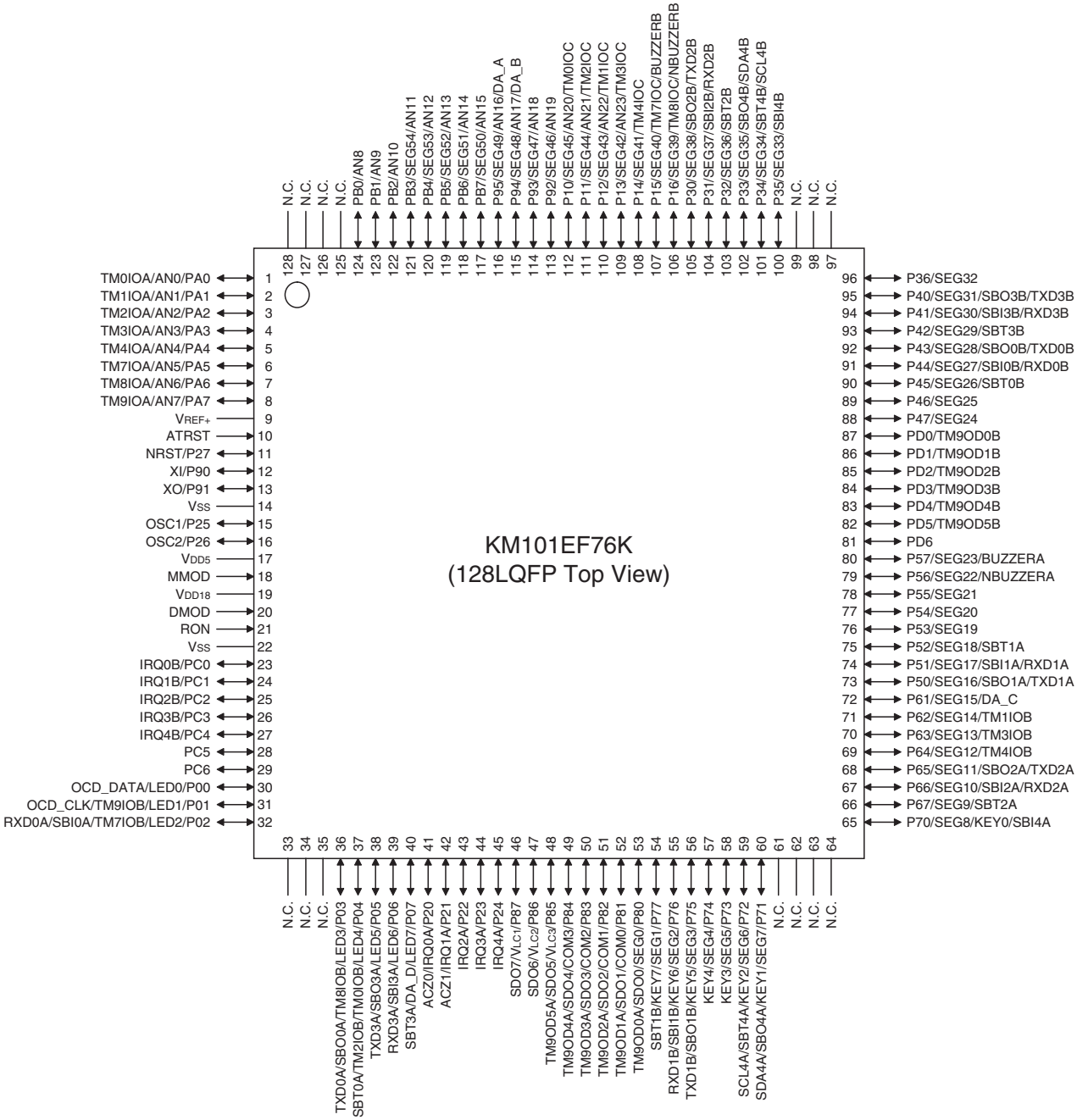
■ Features (continued)

• Ports

Ports	KM101EF76K (pins)	KM101EF57G (pins)	KM101EF56K (pins)
I/O ports	104	70	90
LCD segment	55	41	55
LCD common	4	4	4
Serial interface communication	30	21	30
Timer I/O	34	21	28
Buzzer output	4	2	4
A/D input	24	16	24
External interrupt	10	5	5
LCD power supply	3	3	3
LED driver (high-current)	8	8	8
High-speed oscillation	2	2	2
Low-speed oscillation	2	2	2
D/A output	4	2	4
Special function pins	10	10	10
Operation mode input	3	3	3
Reset input	1	1	1
Analog reference voltage input	1	1	1
Power supply	4	4	4

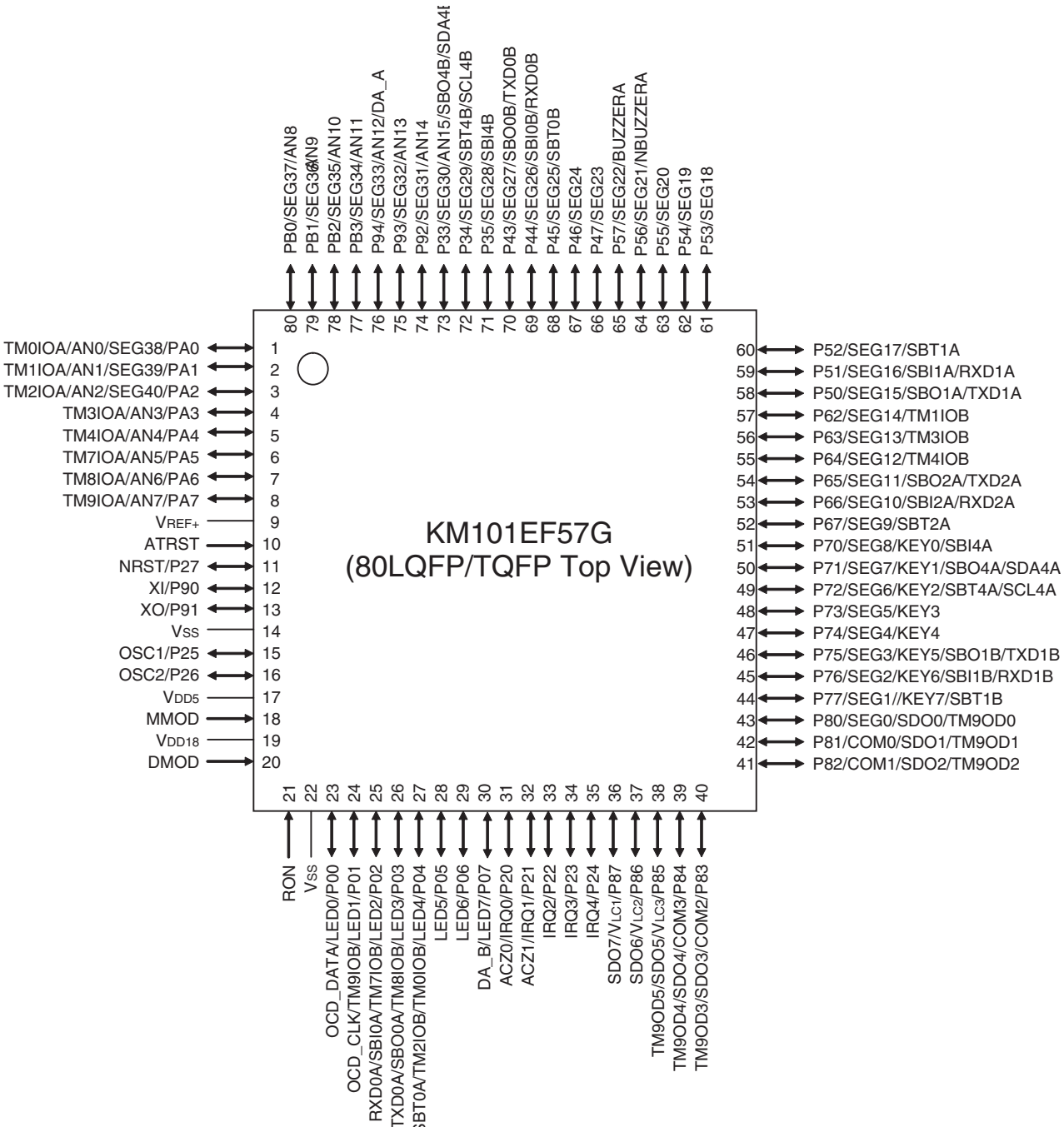
■ Pin Description

• KM101EF76K (LQFP128-P-1818C)



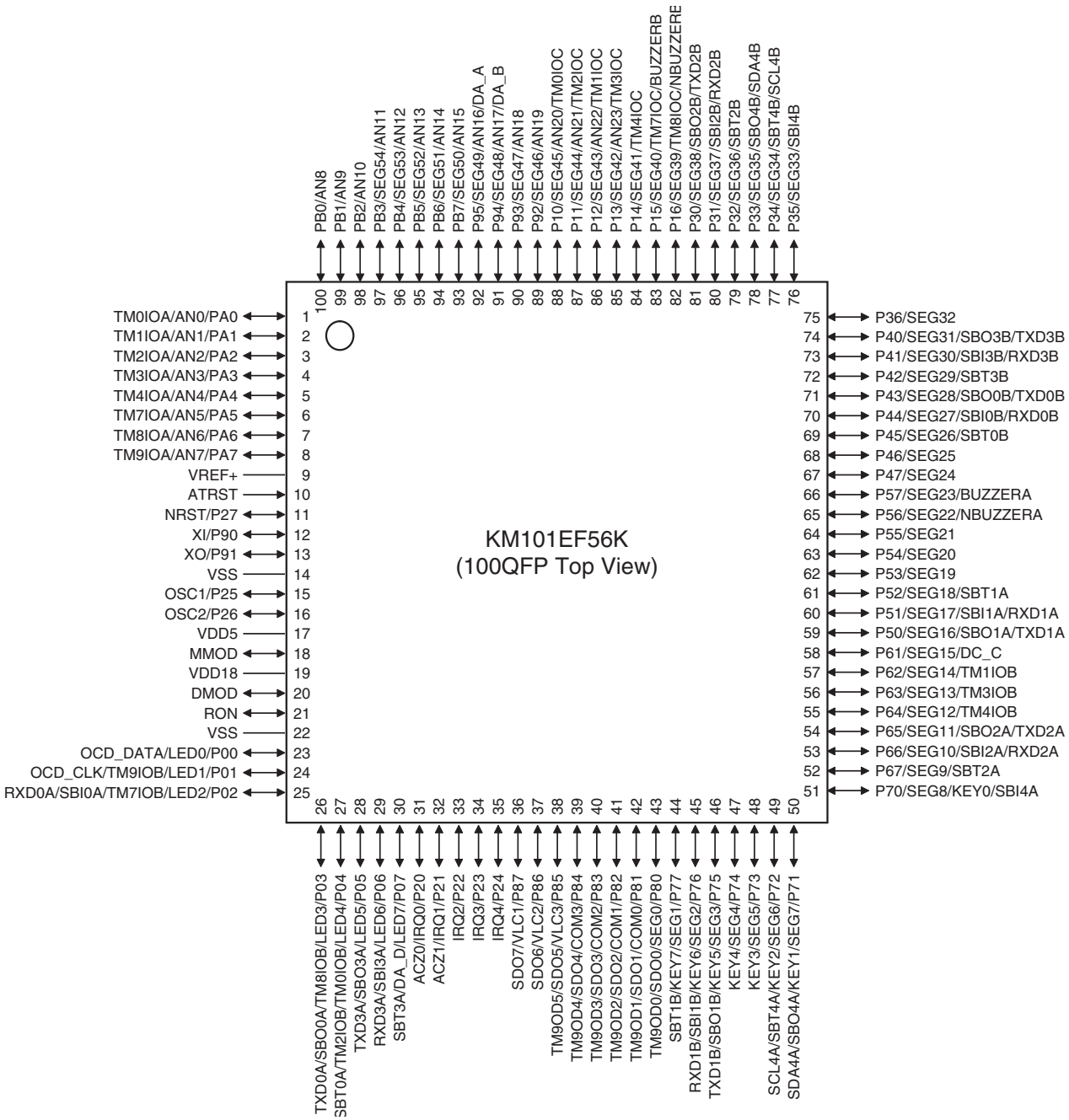
■ Pin Description (continued)

• KM101EF57G (LQFP080-P-1414A, TQFP080-P-1212F)



■ Pin Description (continued)

• KM101EF56K (QFP100-P-1818B)



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