8-bit Microcontroller

KM101EF50 Series
Datasheet

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Mar 23, 2011 Rev 1.00

KM101EF50 Series

8-bit Single-chip Microcontroller

■ Overview

The KM101E series of 8-bit single-chip microcomputers (the memory expansion version of KM101C series) incorporate multiple types of peripheral functions. This chip series is well suited for camera, VCR, MD, TV, CD, LD, printer, telephone, home automation, pager, air conditioner, PPC, fax machine, music instrument and other electrical appliances.

This LSI has embedded flexible microcomputer applications, optimized hardware configurations and a simple yet efficient instruction set. KM101EF50D has an internal 64 KB of ROM and 4 KB of RAM. Peripheral functions include 5 external interrupts, 25 internal interrupts including NMI, 11 timer counters, 4 types of serial interfaces, A/D converter, LCD driver, watchdog timer and buzzer output. The system configuration is suitable for system control microcontrollers such as cameras, timer selectors for VCR, CD players or minicomponents.

With 4 oscillation systems (high-speed internal frequency: 20 MHz, high-speed crystal/ceramic frequency: max. 10 MHz / low-speed crystal/ceramic frequency: 32.768 kHz and PLL: frequency multiplier of the high-speed frequency) contained in the chip, the system clock can be switched to high-speed frequency input (NORMAL mode), PLL input (PLL mode) or low-speed frequency input (SLOW mode). The system clock is generated by dividing the oscillation clock or PLL clock. The optimum operating clock for the system can be selected by switching its frequency ratio by programming.

The machine cycle (minimum instruction execution time) is 100 ns when the external oscillation fosc is 10 MHz (PLL is not used). The machine cycle is 50 ns (maximum) when the internal oscillation frequency is 20 MHz (PLL is not used). A machine cycle in the PLL mode is 50 ns (maximum).

This datasheet describes the following model.

■ Product Summary

Model	ROM Size	RAM Size	Classification	Package
KM101EF50D	64 KB	4 KB	Flash EEPROM version	LQFP064-P-1414

■ Features

- Memory
  ROM capacity: 64 KB
  RAM capacity: 4 KB

- Package
  LQFP064-P-1414 (14 mm × 14 mm / 0.8 mm pitch)

- Machine Cycle
  High-speed mode
    0.05 µs / 20 MHz (2.7 V to 5.5 V)
    0.125 µs / 8 MHz (1.8 V to 5.5 V)
  Low-speed mode
    62.5 µs / 32 kHz (1.8 V to 5.5 V)

- Clock Gear Circuit:
  Variable internal system clock speed (fosc/1, fosc/2, fosc/4, fosc/16, fosc/64 and fosc/128)

- High-speed Clock (fpll-div) Gear Circuit for peripherals:
  Select among "Stop", fpll/1, fpll/2, fpll/4, fpll/8 and fpll/16.

- Oscillation Circuit
  High-speed: internal oscillation (frc) or crystal/ceramic (fosc)
  Low-speed: crystal/ceramic (fx)
  * High-speed internal oscillation: 20 MHz / 16 MHz (selectable)
  * 20 MHz can be selected only when internal high-speed oscillator is used without using external high-speed oscillator or low-speed oscillators.

- Clock Multiplication Circuit
  PLL output clock (fpll)
  fosc × n (n: 2, 3, 4, 5, 6, 8, 10)
  frc/2 × n (n: 4, 5)
  * When clock multiplication circuit is not used, fpll = fosc or fpll = frc

- Memory Bank
  Data memory space is expandable with the memory bank system. (16 banks with 64 KB each)
  Consists of banks for the source address and banks for the destination address.

- Operating Mode
  NORMAL Mode (high-speed mode)
  PLL Mode
  SLOW Mode (low-speed mode)
  HALT Mode
  STOP Mode
  Clock Transition Mode

- Operating Voltage
  1.8 V to 5.5 V

- Operating Ambient Temperature:
  –40°C to +85°C

■ Features (continued)

- Interrupt: 30 sets

<Processing error interrupt>
Non-maskable interrupt (NMI)
<Timer interrupts>
Timer 0 interrupt
Timer 1 interrupt
Timer 2 interrupt
Timer 3 interrupt
Timer 4 interrupt
Timer 6 interrupt
Time base interrupt
Timer 7 interrupt
Timer 7 compare register 2 match interrupt
Timer 8 interrupt
Timer 8 compare register 2 match interrupt
24H timer interrupt
Alarm match interrupt
<Serial interrupt>
Serial Interface 0 interrupt
Serial Interface 0 UART reception interrupt
Serial Interface 1 interrupt
Serial Interface 1 UART reception interrupt
Serial Interface 2 interrupt
Serial Interface 2 UART reception interrupt
Serial Interface 4 interrupt
Serial Interface 4 stop condition interrupt
<A/D interrupt>
A/D conversion interrupt
<Low voltage detection interrupt>
Low voltage detection interrupt
<External interrupt>
IRQ0: Edge selection, noise filter connectable
IRQ1: Edge selection, noise filter connectable
IRQ2: Edge selection, noise filter connectable, both edges interrupt
IRQ3: Edge selection, noise filter connectable, both edges interrupt
IRQ4: Edge selection, noise filter connectable, both edges interrupt, key scan interrupt

■ Features (continued)

- Timer Counter: 11 sets

General-purpose 8-bit timer: 5 sets
General-purpose 16-bit timer: 2 sets
8-bit free-run timer: 1 set
Time-base timer: 1 set
Baud rate timer: 1 set
24 H timer: 1 set

<Timer 0> (General-purpose 8-bit timer)
Square wave output (Timer pulse output), added pulse (2 bits) type PWM output, event count, simple pulse width measurement
Large current output selectable
Clock source :
fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, Timer A output
Real-time control:
Timer (PWM) output is controlled among the three values: "Fixed to High", "Fixed to Low",
or "Hi-Z" at falling edge of External Interrupt 0 (IRQ0)
Double-buffered compare register (×1)

<Timer 1> (General-purpose 8-bit timer)
Square wave output (Timer pulse output), event count, timer synchronous output, 16-bit cascade connection (connected with Timer 0)
Clock source:
fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, Timer A output
Double-buffered compare register (×1)

<Timer 2> (General-purpose 8-bit timer)
Square wave output (Timer pulse output), added pulse (2 bits) type PWM output, event count, simple pulse width measurement
Large current output selectable, 24-bit cascade connection (connected with Timer 0, 1), timer synchronous output
Clock source:
fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, Timer A output
Real-time control:
Timer (PWM) output is controlled among three status: "Fixed to High", "Fixed to Low",
or "Hi-Z" at falling edge of External Interrupt 0 (IRQ0)
Double-buffered compare register (×1)

<Timer 3> (General-purpose 8-bit timer)
Square wave output (Timer pulse output), event count, 16-bit cascade connection (connected with Timer 2),
32-bit cascade connection (connected with Timer 0, 1, 2)
Double-buffered compare register (×1)
Clock source:
fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, Timer A output

<Timer 4> (General-purpose 8-bit timer)
Square wave output (Timer pulse output), added pulse (2 bits) type PWM output, event count, simple pulse width measurement
Clock source:
fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, Timer A output

<Timer 6> (8-bit free-run timer, time-base timer)
8-bit free-run timer
Clock source:
fpll-div, fpll-div/2^2, fpll-div/2^3, fpll-div/2^{12}, fpll-div/2^{13}, fs, fslow, fslow/2^2, fslow/2^3, fslow/2^{12}, fslow/2^{13}
Time base timer
Interrupt generation cycle:
fpll-div/2^7, fpll-div/2^8, fpll-div/2^9, fpll-div/2^{10}, fpll-div/2^{13}, fpll-div/2^{15}, fslow/2^7, fslow/2^8, fslow/2^9, fslow/2^{10},
fslow/2^{13}, fslow/2^{15}

■ Features (continued)

<Timer 7> (General-purpose 16-bit timer)

Clock source:

fpll-div, fs, external clock, Timer A output, Serial Interface 0 transfer clock output, Timer 6 compare match cycle divided by 1, 2, 4, 16

Hardware configuration:

Double-buffered compare register (×2)
Double-buffered input capture register (×2)
Timer interrupt (×2 vector)

Timer function

Square wave output (Timer pulse output), high-precision PWM output (cycle/duty continuous changeable), large current selectable, timer synchronous output, event count, input capture function (both edges operable)

Real-time control

Timer (PWM) output is controlled among the three values: "Fixed to High", "Fixed to Low" or "Hi-Z" at falling edge of External Interrupt 0 (IRQ0)

<Timer 8> (General-purpose 16-bit timer)

Clock source:

fpll-div, fs, external clock, Timer A output, Timer 6 compare match cycle divided by 1, 2, 4, 16

Hardware configuration

Double-buffered compare register (×2)
Input capture register (×1)
Timer interrupt (×2 vector)

Timer function

Square wave output (Timer pulse output), high-precision PWM output (cycle/duty continuous changeable), large current selectable, event count, pulse width measurement, input capture function (both edges operable)
32-bit cascade connection (connected with Timer 7), 32-bit PWM output, input capture is available in 32-bit cascade

<Timer A> (baud rate timer)

Clock output for peripheral functions

Clock source:

fpll-div divided by 1, 2, 4, 8, 16, 32, fs divided by 2, 4

<24H timer>

Clock source (Usable frequency):

fpll (4 MHz, 4.19 MHz, 5 MHz, 8 MHz, 8.38 MHz, 10 MHz, 16 MHz, 16.77 MHz, 20 MHz), fx (32.768 kHz), frc (20 MHz, 16 MHz)

Hardware configuration

0.5 second counter, minute counter, hour counter
Alarm compare register (in 0.5 second, in minutes, in hours) (×1)
Timer interrupt (×2 vector)

Timer Function

Interval function (interrupts every 0.5 second, 1 second, 1 minute, 1 hour, 24 hours)
Alarm function

- Watchdog timer

  Software processing error detection cycle is selectable from $fs/2^{16}$, $fs/2^{18}$, $fs/2^{20}$.
  System reset is generated by the hardware when software processing error is detected twice.

- Synchronous output function (Timer synchronous output, interrupt synchronous output)

  Latch data is output from Port 8 at the event timing of synchronous output signal of Timer 1, Timer 2, Timer 7, or external interrupt 2 (IRQ2)

■ Features (continued)

- Buzzer Output

  Output frequency can be selected from fpll-div/2^9, fpll-div/2^{10}, fpll-div/2^{11}, fpll-div/2^{12}, fpll-div/ 2^{13}, fpll-div/2^{14}, fslow/2^3, fslow/2^4

- A/D converter

  10 bits × 12 channels

- Serial Interface: 4 systems

  <Serial Interface 0> (Full duplex UART/ Clock synchronous serial interface)

  Clock synchronous serial interface

  Transfer clock source:

  fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4, Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock

  MSB/LSB can be selected as the first bit to be transferred, arbitrary size of 1 to 8 bits is selectable.

  Continuous transmission, continuous reception, continuous transmission/reception are available.

  Full duplex UART

  Baud rate timer: selected from Timer 0 to 4, or Timer A

  Parity check, overrun error/framing error are detected

  Transfer bits of 7 to 8 are selectable

  <Serial Interface 1> (Full duplex UART/ Clock synchronous serial interface)

  Clock synchronous serial interface

  Transfer clock source:

  fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4, Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, external clock

  MSB/LSB can be selected as the first bit to be transferred, arbitrary size of 1 to 8 bits are selectable.

  Continuous transmission, continuous reception, continuous transmission/reception are available.

  Full duplex UART

  Baud rate timer: selected from Timer 0 to 4, or Timer A

  Parity check, overrun error/framing error are detected

  Transfer bits of 7 to 8 are selectable

  <Serial Interface 2> (Full duplex UART / Clock synchronous serial interface)

  Clock synchronous serial interface

  Transfer clock source:

  fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4, Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock

  MSB/LSB can be selected as the first bit to be transferred, arbitrary size of 1 to 8 bits are selectable.

  Continuous transmission, continuous reception, continuous transmission/reception are available.

  Full duplex UART

  Baud rate timer: selected from Timer 0 to 4, or Timer A

  Parity check, overrun error/framing error are detected

  Transfer bits of 7 to 8 are selectable

  <Serial Interface 4> (Multi master IIC/ Clock synchronous serial interface)

  Clock synchronous serial interface

  Transfer clock source:

  fpll-div/2, fpll-div/4, fpll-div/8, fpll-div/32, fs/2, fs/4, Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock

  MSB/LSB can be selected as the first bit to be transferred, arbitrary size of 1 to 8 bits are selectable.

  Continuous transmission, continuous reception, continuous transmission/reception are available.

  Multi master IIC

  7-bit or 10-bit slave address can be set.

  General call communication mode is supported

- Auto reset circuit

■ Features (continued)

- Power supply voltage detection circuit

- LED driver: 7 sets

- LCD driver

  Segment output: Max. 28 pins (SEG0 to SEG27)

  Segment output pins can be switched to I/O ports in 1 bit. * At reset, SEG0 to SEG27 are input ports.

  Common output: 8 pins

  COM0 to COM7 can be switched to I/O ports in 1 bit. * COM4 to COM7 are dual ports with SEG0 to SEG3.

  Display mode selection

  Static

  1/2 duty, 1/2 bias

  1/3 duty, 1/3 bias

  1/4 duty, 1/3 bias

  1/8 duty, 1/3 bias

  LCD driver clock

  When the source clock is the main clock (fpll)

  $1/2^{18}$, $1/2^{17}$, $1/2^{16}$, $1/2^{15}$, $1/2^{14}$, $1/2^{13}$, $1/2^{12}$, $1/2^{11}$

  When the source clock is the sub clock (fslow)

  $1/2^{9}$, $1/2^{8}$, $1/2^{7}$, $1/2^{6}$

  Timer 0 to Timer 4

  LCD power supply

  LCD power supply is separated from V_{DD5} (can be used when $V_{LC1} \leq V_{DD5}$)

  External power supply voltage can be selected. (Supply voltage is supplied from V_{LC1}, V_{LC2}, and V_{LC3} pins)

  Internal dividing resistors

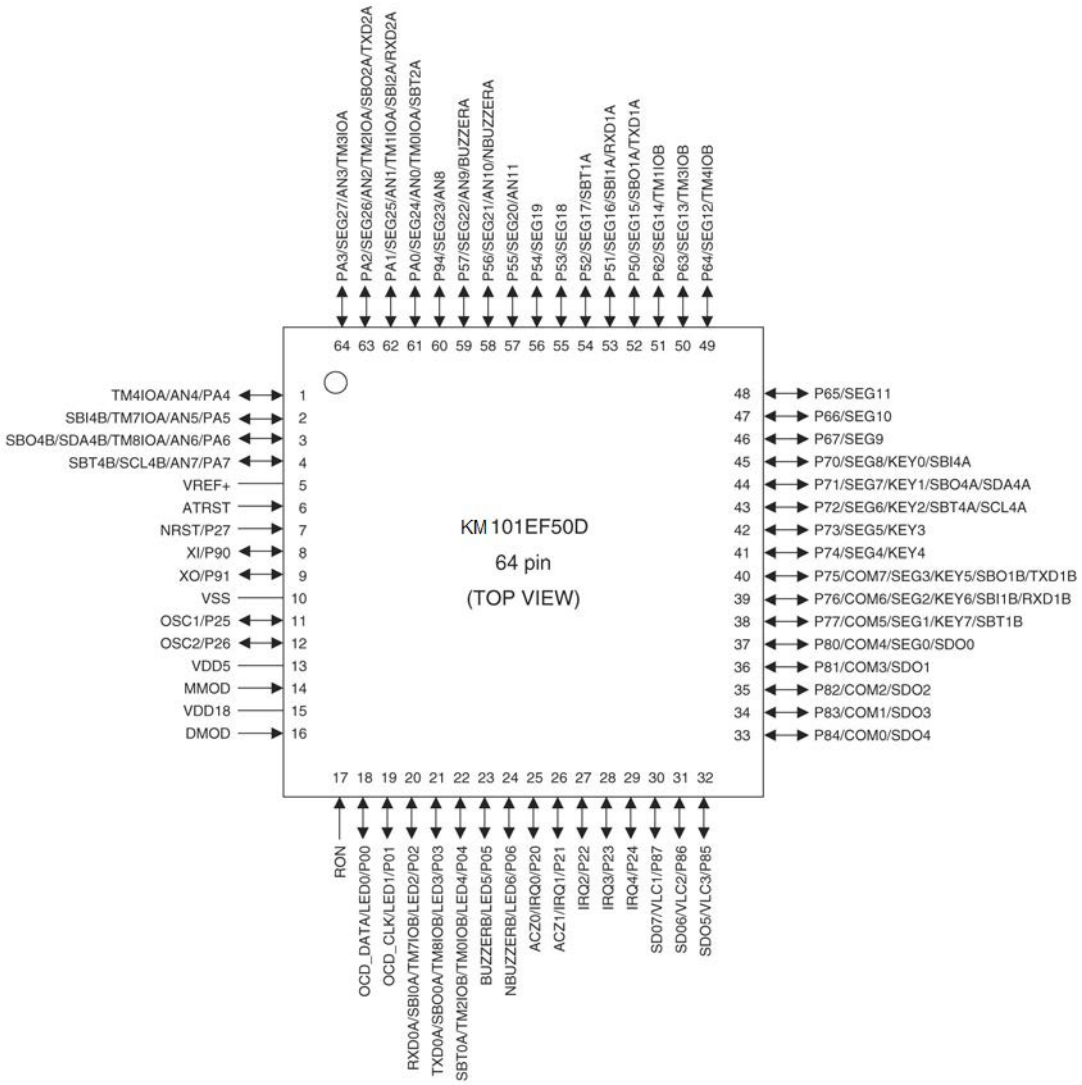
  External power supply voltage is divided the voltage input to V_{LC1} by internal resistors.

- Ports

I/O ports:	55 pins
LCD segment:	28 pins
LCD common:	8 pins
Serial interface communication:	18 pins
Timer I/O:	14 pins
Buzzer output:	4 pins
A/D input:	12 pins
External interrupt:	5 pins
LCD power supply pin:	3 pins
LED (large current output):	7 pins
High-speed oscillation:	2 pins
Low-speed oscillation:	2 pins
Special function:	9 pins
Operating mode control:	4 pins
Reset:	1 pin
Analog reference voltage:	1 pin
Power supply pins:	3 pins

■ Pin Description

- LQFP064-P-1414



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