NAU82028
3.1W Mono Filter-Free Class-D Audio Amplifier with 2 wire interface gain control

1 Description

The NAU82028 is a mono high efficiency filter-free Class-D audio amplifier, which is capable of driving a 4Ω load with up to 3.1W output power. This device provides chip enable pin with extremely low standby current and fast start-up time of 3.4ms. The NAU82028 features a highly flexible 2 wire interface with many useful gain settings. The gain can be selected from 12dB to –20.5dB (plus mute) by using 2 wire interface.

The NAU82028 is ideal for the portable applications of battery drive, as it has advanced features like 93% efficiency, ultra low quiescent current (i.e. 2.0 mA at 3.6V) and superior EMI performance. It has the ability to configure the inputs in either single-ended or differential mode.

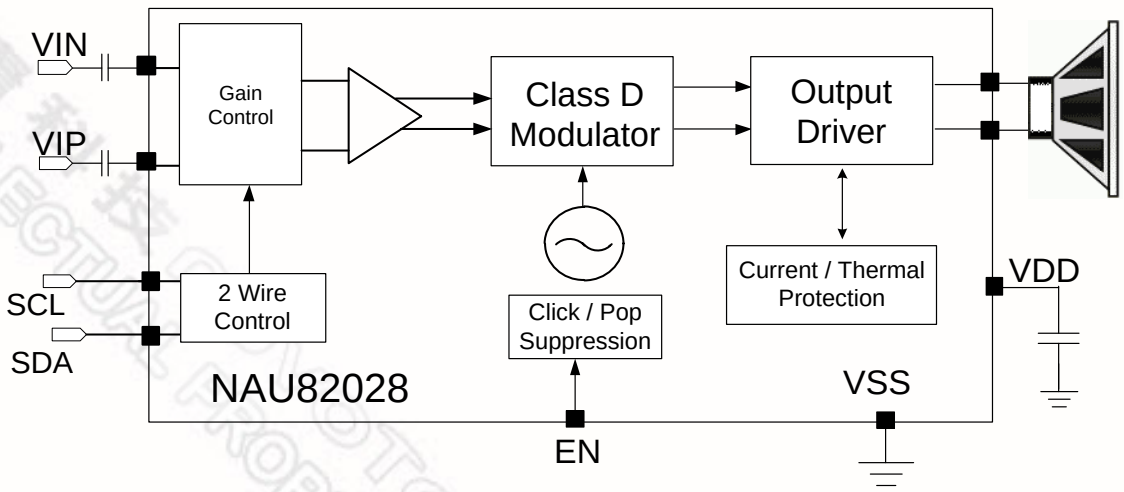
NAU82028 is available in Miniature WCSP-9 (1.56mm x 1.52mm in 0.5mm pitch) package.

Key Features

- Low Quiescent Current:
  - 2.0mA at 3.6V
  - 3.1mA at 5V
- Gain Setting with 2 wire interface
  - 12dB to -19.3dB (plus mute)
- Powerful Mono Class-D Amplifier:
  - 3.1W (4Ω @ 5V, 10% THD+N)
  - 2.46W (4Ω @ 5V, 1% THD+N)
  - 1.77W (8Ω @ 5V, 10% THD+N)
  - 1.41W (8Ω @ 5V, 1% THD+N)
  - 1.54 W (4Ω @ 3.6V, 10% THD+N)
  - 1.26 W (4Ω @ 3.6V, 1% THD+N)
  - 0.9 W (8Ω @ 3.6V, 10% THD+N)
  - 0.76 W (8Ω @ 3.6V, 1% THD+N)
- Low Output Noise: 26 μV_{RMS} (A –Weighted @3.6V)
- Low Current Shutdown Mode
- Click-and Pop Suppression
- 1.56mm x 1.52mm in WCSP (0.5mm Pitch)

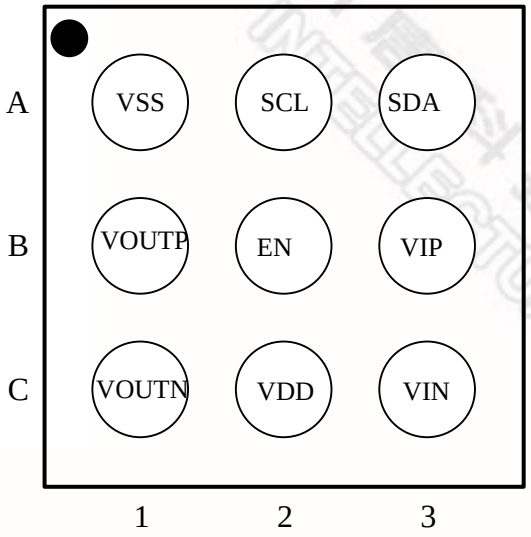
Applications

- Smartphones
- Tablet PCs
- Personal Navigation Devices



NAU82028 Block Diagram

2 Pin out



Part Number	Dimension	Package	Package Material
NAU82028VG	1.56mm x 1.52mm	9-bump WCSP (0.5mm pitch)	Green

3 Pin Descriptions

Pin #	Name	Type	Functionality
A1	VSS	Supply	High Current Ground
A2	SCL	Clock	I2C Clock
A3	SDA	Data	I2C Data
B1	VOUTP	Analog Output	Positive BTL Output
B2	EN	Digital Input	Chip Enable (High = Power Up; Low = Power Down)
B3	VIP	Analog Input	Positive Differential Input
C1	VOUTN	Analog Output	Negative BTL Output
C2	VDD	Supply	Power Supply
C3	VIN	Analog Input	Negative Differential Input

Table 1 NAU82028 Pin description

Operating Characteristics

Conditions: EN = VDD =3.6V, VSS = 0V, Av = 12dB, $Z_L = \infty$, Bandwidth = 20Hz to 22kHz, T_A = 25 °C; unless otherwise noted

Parameter	Symbol	Comments/Conditions		Min	Typ	Max	Units
Power Delivered							
Output Power	P_{out}	Z_L = 4Ω + 33μH THD + N = 10%	VDD = 5.0V		3.1		W
			VDD = 3.6V		1.54		
		Z_L = 4Ω + 33μH THD + N = 1%	VDD = 5.0V		2.46		
			VDD = 3.6V		1.26		
		Z_L = 8Ω + 68μH THD + N = 10%	VDD = 5.0V		1.77		
			VDD = 3.6V		0.90		
		Z_L = 8Ω + 68μH THD + N = 1%	VDD = 5.0V		1.41		
			VDD = 3.6V		0.76		

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Chip Enable (EN)						
Voltage Enable High	V_{EN_H}	VDD = 2.5V to 5.5V	1.3			V
Voltage Enable Low	V_{EN_L}	VDD = 2.5V to 5.5V			0.35	V
Input Leakage Current				0.1	2.0	μA
Thermal and Current Protection						
Thermal Shutdown Temperature				150		°C
Thermal Shutdown Hysteresis				20		°C
Limiting Current	I_{LIMIT}			2.0		A
Single Ended Input Resistance	R_{IN}	A_V = 12dB		75		kΩ

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Normal Operation						
Quiescent Current Consumption	I_{QUI}	VDD = 3.6V		2.0		mA
		VDD = 5V		3.1		mA
Shut Down Current	I_{OFF}	EN = 0		0.1		μA
Oscillator Frequency	f_{OSC}			300		kHz
Efficiency	η	WCSP (Z_L=8Ω)		93		%
Start Up Time	T_{start}			3.4		ms
Output Offset Voltage	V_{OS}			±1		mV
Common Mode Rejection Ratio	CMRR	f_{IN} = 217Hz		65		dB
Click-and-Pop Suppression		1Hz Shutdown (Z_L=8Ω)		83		dBV
Power Supply Rejection Ratio	PSRR	DC PSRR		100		dB
		AC PSRR V_{RIPPLE} = 0.2Vpp @217Hz		76		dB
		V_{RIPPLE} = 0.2Vpp@1kHz		63		dB
		V_{RIPPLE} = 0.2Vpp@10kHz		52		dB
Noise Performance		With A-weighted		26		μV_{RMS}
		Without A-weighted		36		μV_{RMS}

Absolute Maximum Ratings

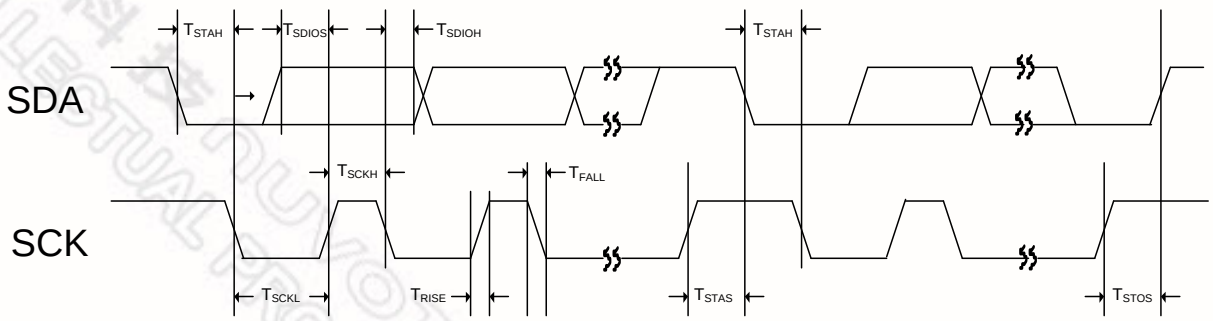
Parameter	Symbol	Condition	Min	Max	Units
DC Power Supply	VDD	VDD-VSS	-0.30	+6.00	V
Analog Input Voltage	AV_{IN}	V_{IN}-VSS	-0.3	VDD+0.3	V
Digital Input Voltage	DV_{IN}	DV_{IN}-VSS	-0.3	VDD+0.3	V
Minimum Load Resistance	R_L			3.2	Ω
Continuous Power Dissipation	P_O	WCSP, T=25°C		530	mW
Continuous Power Dissipation	P_O	WCSP, T=85°C		275	mW
Storage temperature range	Tst		-55	+150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty.

Recommended Operating Conditions

Parameter	Symbol	Condition	Min	Typical	Max	Units
DC Power Supply	VDD	VDD-VSS	2.50	5.00	5.50	V
High-level input voltage(EN pin)	V_{IH}		1.30			V
Low-level input voltage(EN pin)	V_{IL}				0.35	V
Operating Temperature	T_A		-40	+25	+85	°C

Digital Serial Interface Timing



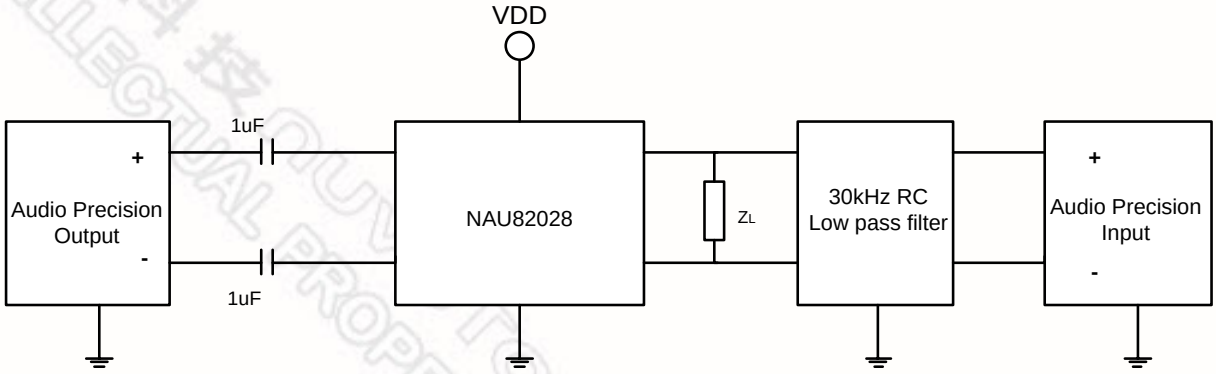
Two wire control mode timing

Symbol	Description	Min	Typ	Max	Unit
T_{STAH}	SDA falling edge to SCL falling edge hold timing in START / Repeat START condition	600	-	-	ns
T_{STAS}	SCL rising edge to SDA falling edge setup timing in Repeat START condition	600	-	-	ns
T_{STOS}	SCL rising edge to SDA rising edge setup timing in STOP condition	600	-	-	ns
T_{SCLH}	SCL High Pulse Width	600	-	-	ns
T_{SCLL}	SCL Low Pulse Width	1,300	-	-	ns
T_{RISE}	Rise Time for all 2-wire Mode Signals	-	-	300	ns
T_{FALL}	Fall Time for all 2-wire Mode Signals	-	-	300	ns
T_{SDAS}	SDA to SCL Rising Edge DATA Setup Time	100	-	-	ns
T_{SDAH}	SCL falling Edge to SDA DATA Hold Time	0	-	600	ns

Digital Serial Interface Electrical Characteristics

Condition	Min	Typ.	Max.	Unit	Test Conditions
Input Leakage Current SCL, SDA	-1	-	+1	µA	VDD = 5.5V
Input High Voltage VIH	0.7 VDD		5.5	V	
Input low Voltage VIL	VSS		0.3 VDD	V	
VOH (SCL, SDA)	0.9 VDD			V	
VOL (SCL, SDA)			0.2 VDD	V	IOL = 1 mA
SDA, SCL; pull up resistor value		50k		Ohm	

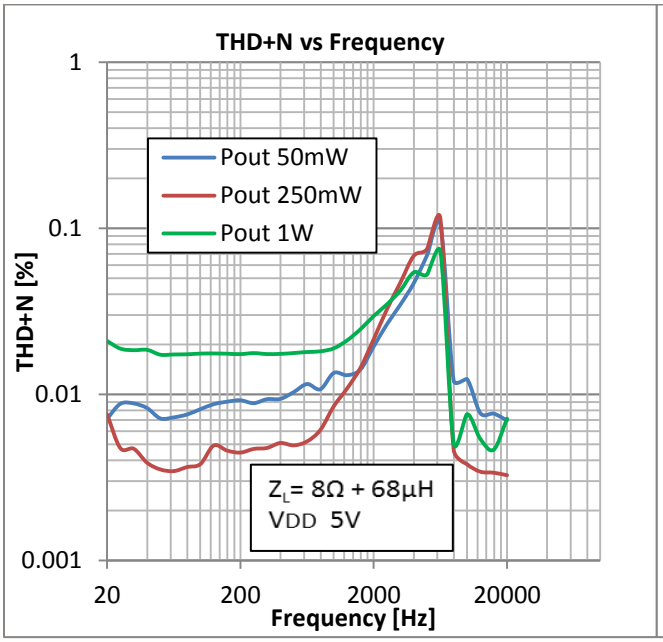
The following setup is used to measure the above parameters

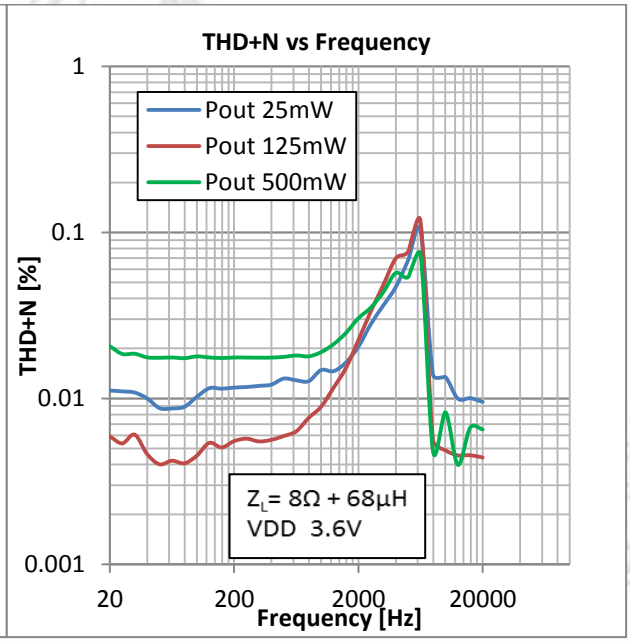


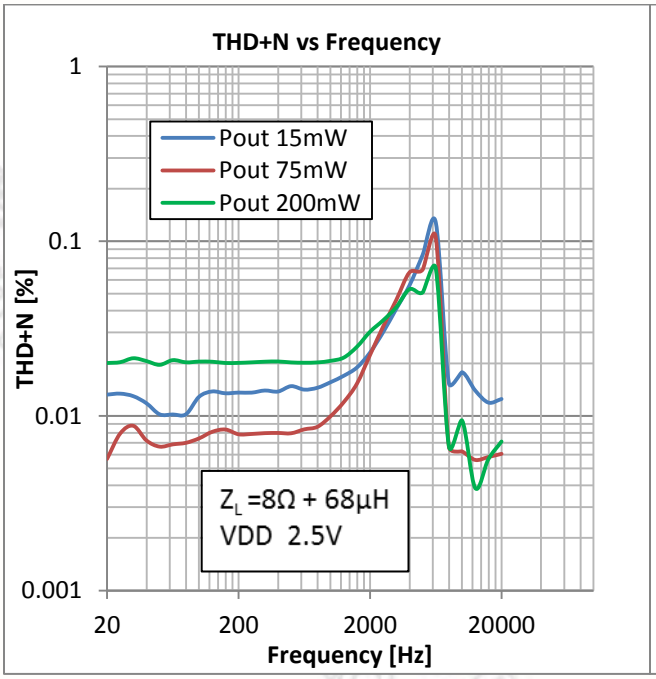
The low pass filter is implemented by using R= 1kΩ and C= 4.7nF.

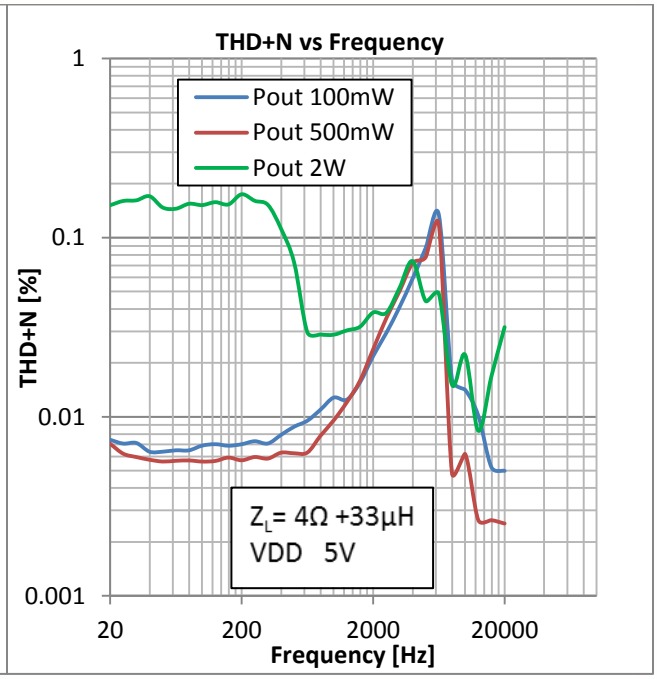
4 Typical Operating Characteristics

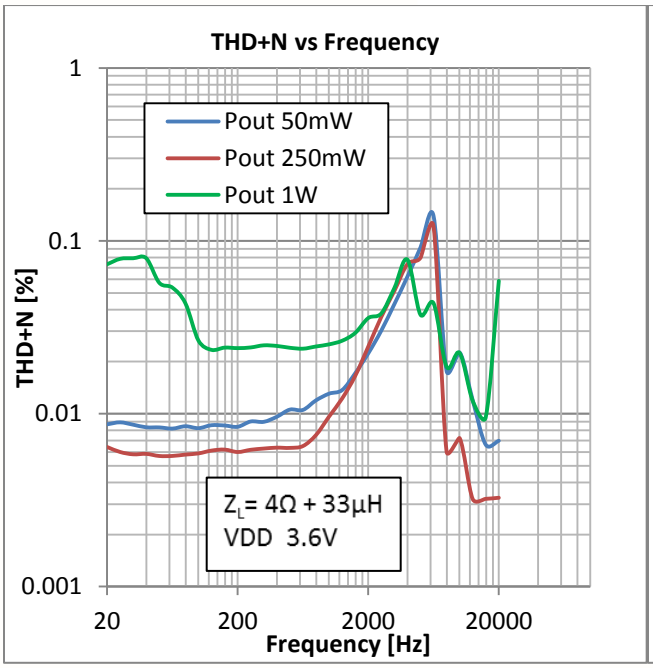
Conditions: EN = V_{DD} = 3.6V, VSS = 0V, Av = 12dB, Bandwidth = 20Hz to 22 kHz, T_A = 25 °C, unless otherwise noted

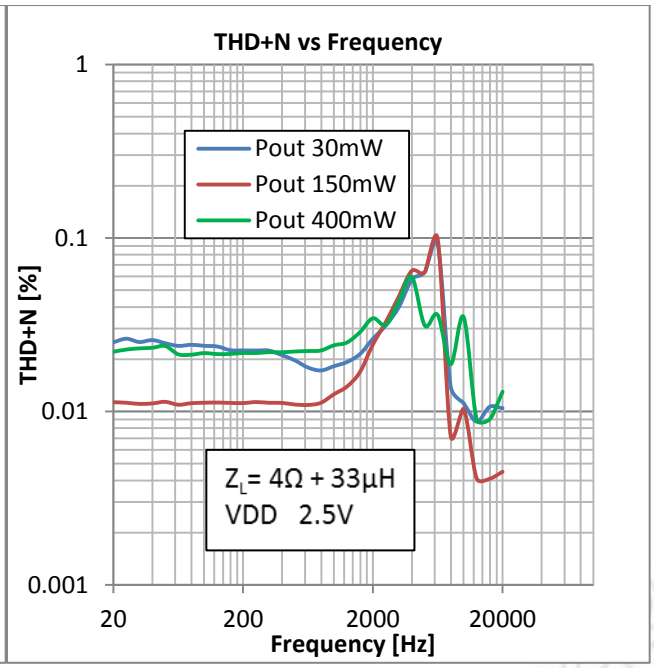


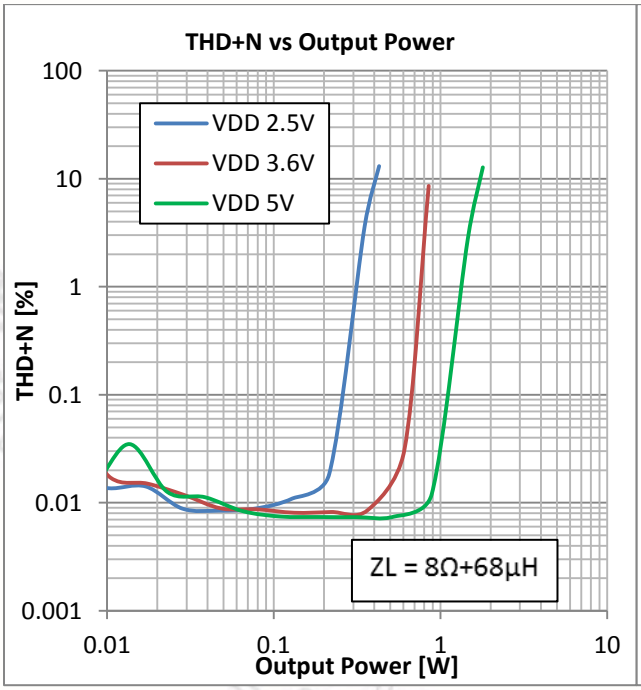


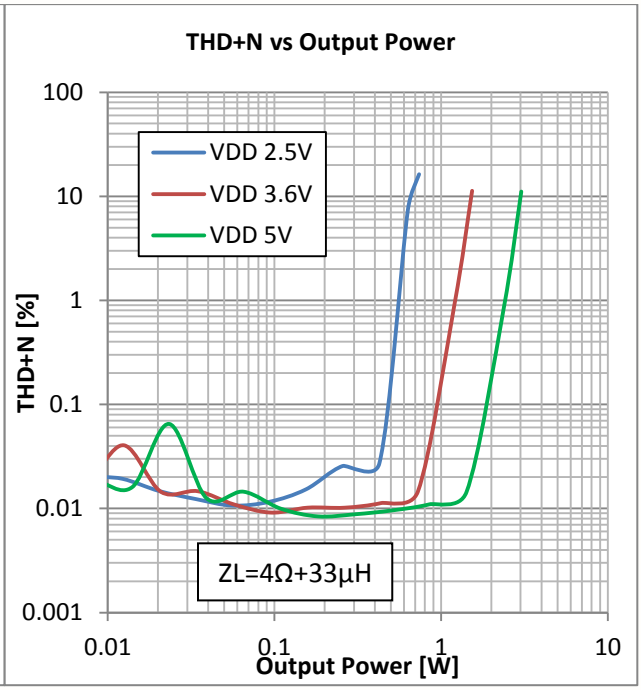


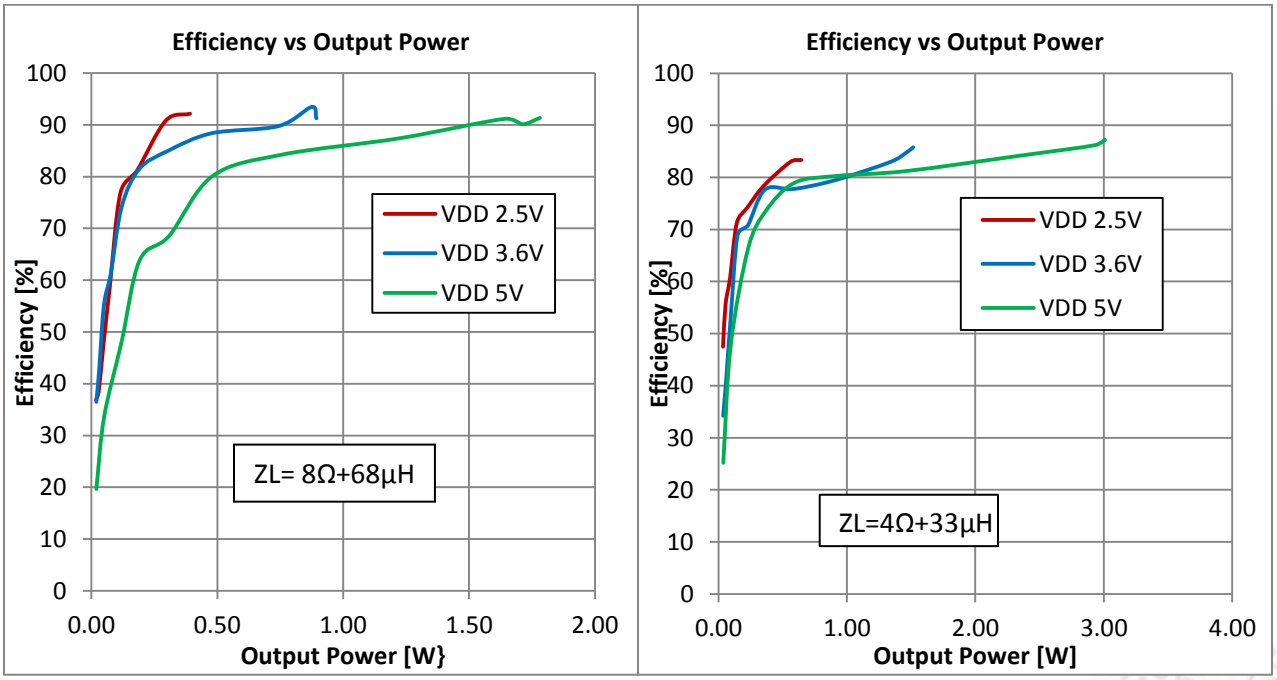


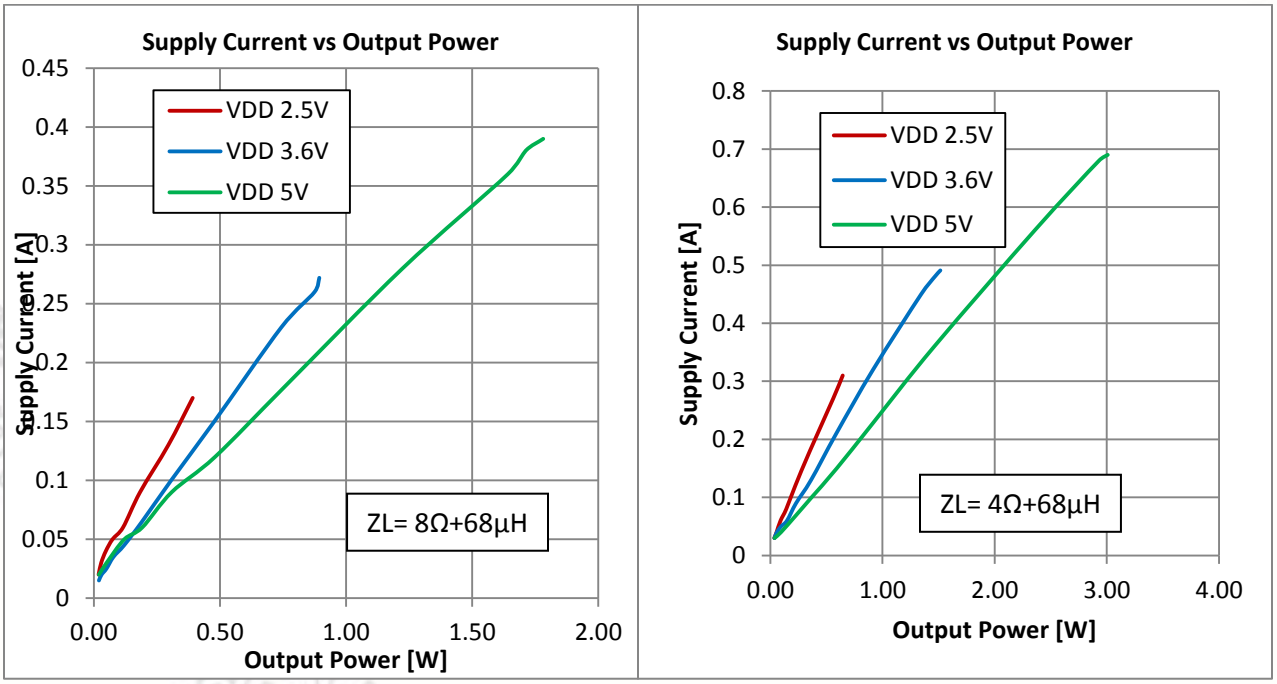

THD+N vs Frequency
Pout 50mW
Pout 250mW
Pout 1W
Z_L= 4Ω + 33µH
VDD 3.6V
THD+N [%]
Frequency [Hz]
1
0.1
0.01
0.001
20
200
2000
20000

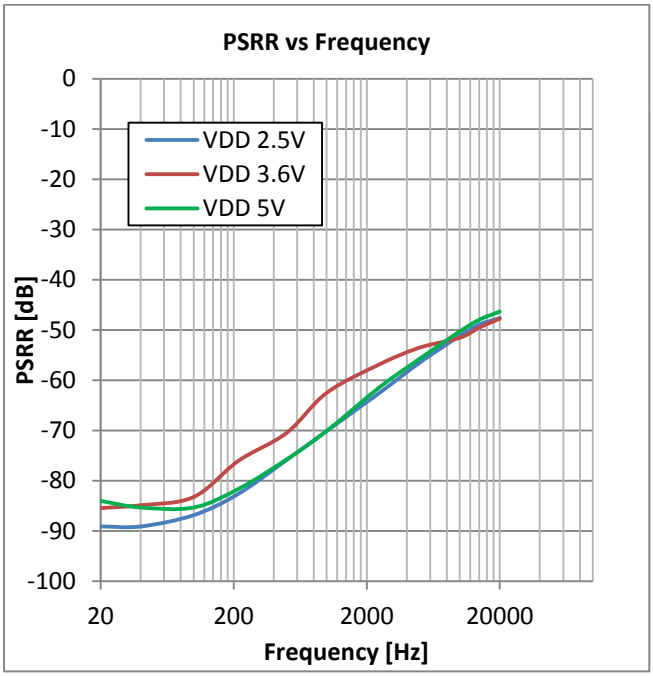

THD+N vs Frequency
Pout 30mW
Pout 150mW
Pout 400mW
Z_L= 4Ω + 33µH
VDD 2.5V
THD+N [%]
Frequency [Hz]
1
0.1
0.01
0.001
20
200
2000
20000


THD+N vs Output Power
VDD 2.5V
VDD 3.6V
VDD 5V
ZL = 8Ω+68µH
THD+N [%]
Output Power [W]
100
10
1
0.1
0.01
0.001
0.01
0.1
1
10


THD+N vs Output Power
VDD 2.5V
VDD 3.6V
VDD 5V
ZL=4Ω+33µH
THD+N [%]
Output Power [W]
100
10
1
0.1
0.01
0.001
0.01
0.1
1
10


Efficiency vs Output Power
Efficiency [%]
Output Power [W}
VDD 2.5V
VDD 3.6V
VDD 5V
ZL= 8Ω+68μH
Efficiency vs Output Power
Efficiency [%]
Output Power [W]
VDD 2.5V
VDD 3.6V
VDD 5V
ZL=4Ω+33μH


Supply Current vs Output Power
Supply Current [A]
Output Power [W]
VDD 2.5V
VDD 3.6V
VDD 5V
ZL= 8Ω+68μH
Supply Current vs Output Power
Supply Current [A]
Output Power [W]
VDD 2.5V
VDD 3.6V
VDD 5V
ZL= 4Ω+68μH



5 Special Feature Description

The NAU82028 offers excellent quantity performance as high efficiency, high output power and low quiescent current. It also provides the following special features.

5.1 Gain Setting with 2 wire interface control

The NAU82028 provides programmable volume control by using the VLCCTRL register . The possible gain values are listed in the table below:

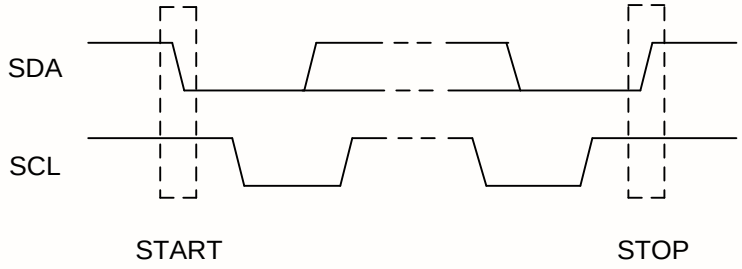
VLCRTL[5:0] Reg 0x1B	GAIN
0x0	12 dB
0x1	10.4 dB
0x2	8.8 dB
0x3	7.1dB
0x4	5.4 dB
0x5	3.6 dB
0x6	1.7 dB
0x7	-0.2 dB
0x8	-2.0 dB
0x9	-3.9 dB
0xA	-5.8 dB
0xB	-7.8 dB
0xC	-9.7 dB
0xD	-11.7 dB
0xE	-13.6 dB
0xF	-15.6 dB
0x10	-17.6 dB
0x11	-19.3 dB
0x12	-20.4 dB
0x13	-20.5 dB
0x14	-20.2 dB
0x15	-20.0 dB
0x16	-19.8 dB
0x17	-19.7 dB
0x18	-19.6 dB
0x19	-19.5 dB
0x1A	-19.5 dB
0x1B	-19.4 dB
0x1C	-19.4 dB
0x1D	-19.4 dB
0x1E	-19.4 dB
0x1F	-19.3 dB
0x3F	Mute

5.1.1 2-Wire-Serial Control and Data Bus (I^2C Style Interface)

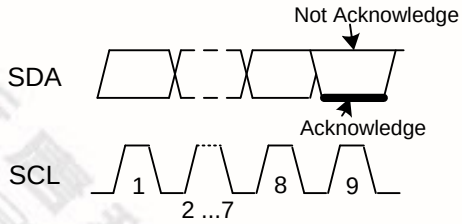
The serial interface provides a 2-wire bidirectional read/write data interface similar to and typically compatible with standard I2C protocol. This protocol defines any device that sends CLK onto the bus as a master, and the receiving device as slave. The NAU82028 can function only as a slave device.
An external clock drives the device, and in accordance with the protocol, data is sent to or from the device accordingly. All functions are controlled by means of a register control interface in the device.

5.1.2 2-Wire Protocol Convention

All 2-Wire interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDA while SCL is HIGH. All 2-Wire interface operations are terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH. A STOP condition at the end of a read or write operation places the serial interface in standby mode.
An acknowledge (ACK), is a software convention is used to indicate a successful data transfer. The transmitting device releases the SDA bus after transmitting eight bits to allow for the ACK response. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data.
Following a START condition, the master must output a device address byte. This consists of a 7-bit device address, and the LSB of the device address byte is the R/W (Read/Write) control bit. When R/W= 1, this indicates the master is initiating a read operation from the slave device, and when R/W=0, the master is initiating a write operation to the slave device. If the device address matches the address of the slave device, the slave will output an ACK during the period when the master allows for the ACK signal.



START and STOP signals



Acknowledge and NOT Acknowledge

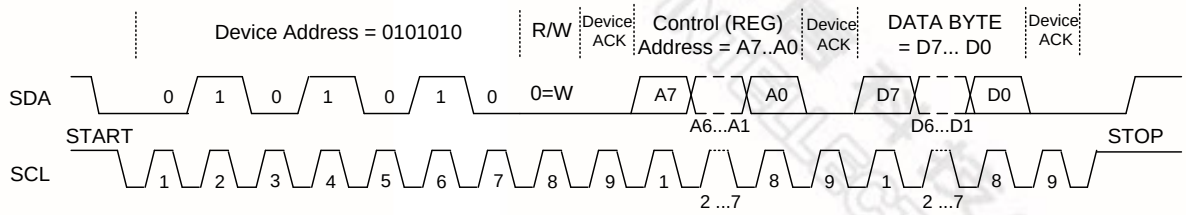
0	1	0	1	0	1	0	R/W	Device Address Byte
A7	A6	A5	A4	A3	A2	A1	A0	Control Address Byte
D7	D6	D5	D4	D3	D2	D1	D0	Data Byte

Slave Address Byte, Control Address Byte, and Data Byte

5.1.3 2-Wire Write Operation

A Write operation consists of a two-byte instruction followed by a Data Byte. A Write operation requires a START condition, followed by a valid device address byte with R/W= 0, a valid control address byte, data byte, and a STOP condition.

The NAU82028 is permanently programmed with "010 1010" (0x2A) as the Device Address. If the Device Address matches this value, the NAU82028 will respond with the expected ACK signaling as it accepts the data being transmitted into it.



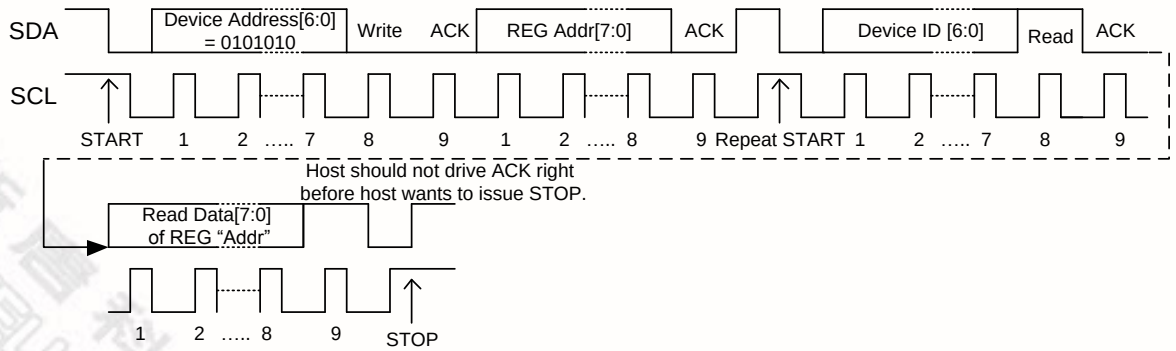
Write Sequence

5.1.4 2-Wire Single Read Operation

A Read operation consists of a three-byte Write instruction followed by a Read instruction of data byte. The bus master initiates the operation issuing the following sequence: a START condition, device address byte with the R/W bit set to "0", and a Control Register Address byte. This indicates to the slave device which of its control registers is to be accessed.

The NAU82028 is permanently programmed with "010 1010" (0x2A) as its device address. If the device address matches this value, the NAU82028 will respond with the expected ACK signaling as it accepts the Control Register Address being transmitted into it. After this, the master transmits a second START condition, and a second instantiation of the same device address, but now with R/W=1.

After again recognizing its device address, the NAU82028 transmits an ACK, followed by a one byte value containing the data from the selected control register inside the NAU82028. During this phase, the master generates the ACK signaling with byte transferred from the NAU82028.



Read Sequence

5.1.5 2-Wire Timing

The NAU82028 is compatible with serial clock speeds defined as "standard mode" with SCL 0 - 100 kHz, and "fast mode" with SCL 0 - 400 kHz. At these speeds, the total bus line capacitance load is required to be 400 pF or less. Open collector drivers are required for the serial interface. Therefore, the bus line rise time is determined by the total serial bus capacitance and the VDD pull-up resistors. The NAU82028 defaults to a weak pull up (typical 50 k ohm) for applications with no external pull up resistor.

5.2 Register Map

The NAU82028 contains the registers as shown in the table below.

Addr (Hex)	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default (Hex)	Note
1B			VOL CTRL[5]	VOL CTRL[4]	VOL CTRL[3]	VOL CTRL[2]	VOL CTRL[1]	VOL CTRL[0]	00	RW

5.3 Register Map Details

0x1B: VOLCTRL[5:0]

This register can be used to adjust the output volume.

Bit	Default	Function when set to '1'
VOLCTRL[5]	0	Adjust Output Volume
VOLCTRL[4]	0	Adjust Output Volume
VOLCTRL[3]	0	Adjust Output Volume
VOLCTRL[2]	0	Adjust Output Volume
VOLCTRL[1]	0	Adjust Output Volume
VOLCTRL[0]	0	Adjust Output Volume

5.4 Device Protection

The NAU82028 includes device protection for three operating scenarios. They are

1. Thermal Overload
2. Short circuit
3. Supply under voltage

5.4.1 Thermal Overload Protection

When the device internal junction temperature reaches 150°C, the NAU82028 will disable the output drivers. When the device cools down and a safe operating temperature of 130°C has been reached for at least about 100ms, the output drivers will be enabled again.

5.4.2 Short Circuit Protection

If a short circuit is detected on any of the pull-up or pull-down devices on the output drivers for at least 16.7µs, the output drivers will be disabled for 100ms. The output drivers will then be enabled again and check for the short circuit. If the short circuit is still present, the output drivers are disabled after 16.7µs. This cycle will continue until the short circuit is removed. The short circuit threshold is 2.0A at 3.6V.

5.4.3 Supply under Voltage Protection

If the supply voltage drops under 2.1V, the output drivers will be disabled while the NAU82028 control circuitry still operates. This will avoid the battery supply to drag down too low before the host processor can safely shut down the devices on the system. If the supply drops further below 1.6 V the internal power on reset is activated and puts the entire device in power down state.

5.5 Power up and Power down Control

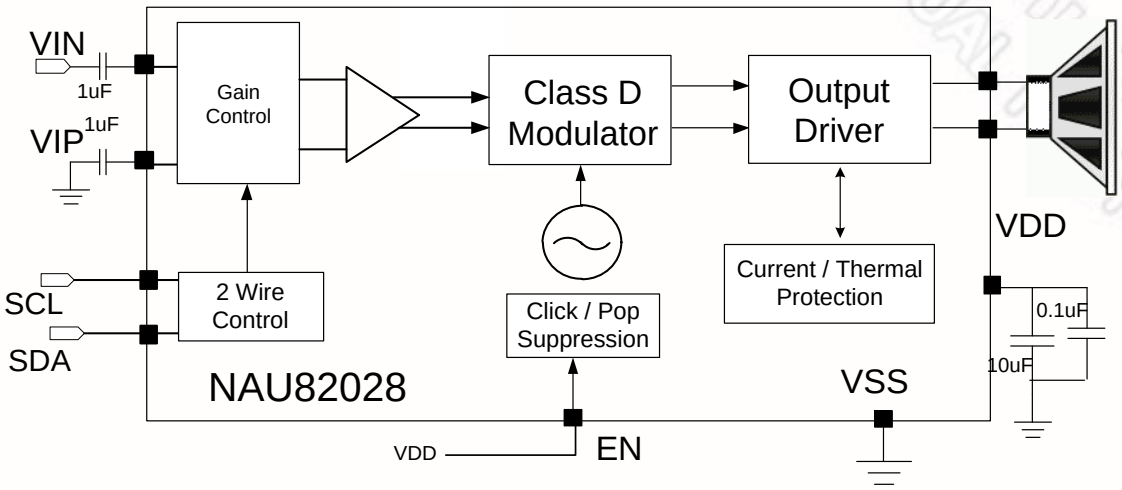
When the supply voltage ramps up, the internal power on reset circuit gets triggered. At this time all internal circuits will be set to power down state. The device can be enabled by setting the EN pin high. Upon setting the EN pin high, the device will go through an internal power up sequence in order to minimize 'pops' on the speaker output. The complete power up sequence will take about 4ms. The device will power down in about 30µs, when the EN pin is set low.

It is important to keep the input signal at zero amplitude in order to minimize the 'pops' when the EN pin is toggled.

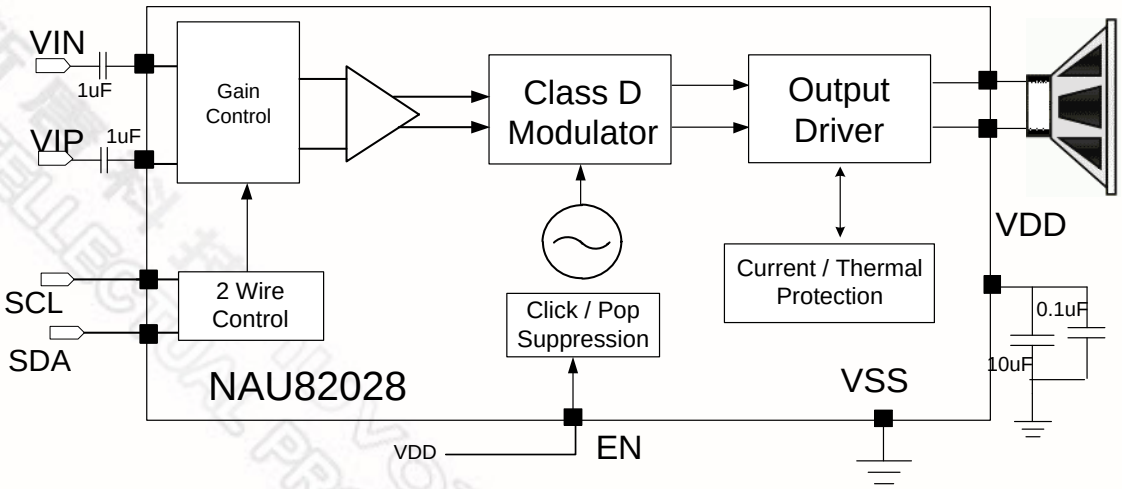
6 Application Information

6.1 Application diagram

6.1.1 Single ended input configuration



6.1.2 Differential input configuration

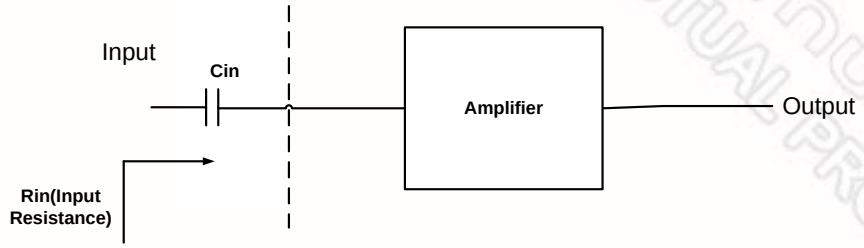


6.2 Component selection

6.2.1 Coupling Capacitors

An ac coupling capacitor (C_{in}) is used to block the dc content from the input source. The input resistance of the amplifier (R_{in}) together with the C_{in} will act as a high pass filter. So depending on the required cut off frequency the C_{in} can be calculated by using the following formula

$$C_{in} = \frac{1}{2\pi R_{in} f_c}$$ Where f_c is the desired cut off frequency of the High pass filter.



6.2.2 Bypass Capacitors

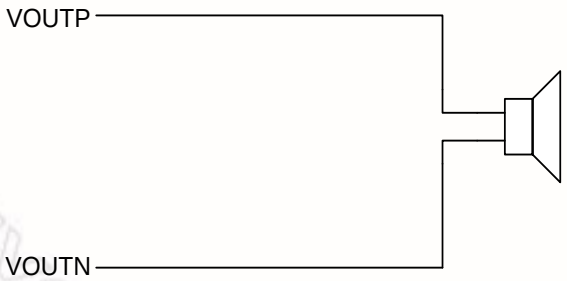
Bypass capacitors are required to remove the ac ripple on the VDD pins. The value of these capacitors depends on the length of the VDD trace. In most cases, 10µF and 0.1µF are enough to get the good performance.

6.3 Layout considerations

Good PCB layout and grounding techniques are essential to get the good audio performance. It is better to use low resistance traces as these devices are driving low impedance loads. The resistance of the traces has a significant effect on the output power delivered to the load. In order to dissipate more heat, use wide traces for the power and ground lines.

6.4 Class D without filter

The NAU82028 is designed for use without any filter on the output line. That means the outputs can be directly connected to the speaker in the simplest configuration. This type of filter less design is suitable for portable applications where the speaker is very close to the amplifier. In other words, this is preferable in applications where the length of the traces between the speaker and amplifier is short. The following diagram shows this simple configuration.



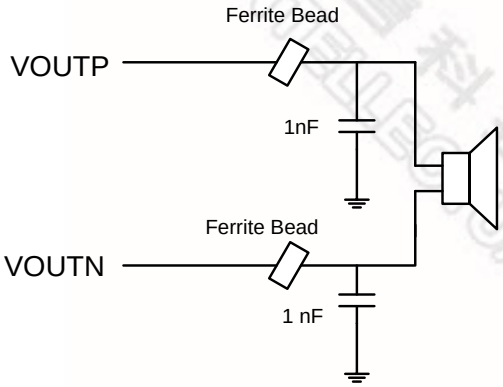
NAU82028 outputs connected to speaker without filter circuit

6.5 Class D with filter

In some applications, short trace lengths are not possible because of speaker size limitations and other layout reasons. In these applications, the long traces will cause EMI issues. There are two types of filter circuits available to reduce the EMI effects. These are ferrite bead and LC filters.

6.5.1 Ferrite Bead filter

The ferrite bead filters are used to reduce the high frequency emissions. The typical circuit diagram is shown in the figure.

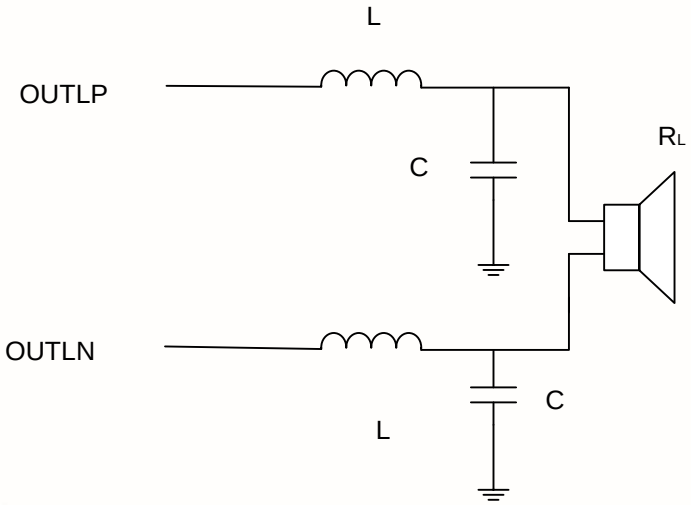


NAU82028 outputs connected to speaker with Ferrite Bead filter

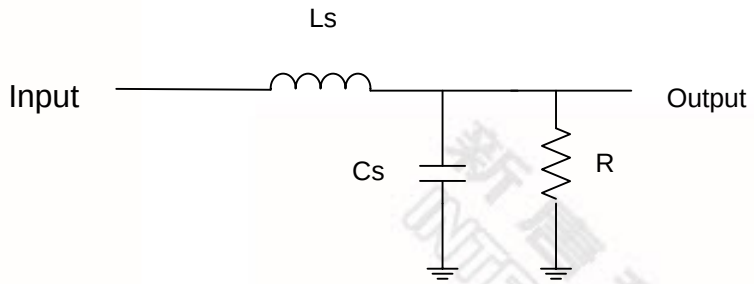
The characteristic of ferrite bead is such that it offers higher impedance at high frequencies. For better EMI performance select ferrite bead which offers highest impedance at high frequencies, so that it will attenuate the signals at higher frequencies. Usually the ferrite beads have low impedance in the audio range, so it will act as a pass through filter in the audio frequency range.

6.5.2 LC filter

The LC filter is used to suppress the low frequency emissions. The following diagram shows the NAU82028 outputs connected to the speaker with LC filter circuit. R_L is the resistance of the speaker coil.



NAU82028 outputs connected to speaker with LC filter



Standard Low pass LCR filter

The following are the equations for the critically damped (ζ = 0.707) standard low pass LCR filter

$$2\pi f_c = \frac{1}{\sqrt{LC}} \quad f_c \text{ is the cutoff frequency}$$

$$= 0.707 = \frac{1}{2R} * \sqrt{\frac{L}{C}}$$

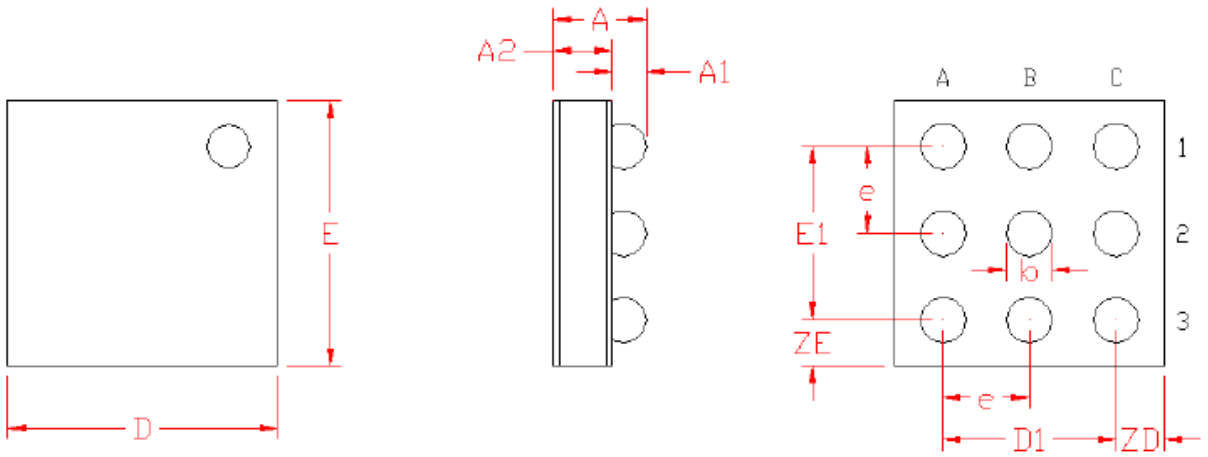
The L and C values for differential configuration can be calculated by duplicating the single ended configuration values and substituting $R_L = 2R$.

6.6 NAU82028 EMI performance

The NAU82028 includes a spread spectrum oscillator for reduced EMI. The PWM oscillator frequency typically sweeps in a range of 300 kHz +/- 15 kHz in order to spread the energy of the PWM pulses over a larger frequency band. In addition, slew rate control on the output drivers allows the application of 'filter less' loads, while suppressing EMI at high frequencies.

7 Package Dimensions

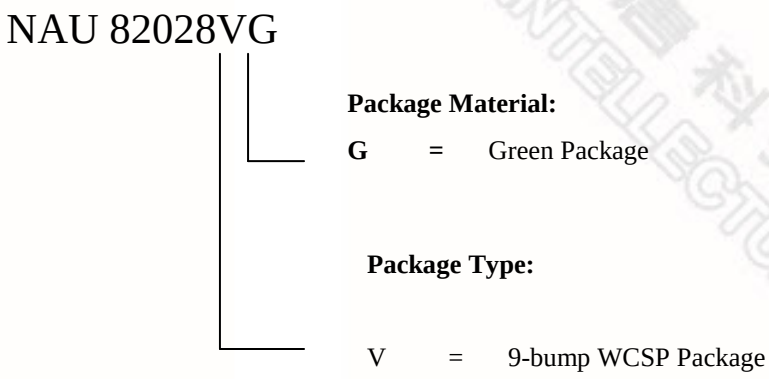
7.1 9 bump WCSP (0.5mm pitch)(1.56mm x1.52mm)



SYMBOL	DIMENSION(mm)		
	MIN	NOM	MAX
A	0.490	0.540	0.590
A1	0.175	0.200	0.225
A2	0.300	0.340	0.380
b	0.238	0.265	0.292
D	1.520	1.560	1.600
E	1.485	1.525	1.565
D1	1.000		
E1	1.000		
ZD	0.280		
ZE	0.2625		
e	0.500		
Solder ball Diameter	0.250		

8 Ordering Information

Nuvoton Part Number Description



Version History

VERSION	DATE	PAGE	DESCRIPTION
Rev0.1	Dec, 2012	NA	Preliminary Version
Rev0.2	Mar, 2013	1,3,4,6-10,13	1. Operating characteristics modified 2. Typical operating characteristics plots modified 3. Gain setting with 2 wire interface table modified for NAU82028

Table 2 Version History

Important Notice

Nuvoton products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Furthermore, Nuvoton products are not intended for applications wherein failure of Nuvoton products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Nuvoton customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nuvoton for any damages resulting from such improper use or sales.