NuMicro® Family

Arm® 32-bit Cortex®-M23 Microcontroller

NUC1262 Series
Datasheet

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1 GENERAL DESCRIPTION

The NuMicro® NUC1262 series 32-bit microcontroller is based on Arm® Cortex®-M23 core for Armv8-M architecture with LED Light Strip Interface (LLSI) and USB2.0 full-speed device using built-in 48 MHz oscillator to support the communication with PC and Mobile accessories. It runs up to 72 MHz and features 128 Kbytes of Flash, 20 Kbytes of SRAM, 2.5V ~ 5.5V wide operating voltage, and -40°C ~+105°C operating temperature.

The NUC1262 series has 10 channels of LED Light Strip Interface (LLSI) which is easy to control the LED light strip, up to 24 channels of high-speed PWM with clock frequency up to 72 MHz for precision control, up to 9 channels 50 mA high sink current pins that can drive high-brightness LEDs.

The NUC1262 series supports USB 2.0 full-speed device interfaces without external crystal oscillators, and USB commands can be used for light control. In addition, the NUC1262 series has a built-in 2 Kbytes of SPROM (Security Protection ROM), which provides an independent security encryption area to protect the intellectual property rights of developers. The NUC1262 series can be widely used in industrial control, lighting control, keyboard/mouse, and home appliances related applications.

The NUC1262 series is equipped with plenty of peripherals supporting up to 10 channels of LED Light Strip Interface (LLSI), up to 24 channels of 16-bit PWM, up to 9 channels of 50mA high sink current pins and USB 2.0 full-speed devices without external crystal oscillators. The NUC1262 series also equipped with Timers, Watchdog Timers, up to 10 channels of PDMA, 2 sets of UART, 2 sets of I²C, 2 sets of SPI/I²S, making it highly suitable for connecting comprehensive external modules. It also integrates high performance analog circuit, such as 8 channels of 12-bit 800 KSPS ADC, and supports high anti-interference capability 7 kV ESD (HBM)/ 4.4 kV EFT.

Supported packages include QFN48 (7 mm x 7 mm), LQFP48 (7 mm x 7 mm), and LQFP64 (7 mm x 7 mm), which are pin-compatible to other Nuvoton series to make the system design and parts change on functional enhancement easily.

Nuvoton NuMaker-NUC1262SE evaluation board and Nu-Link debugger are powerful tools for product evaluation and development. It supports IDEs provided by third parties, such as Keil® MDK, IAR EWARM and NuEclipse IDE with GNU GCC compiler.

1.1 Key Features and Application

Product Line	USB	UART	I²C	SPI/I²S	PWM	LED Lighting Strip Interface (LLSI)	PDMA	GPIO	ADC
NUC1262	2.0 FS Device	2	2	2	24	10	10	50	8

Table 1.1-1 Key Features Support Table

The NuMicro® NUC1262 series is suitable for a wide range of applications such as:

- Industrial Control
- Lighting Control
- Keyboard/Mouse
- Home Appliance
- Amusement Device
- Home Automation
- Security Alarm System
- Portable Data Collector

- USB to SPI Device
- PWM Control
- LED Control

2 FEATURES

Core and System	
Arm® Cortex®-M23 without TrustZone®	• Arm® Cortex®-M23 core, running up to 72 MHz when V_{DD} = 2.5V ~ 5.5V • Built-in Nested Vectored Interrupt Controller (NVIC) • 32-bit Single-cycle hardware multiplier and 32-bit 17-cycle hardware divider • 24-bit system tick timer • Supports Programmble and maskable interrupt • Supports Low Power Sleep mode by WFI and WFE instructions • Supports single cycle I/O access
Brown-out Detector (BOD)	• Four-level BOD with brown-out interrupt and reset option (4.4V/3.7V/2.7V/2.2V)
Low Voltage Reset (LVR)	• LVR with 2.0V threshold voltage level
Security	• 96-bit Unique ID (UID) • 128-bit Unique Customer ID (UCID)
Memories	
Flash	• Up to 128 KB application ROM (APROM) • Up to 4 KB Flash for user program loader (LDROM) • Up to 2 KB security protection ROM (SPROM) • 2 KB page erase for all embedded Flash • Supports CRC-32 checksum calculation function • Hardware external read protection of whole Flash memory by Security Lock Bit • Supports In-System-Programming (ISP), In-Application-Programming (IAP) update embedded Flash memory • Supports 2-wired ICP update through SWD/ICE interface
SRAM	• Up to 20 KB embedded SRAM • Supports byte-, half-word- and word-access • Supports PDMA mode
Cyclic Redundancy Calculation (CRC)	• Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32 • Programmable initial value • Supports programmable order reverse setting for input data and CRC checksum

	• Supports programmable 1's complement setting for input data and CRC checksum • Supports 8/16/32-bit of data width • Interrupt generated once checksum error occurs • Programmable seed value • 8-bit write mode: 1-AHB clock cycle operation • 16-bit write mode: 2-AHB clock cycle operation • 32-bit write mode: 4-AHB clock cycle operation • Supports using PDMA to write data to perform CRC operation
Peripheral DMA (PDMA)	• Supports up to 10 independent configurable channels for automatic data transfer between memories and peripherals • Channel 0, 1 supports time-out function • Basic and Scatter-Gather Transfer modes • Each channel supports circular buffer management using Scatter-Gather Transfer mode • Two types of priorities modes: Fixed-priority and Round-robin modes • Transfer data width of 8, 16, and 32 bits • Single and burst transfer type • Source and destination address can be increment or fixed • PDMA transfer count up to 65536 • Request source can be from software, SPI/I^2S, UART, I^2C, ADC, BPWM, LLSI and Timer
Clocks	
External Clock Source	• 4~24 MHz High-speed eXternal crystal oscillator (HXT) for precise timing operation • 32.768 kHz Low-speed eXternal crystal oscillator (LXT) for low-power system operation • Supports clock failure detection for external crystal oscillators and exception generatation (NMI)
Internal Clock Source	• 48 MHz High-speed Internal RC oscillator (HIRC) trimmed to 0.25% accuracy that can optionally be used as a system clock • 10 kHz Low-speed Internal RC oscillator (LIRC) for watchdog timer and wakeup operation • Up to 144 MHz on-chip PLL, sourced from HIRC or HXT, allows CPU operation up to the maximim CPU frequency without the need for a high-frequency crystal
Timers	
32-bit Timer	**TIMER** • Four sets of 32-bit timers, each timer having one 24-bit up

counter and one 8-bit prescale counter

- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Supports event counting function from external pin
- Supports event counting source from internal USB SOF signal
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter
- Supports internal capture triggered while internal ACMP output signal and LIRC transition
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Supports Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger PWM, ADC, PDMA function
- Supports Inter-Timer trigger mode

BPWM

- Supports maximum clock source frequency up to 72 MHz
- Supports up to four BPWM modules; each module provides 6 output channels
- Supports independent mode for BPWM output/Capture input channel
- Supports 12-bit pre-scalar from 1 to 4096
- Supports 16-bit resolution BPWM counter
- Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each BPWM pin
- Edge detect brake source to control brake state until brake interrupt cleared
- Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:
  - BPWM counter match zero, period value or compared value
- Supports trigger ADC on the following events:
  - BPWM counter match zero, period value or compared value
- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

Watchdog	• 18-bit free running up counter for WDT time-out interval • Selectable time-out interval (2^4 ~ 2^{20}) and the time-out interval is 416us ~ 27.3 s if WDT_CLK = 38.4 kHz (LIRC) • System kept in reset state for a period of (1 / WDT_CLK) * 63 • Able to wake up from Power-down or Idle mode • Interrupt or reset selectable on watchdog time-out • Supports selectable WDT reset delay period, including 1026, 130, 18 or 3 WDT_CLK reset delay period • Supports to force WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register • Supports WDT time-out wake-up function only if WDT clock source is selected as LIRC or LXT
Window Watchdog	• Clock sources from HCLK/2048 (default selection) or LIRC • Window set by 6-bit down counter with 11-bit prescale • WWDT counter suspends in Idle/Power-down mode • Supports Interrupt
Analog Interfaces	
Analog-to-Digital Converter (ADC)	• Analog input voltage range: 0 ~ AV_{DD} • 12-bit resolution and 10-bit accuracy is guaranteed • Up to 8 single-end analog input channels or 4 differential analog input channels • Maximum ADC peripheral clock frequency is 20 MHz • Up to 800 KSPS sampling rate • Configurable ADC internal sampling time • Four operation modes: – Single mode: A/D conversion is performed one time on a specified channel – Burst mode: A/D converter samples and converts the specified single channel and sequentially stores the result in FIFO – Single-cycle Scan mode: A/D conversion is performed only one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel – Continuous Scan mode: A/D converter continuously performs Single-cycle Scan mode until software stops A/D conversion • An A/D conversion can be started by: – Software Write 1 to ADST bit – External pin (STADC) – Timer 0~3 overflow pulse trigger – BPWM trigger • Each conversion result is held in data register of each

	channel with valid and overrun indicators • Conversion result can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting • 2 internal channels: band-gap voltage (VBG) and temperature sensor input • Supports PDMA transfer mode • Supports Calibration mode
Communication Interfaces	
UART	• Supports up to 2 UARTs: UART0, UART1 • UART baud rate clock from LXT(32.768 kHz) with 9600bps can work normally in Power-down mode even system clock is stopped (UART0/UART1 support) • Supports Single-wire function mode • Full-duplex asynchronous communications • Separates receive and transmit 16/16 bytes entry FIFO for data payloads (UART0/UART1 support) • Supports hardware auto-flow control (RX, TX, CTS and RTS) and programmable receiver buffer trigger level (UART0/UART1 support) • Supports programmable baud rate generator for each channel individually • Supports 8-bit receiver buffer time-out detection function (UART0/UART1 support) • Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART_TOUT [15:8]) (UART0/UART1 support) • Supports Auto-Baud Rate measurement and baud rate compensation function(UART0/UART1 support) • Supports break error, frame error, parity error and receive/transmit buffer overflow detection function • Fully programmable serial-interface characteristics • Programmable number of data bit, 5-, 6-, 7-, 8- bit character • Programmable parity bit, even, odd, no parity or stick parity bit generation and detection • Programmable stop bit, 1, 1.5, or 2 stop bit generation • Supports IrDA SIR function mode (UART0/UART1 support) • Supports for 3/16 bit duration for normal mode • Supports RS-485 mode (UART0/UART1 support) • Supports RS-485 9-bit mode • Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction • Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 • Address Match (AAD mode) wake-up function

	(UART0/UART1 support) • Supports PDMA mode
I²C	• Up to 2 sets of I²C devices • Master/Slave mode • Bidirectional data transfer between masters and slaves • Multi-master bus (no central master) • Supports 7-bit and 10-bit addressing mode • Standard mode (100 kbps) and Fast mode (400 kbps) and Fast mode plus (1 Mbps) • Arbitration between simultaneously transmitting masters without corruption of serial data on the bus • Serial clock synchronization allows devices with different bit rates to communicate via one serial bus • Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer • Supports 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows • Programmable clocks allow versatile rate control • Multiple address recognition (four slave addresses with mask option) • Supports setup/hold time programmable • Multi-address Power-down wake-up function • Supports PDMA transfer • Supports Bus Management (SM/PM compatible) function
SPI/I²S	• Supports one SPI/ I²S controller • Pin defined in SPI and I²S mode: **SPI** • Supports Master or Slave mode operation • Configurable bit length of a transfer word from 8 to 32-bit • Provides separate 4-level of 32-bit (or 8-level of 16-bit) depth transmit and receive FIFO buffers • Supports MSB first or LSB first transfer sequence • Supports Byte Reorder function • Byte or Word Suspend mode • Master and slave mode up to 24 MHz (when chip works at V_{DD} = 1.8 ~3.6V) • Supports one data channel half-duplex transfer • Support receive-only mode • SPI Supports PDMA transfer **I²S** • Supports Master or Slave mode operation • Capable of handling 8-, 16-, 24- and 32-bit word sizes in I²S

	mode • Provides separate 4-level depth transmit and receive FIFO buffers in I²S mode • Generates interrupt requests when buffer levels cross a programmable boundary • Supports monaural and stereo audio data in I²S mode • Supports PCM mode A, PCM mode B, I²S and MSB justified data format in I²S mode • Supports PDMA transfer
GPIO	• Four I/O modes: – Quasi-bidirectional mode – Push-Pull Output mode – Open-Drain Output mode – Input only with high impendence mode • High sink current (50mA) supports up to 9 I/O pins • Schmitt trigger input • I/O pin configured as interrupt source with edge/level trigger setting • I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode • Maximum I/O Speed is 24 MHz when V_{DD} = 2.5 ~ 5.5V • Supports up to 38/38/50 GPIOs for QFN48 and LQFP48/64 respectively • Enabling the pin interrupt function will also enable the wake-up function
Advanced Connectivity	
USB 2.0 Full Speed	• One set of USB 2.0 FS Device (12 Mbps) • On-chip USB Transceiver • Provides 1 interrupt source with 5 interrupt events • Supports Control, Bulk In/Out, Interrupt and Isochronous transfers • Auto suspend function when no bus signaling for 3 ms • Provides 8 programmable endpoints • Includes 512 Bytes internal SRAM as USB buffer • Provides remote wake-up capability • Supports Crystal-less function • Start of Frame (SOF) locked clock pulse generation

3 PARTS INFORMATION

3.1 NUC1262 Series Naming Rule

NUC	1262	S	E	4	A	E
Core	Line	Package	Flash	SRAM	Reserve	Temperature
Cortex®-M23	1262: USB	N: QFN48 (7x7 mm) L: LQFP48 (7x7 mm) S: LQFP64 (7x7 mm)	E: 128 KB	4: 20 KB		E:-40˚C ~ 105˚C

3.2 NUC1262 Selection Guide

Part Number	NUC1262NE4AE	NUC1262LE4AE	NUC1262SE4AE
Flash (KB)	128		
SRAM (KB)	20		
System Frequency (MHz)	72		
ISP ROM (KB)	4		
I/O	38	38	50
Timer	4		
PWM	24		
PDMA	10		
LLSI	8	8	10
High Sink 50 mA	9		
UART	2		
SPI /I^2S	2		
I^2C	2		
USB FS	1		
PLL (MHz)	144		
LXT	√		
12-bit ADC	8		
Package	QFN48	LQFP48	LQFP64

4 PIN CONFIGURATION

Users can find pin configuration information in the Multi-function Pin Diagram section or by using NuTool - PinConfig. The NuTool - PinConfig contains all Nuvoton NuMicro® Family chip series with all part number, and helps users configure GPIO multi-function correctly and handily.

4.1 Pin Configuration

4.1.1 Pin Diagram

4.1.1.1 *NuMicro® NUC1262 LQFP64 Pin Diagram*

Corresponding Part Number: NUC1262SE4AE

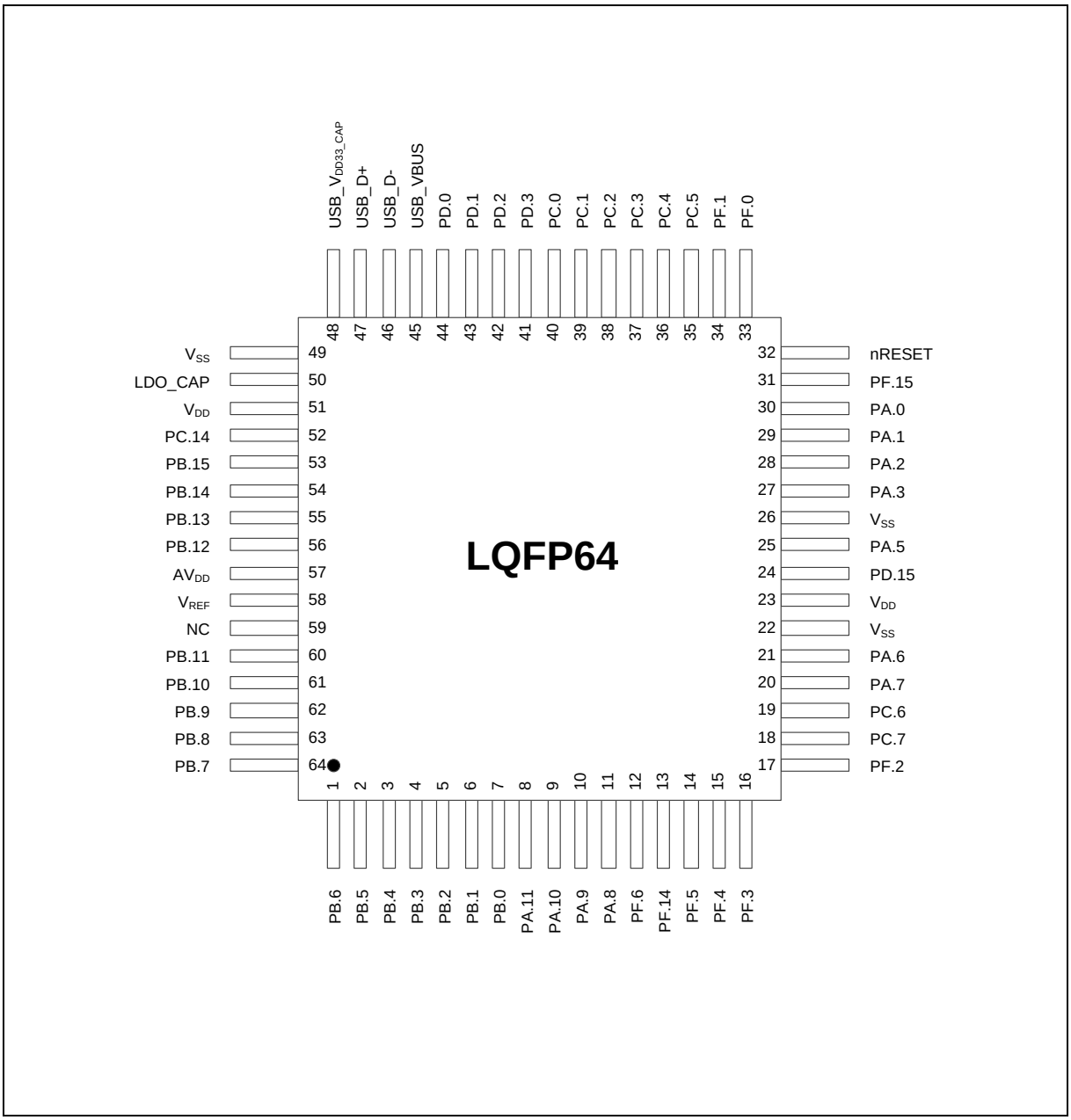


Figure 4.1-1 NuMicro® NUC1262 LQFP 64-pin Diagram

4.1.1.2 *NuMicro® NUC1262 LQFP48 Pin Diagram*

Corresponding Part Number: NUC1262LE4AE

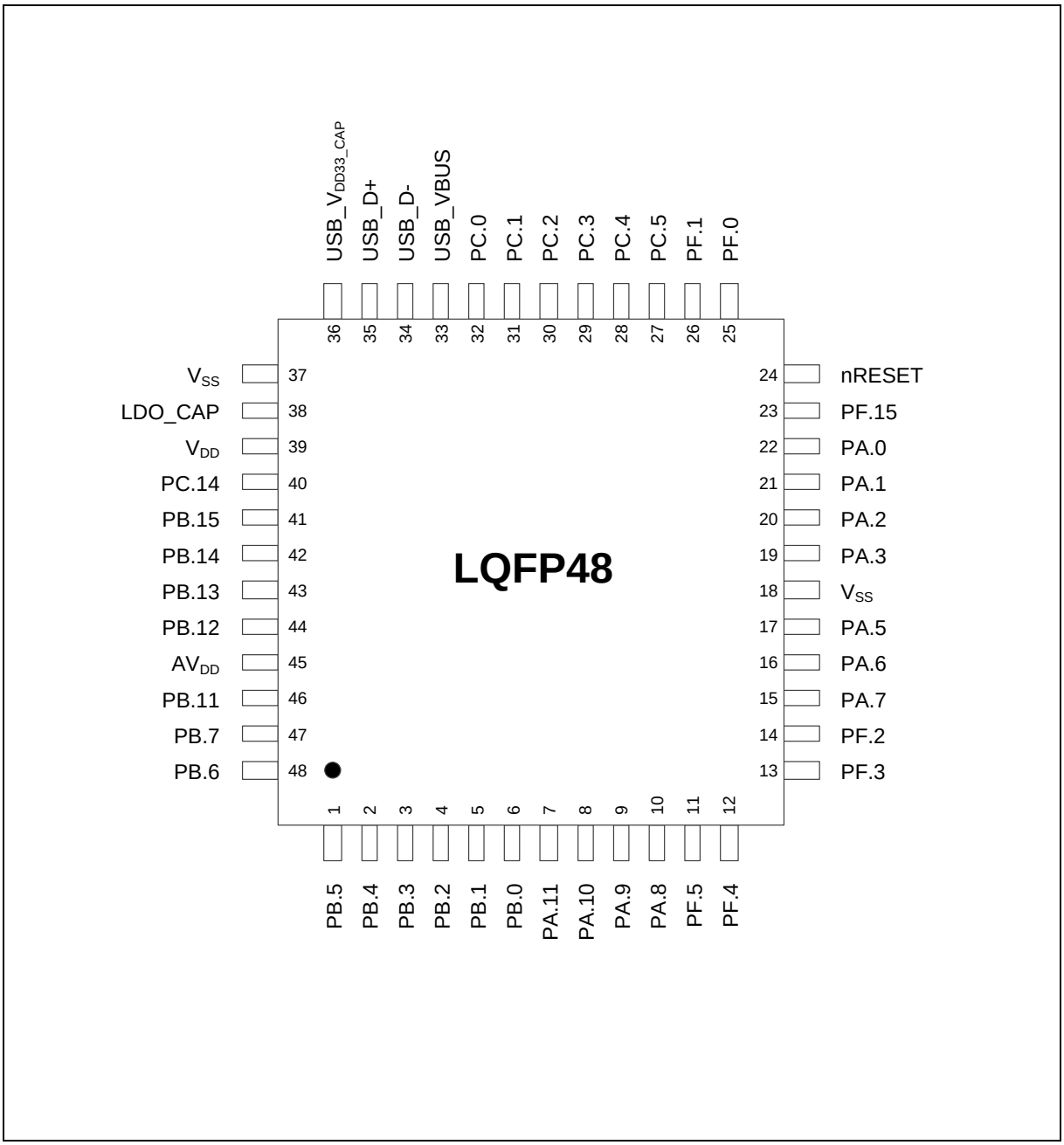


Figure 4.1-2 NuMicro® NUC1262 LQFP 48-pin Diagram

4.1.1.3 *NuMicro® NUC1262 QFN48 Pin Diagram*

Corresponding Part Number: NUC1262NE4AE

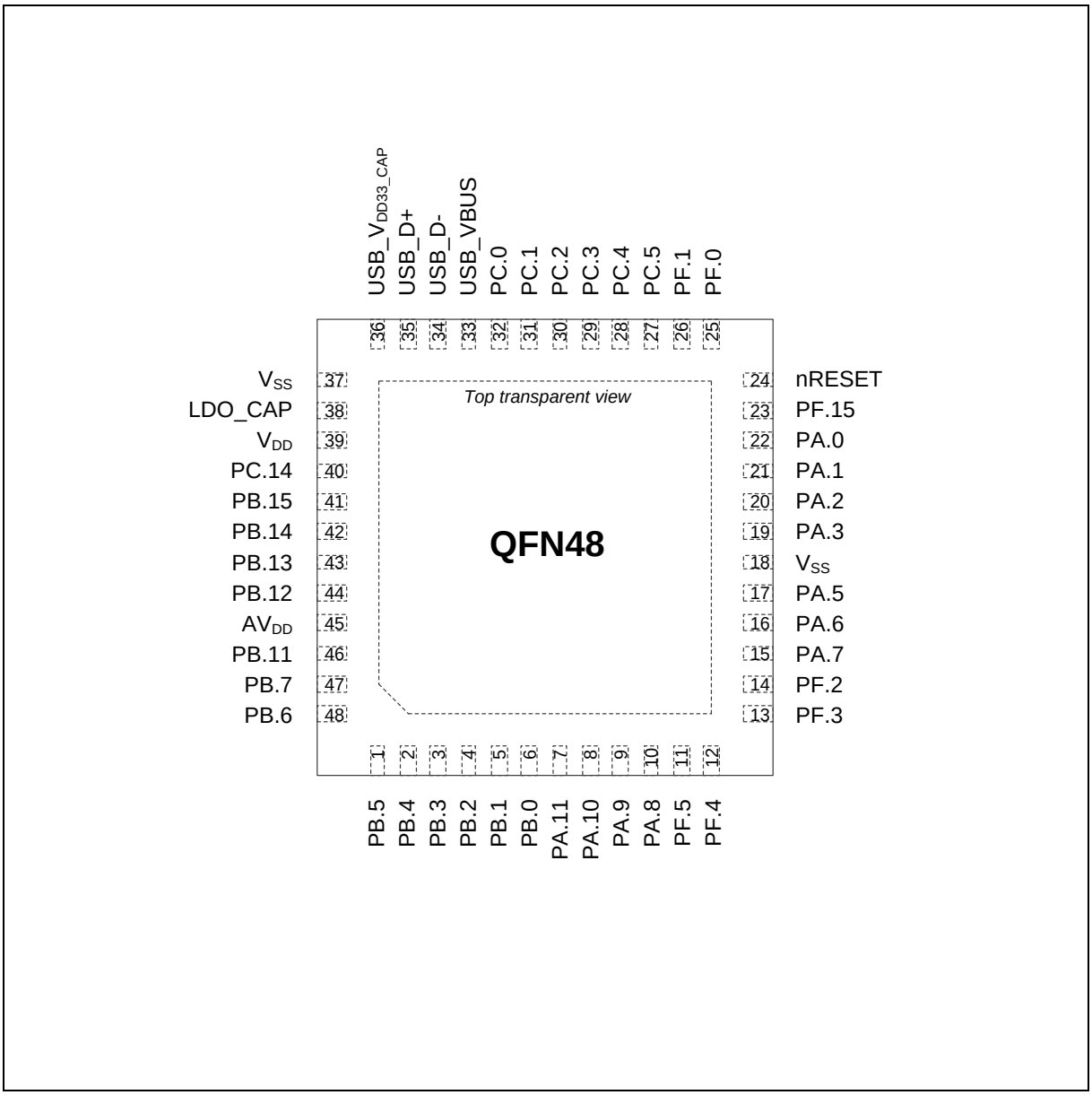


Figure 4.1-3 NuMicro® NUC1262 QFN 48-pin Diagram

4.1.2 Multi-function Pin Diagram

4.1.2.1 *NuMicro® NUC1262 LQFP64 Pin Multi-function Pin Diagram*

Corresponding Part Number: NUC1262SE4AE

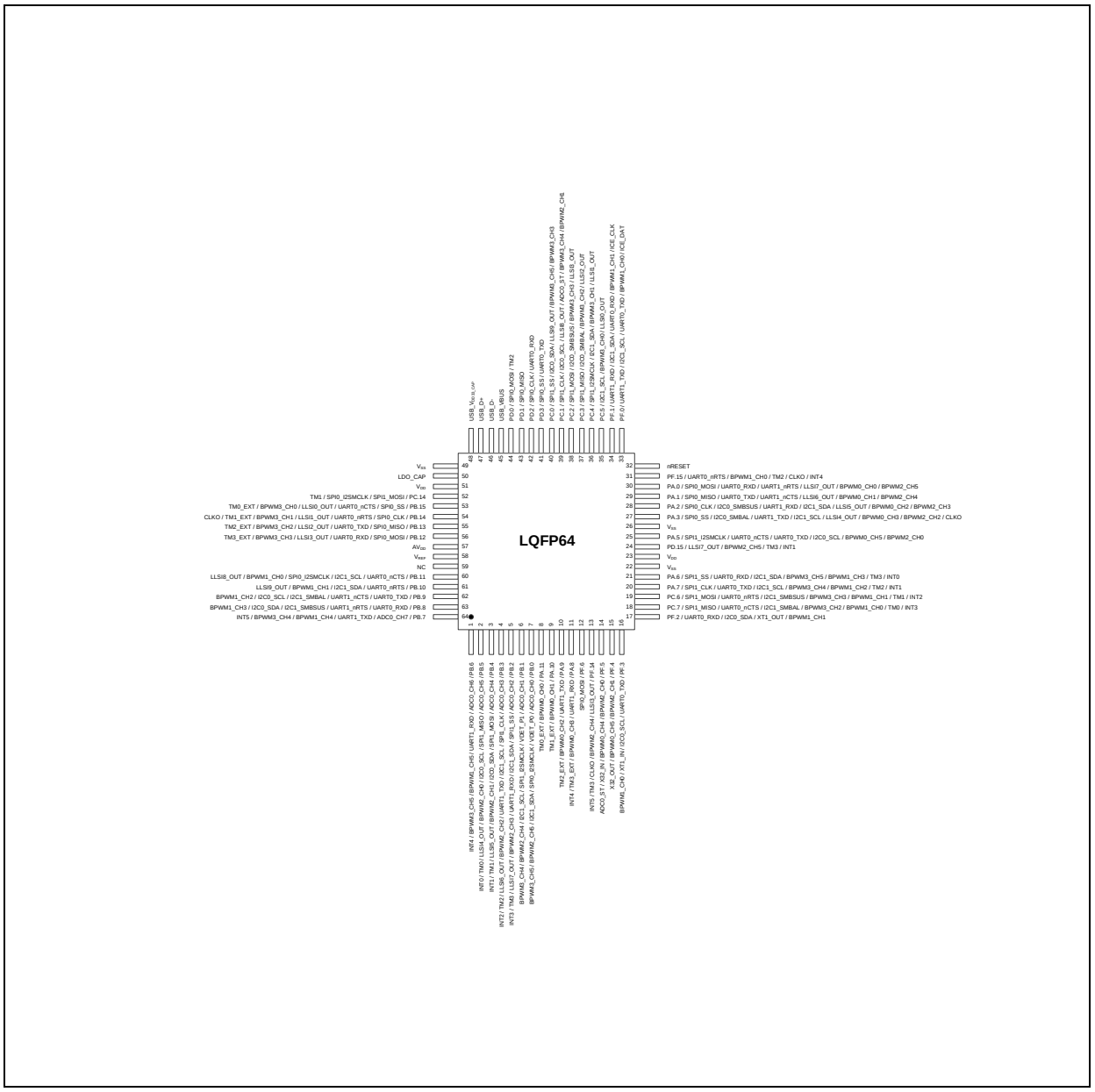


Figure 4.1-4 NuMicro® NUC1262 LQFP 64-pin Multi-function Pin Diagram

4.1.2.2 *NuMicro® NUC1262 LQFP48 Pin Multi-function Pin Diagram*

Corresponding Part Number: NUC1262LE4AE

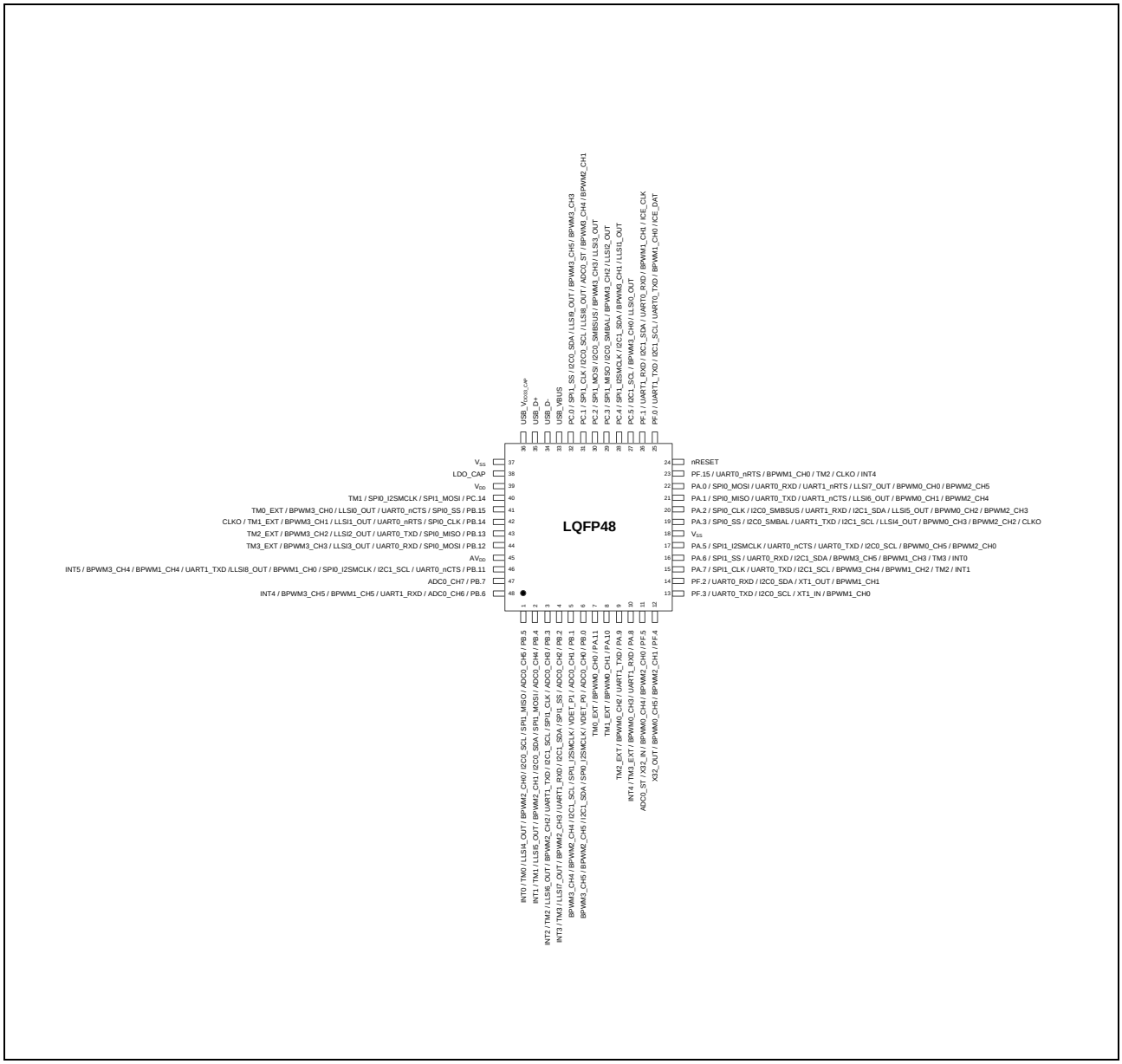


Figure 4.1-5 NuMicro® NUC1262 LQFP 48-pin Multi-function Pin Diagram

4.1.2.3 *NuMicro® NUC1262 QFN48 Pin Multi-function Pin Diagram*

Corresponding Part Number: NUC1262NE4AE

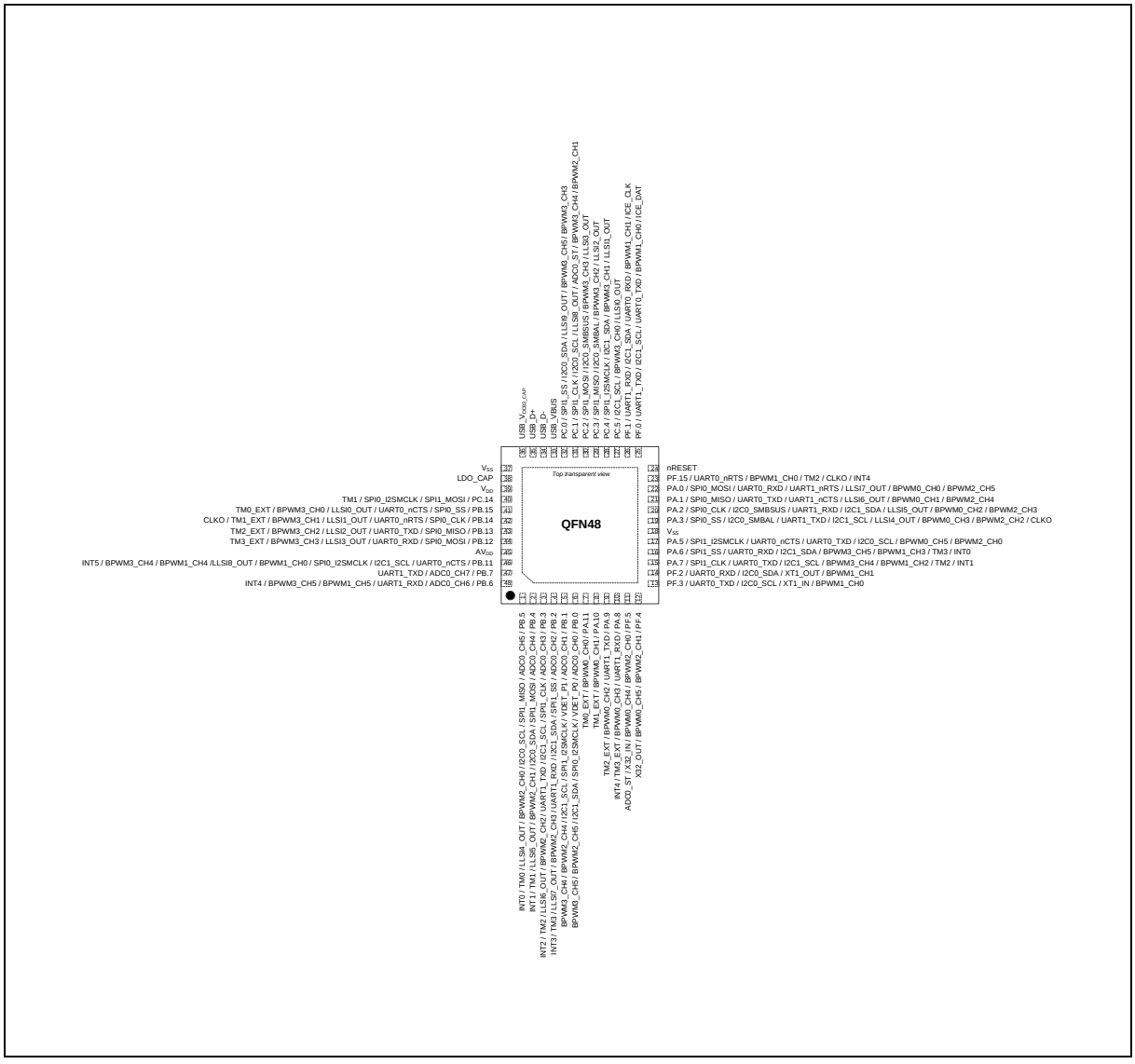


Figure 4.1-6 NuMicro® NUC1262 QFN 48-pin Multi-function Pin Diagram

4.2 Pin Mapping

Different part number with same package might has different function. Please refer to the selection guide in section 3.2, Pin Configuration in section 4.1 or NuTool - PinConfig.

Corresponding Part Number: NUC1262NE4AE, NUC1262LE4AE, NUC1262SE4AE

	NUC1262		
Pin Name	48 Pin	48 Pin	64 Pin
PB.6	48	48	1
PB.5	1	1	2
PB.4	2	2	3
PB.3	3	3	4
PB.2	4	4	5
PB.1	5	5	6
PB.0	6	6	7
PA.11	7	7	8
PA.10	8	8	9
PA.9	9	9	10
PA.8	10	10	11
PF.6			12
PF.14			13
PF.5	11	11	14
PF.4	12	12	15
PF.3	13	13	16
PF.2	14	14	17
PC.7			18
PC.6			19
PA.7	15	15	20
PA.6	16	16	21
V_{SS}			22
V_{DD}			23
PD.15			24
PA.5	17	17	25
V_{SS}	18	18	26
PA.3	19	19	27
PA.2	20	20	28
PA.1	21	21	29
PA.0	22	22	30

PF.15	23	23	31
nRESET	24	24	32
PF.0	25	25	33
PF.1	26	26	34
PC.5	27	27	35
PC.4	28	28	36
PC.3	29	29	37
PC.2	30	30	38
PC.1	31	31	39
PC.0	32	32	40
PD.3			41
PD.2			42
PD.1			43
PD.0			44
USB_VBUS	33	33	45
USB_D-	34	34	46
USB_D+	35	35	47
USB_VDD33_CAP	36	36	48
V_{SS}	37	37	49
LDO_CAP	38	38	50
V_{DD}	39	39	51
PC.14	40	40	52
PB.15	41	41	53
PB.14	42	42	54
PB.13	43	43	55
PB.12	44	44	56
AV_{DD}	45	45	57
V_{REF}			58
NC			59
PB.11	46	46	60
PB.10			61
PB.9			62
PB.8			63
PB.7	47	47	64

4.3 Pin Functional Description

4.3.1 Multi-function Summary Table

Group	Pin Name	GPIO	MFP	Type	Description
ADC0	ADC0_CH0	PB.0	MFP1	A	ADC0 channel 0 analog input.
	ADC0_CH1	PB.1	MFP1	A	ADC0 channel 1 analog input.
	ADC0_CH2	PB.2	MFP1	A	ADC0 channel 2 analog input.
	ADC0_CH3	PB.3	MFP1	A	ADC0 channel 3 analog input.
	ADC0_CH4	PB.4	MFP1	A	ADC0 channel 4 analog input.
	ADC0_CH5	PB.5	MFP1	A	ADC0 channel 5 analog input.
	ADC0_CH6	PB.6	MFP1	A	ADC0 channel 6 analog input.
	ADC0_CH7	PB.7	MFP1	A	ADC0 channel 7 analog input.
	ADC0_ST	PF.5	MFP11	I	ADC0 external trigger input pin.
		PC.1	MFP11	I	
BPWM0	BPWM0_CH0	PA.11	MFP9	I/O	BPWM0 channel 0 output/capture input.
		PA.0	MFP12	I/O	
	BPWM0_CH1	PA.10	MFP9	I/O	BPWM0 channel 1 output/capture input.
		PA.1	MFP12	I/O	
	BPWM0_CH2	PA.9	MFP9	I/O	BPWM0 channel 2 output/capture input.
		PA.2	MFP12	I/O	
	BPWM0_CH3	PA.8	MFP9	I/O	BPWM0 channel 3 output/capture input.
		PA.3	MFP12	I/O	
	BPWM0_CH4	PF.5	MFP8	I/O	BPWM0 channel 4 output/capture input.
	BPWM0_CH5	PF.4	MFP8	I/O	BPWM0 channel 5 output/capture input.
		PA.5	MFP12	I/O	
BPWM1	BPWM1_CH0	PF.3	MFP11	I/O	BPWM1 channel 0 output/capture input.
		PF.15	MFP12	I/O	
		PF.0	MFP12	I/O	
		PC.7	MFP12	I/O	
		PB.11	MFP10	I/O	
	BPWM1_CH1	PF.2	MFP11	I/O	BPWM1 channel 1 output/capture input.
		PF.1	MFP12	I/O	
		PC.6	MFP12	I/O	
		PB.10	MFP10	I/O	
	BPWM1_CH2	PA.7	MFP12	I/O	BPWM1 channel 2 output/capture input.
		PB.9	MFP10	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
	BPWM1_CH3	PA.6	MFP12	I/O	BPWM1 channel 3 output/capture input.
		PB.8	MFP10	I/O	
	BPWM1_CH4	PB.7	MFP10	I/O	BPWM1 channel 4 output/capture input.
	BPWM1_CH5	PB.6	MFP10	I/O	BPWM1 channel 5 output/capture input.
BPWM2	BPWM2_CH0	PB.5	MFP11	I/O	BPWM2 channel 0 output/capture input.
		PF.5	MFP7	I/O	
		PA.5	MFP13	I/O	
	BPWM2_CH1	PB.4	MFP11	I/O	BPWM2 channel 1 output/capture input.
		PF.4	MFP7	I/O	
		PC.1	MFP13	I/O	
	BPWM2_CH2	PB.3	MFP11	I/O	BPWM2 channel 2 output/capture input.
		PA.3	MFP13	I/O	
	BPWM2_CH3	PB.2	MFP11	I/O	BPWM2 channel 3 output/capture input.
		PA.2	MFP13	I/O	
	BPWM2_CH4	PB.1	MFP11	I/O	BPWM2 channel 4 output/capture input.
		PA.1	MFP13	I/O	
		PF.14	MFP12	I/O	
	BPWM2_CH5	PB.0	MFP11	I/O	BPWM2 channel 5 output/capture input.
		PA.0	MFP13	I/O	
		PD.15	MFP12	I/O	
BPWM3	BPWM3_CH0	PC.5	MFP12	I/O	BPWM3 channel 0 output/capture input.
		PB.15	MFP11	I/O	
	BPWM3_CH1	PC.4	MFP12	I/O	BPWM3 channel 1 output/capture input.
		PB.14	MFP11	I/O	
	BPWM3_CH2	PC.3	MFP12	I/O	BPWM3 channel 2 output/capture input.
		PB.13	MFP11	I/O	
		PC.7	MFP11	I/O	
	BPWM3_CH3	PC.2	MFP12	I/O	BPWM3 channel 3 output/capture input.
		PC.0	MFP13	I/O	
		PB.12	MFP11	I/O	
		PC.6	MFP11	I/O	
	BPWM3_CH4	PB.1	MFP12	I/O	BPWM3 channel 4 output/capture input.
		PA.7	MFP11	I/O	
		PC.1	MFP12	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
		PB.7	MFP12	I/O	
	BPWM3_CH5	PB.0	MFP12	I/O	BPWM3 channel 5 output/capture input.
		PA.6	MFP11	I/O	
		PC.0	MFP12	I/O	
		PB.6	MFP12	I/O	
CLKO	CLKO	PA.3	MFP14	O	Clock Out
		PF.15	MFP14	O	
		PB.14	MFP14	O	
		PF.14	MFP13	O	
I2C0	I2C0_SCL	PB.5	MFP6	I/O	I2C0 clock pin.
		PF.3	MFP4	I/O	
		PA.5	MFP9	I/O	
		PC.1	MFP9	I/O	
		PB.9	MFP9	I/O	
	I2C0_SDA	PB.4	MFP6	I/O	I2C0 data input/output pin.
		PF.2	MFP4	I/O	
		PC.0	MFP9	I/O	
		PB.8	MFP9	I/O	
	I2C0_SMBAL	PA.3	MFP7	O	I2C0 SMBus SMBALTER pin
		PC.3	MFP9	O	
	I2C0_SMBSUS	PA.2	MFP7	O	I2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
		PC.2	MFP9	O	
I2C1	I2C1_SCL	PB.3	MFP4	I/O	I2C1 clock pin.
		PB.1	MFP9	I/O	
		PA.7	MFP8	I/O	
		PA.3	MFP9	I/O	
		PF.0	MFP3	I/O	
		PC.5	MFP9	I/O	
		PB.11	MFP7	I/O	
	I2C1_SDA	PB.2	MFP4	I/O	I2C1 data input/output pin.
		PB.0	MFP9	I/O	
		PA.6	MFP8	I/O	
		PA.2	MFP9	I/O	
		PF.1	MFP3	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
		PC.4	MFP9	I/O	
		PB.10	MFP7	I/O	
	I2C1_SMBAL	PC.7	MFP8	O	I2C1 SMBus SMBALTER pin
		PB.9	MFP7	O	
	I2C1_SMBSUS	PC.6	MFP8	O	I2C1 SMBus SMBSUS pin (PMBus CONTROL pin)
		PB.8	MFP7	O	
ICE	ICE_CLK	PF.1	MFP14	I	Serial wired debugger clock pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
	ICE_DAT	PF.0	MFP14	I/O	Serial wired debugger data pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
INT0	INT0	PB.5	MFP15	I	External interrupt 0 input pin.
		PA.6	MFP15	I	
INT1	INT1	PB.4	MFP15	I	External interrupt 1 input pin.
		PA.7	MFP15	I	
		PD.15	MFP15	I	
INT2	INT2	PB.3	MFP15	I	External interrupt 2 input pin.
		PC.6	MFP15	I	
INT3	INT3	PB.2	MFP15	I	External interrupt 3 input pin.
		PC.7	MFP15	I	
INT4	INT4	PA.8	MFP15	I	External interrupt 4 input pin.
		PF.15	MFP15	I	
		PB.6	MFP13	I	
INT5	INT5	PB.7	MFP13	I	External interrupt 5 input pin.
		PF.14	MFP15	I	
LLSI0	LLSI0_OUT	PC.5	MFP15	O	LED Lighting Strip Interface 0 output pin.
		PB.15	MFP10	O	
LLSI1	LLSI1_OUT	PC.4	MFP15	O	LED Lighting Strip Interface 1 output pin.
		PB.14	MFP10	O	
LLSI2	LLSI2_OUT	PC.3	MFP15	O	LED Lighting Strip Interface 2 output pin.
		PB.13	MFP10	O	
LLSI3	LLSI3_OUT	PC.2	MFP15	O	LED Lighting Strip Interface 3 output pin.
		PB.12	MFP10	O	
		PF.14	MFP11	O	
LLSI4	LLSI4_OUT	PB.5	MFP12	O	LED Lighting Strip Interface 4 output pin.

Group	Pin Name	GPIO	MFP	Type	Description
		PA.3	MFP10	O	
LLSI5	LLSI5_OUT	PB.4	MFP12	O	LED Lighting Strip Interface 5 output pin.
		PA.2	MFP10	O	
LLSI6	LLSI6_OUT	PB.3	MFP12	O	LED Lighting Strip Interface 6 output pin.
		PA.1	MFP10	O	
LLSI7	LLSI7_OUT	PB.2	MFP12	O	LED Lighting Strip Interface 7 output pin.
		PA.0	MFP10	O	
		PD.15	MFP11	O	
LLSI8	LLSI8_OUT	PC.1	MFP10	O	LED Lighting Strip Interface 8 output pin.
		PB.11	MFP11	O	
LLSI9	LLSI9_OUT	PC.0	MFP10	O	LED Lighting Strip Interface 9 output pin.
		PB.10	MFP11	O	
SPI0	SPI0_CLK	PA.2	MFP4	I/O	SPI0 serial clock pin.
		PB.14	MFP4	I/O	
		PD.2	MFP4	I/O	
	SPI0_I2SMCLK	PB.0	MFP8	I/O	SPI0 I^2S master clock output pin
		PC.14	MFP4	I/O	
		PB.11	MFP9	I/O	
	SPI0_MISO	PA.1	MFP4	I/O	SPI0 MISO (Master In, Slave Out) pin.
		PB.13	MFP4	I/O	
		PD.1	MFP4	I/O	
	SPI0_MOSI	PA.0	MFP4	I/O	SPI0 MOSI (Master Out, Slave In) pin.
		PB.12	MFP4	I/O	
		PF.6	MFP5	I/O	
		PD.0	MFP4	I/O	
	SPI0_SS	PA.3	MFP4	I/O	SPI0 slave select pin.
		PB.15	MFP4	I/O	
		PD.3	MFP4	I/O	
SPI1	SPI1_CLK	PB.3	MFP2	I/O	SPI1 serial clock pin.
		PA.7	MFP2	I/O	
		PC.1	MFP2	I/O	
	SPI1_I2SMCLK	PB.1	MFP2	I/O	SPI1 I^2S master clock output pin
		PA.5	MFP2	I/O	
		PC.4	MFP2	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
	SPI1_MISO	PB.5	MFP2	I/O	SPI1 MISO (Master In, Slave Out) pin.
		PC.3	MFP2	I/O	
		PC.7	MFP4	I/O	
	SPI1_MOSI	PB.4	MFP2	I/O	SPI1 MOSI (Master Out, Slave In) pin.
		PC.2	MFP2	I/O	
		PC.14	MFP2	I/O	
		PC.6	MFP4	I/O	
	SPI1_SS	PB.2	MFP2	I/O	SPI1 slave select pin.
		PA.6	MFP2	I/O	
		PC.0	MFP2	I/O	
TM0	TM0	PB.5	MFP14	I/O	Timer0 event counter input/toggle output pin.
		PC.7	MFP14	I/O	
	TM0_EXT	PA.11	MFP13	I/O	Timer0 external capture input/toggle output pin.
		PB.15	MFP13	I/O	
TM1	TM1	PB.4	MFP14	I/O	Timer1 event counter input/toggle output pin.
		PC.14	MFP13	I/O	
		PC.6	MFP14	I/O	
	TM1_EXT	PA.10	MFP13	I/O	Timer1 external capture input/toggle output pin.
		PB.14	MFP13	I/O	
TM2	TM2	PB.3	MFP14	I/O	Timer2 event counter input/toggle output pin.
		PA.7	MFP14	I/O	
		PF.15	MFP13	I/O	
		PD.0	MFP14	I/O	
	TM2_EXT	PA.9	MFP13	I/O	Timer2 external capture input/toggle output pin.
		PB.13	MFP13	I/O	
TM3	TM3	PB.2	MFP14	I/O	Timer3 event counter input/toggle output pin.
		PA.6	MFP14	I/O	
		PF.14	MFP14	I/O	
		PD.15	MFP14	I/O	
	TM3_EXT	PA.8	MFP13	I/O	Timer3 external capture input/toggle output pin.
		PB.12	MFP13	I/O	
UART0	UART0_RXD	PF.2	MFP3	I	UART0 data receiver input pin.
		PA.6	MFP7	I	
		PA.0	MFP7	I	

Group	Pin Name	GPIO	MFP	Type	Description
		PF.1	MFP4	I	
		PB.12	MFP6	I	
		PD.2	MFP9	I	
		PB.8	MFP5	I	
	UART0_TXD	PF.3	MFP3	O	UART0 data transmitter output pin.
		PA.7	MFP7	O	
		PA.5	MFP8	O	
		PA.1	MFP7	O	
		PF.0	MFP4	O	
		PB.13	MFP6	O	
		PD.3	MFP9	O	
		PB.9	MFP5	O	
	UART0_nCTS	PA.5	MFP7	I	UART0 clear to Send input pin.
		PB.15	MFP6	I	
		PC.7	MFP7	I	
		PB.11	MFP5	I	
	UART0_nRTS	PF.15	MFP7	O	UART0 request to Send output pin.
		PB.14	MFP6	O	
		PC.6	MFP7	O	
		PB.10	MFP5	O	
UART1	UART1_RXD	PB.2	MFP6	I	UART1 data receiver input pin.
		PA.8	MFP7	I	
		PA.2	MFP8	I	
		PF.1	MFP2	I	
		PB.6	MFP6	I	
	UART1_TXD	PB.3	MFP6	O	UART1 data transmitter output pin.
		PA.9	MFP7	O	
		PA.3	MFP8	O	
		PF.0	MFP2	O	
		PB.7	MFP6	O	
	UART1_nCTS	PA.1	MFP8	I	UART1 clear to Send input pin.
		PB.9	MFP6	I	
	UART1_nRTS	PA.0	MFP8	O	UART1 request to Send output pin.
		PB.8	MFP6	O	

Group	Pin Name	GPIO	MFP	Type	Description
VDET	VDET_P0	PB.0	MFP1	A	Voltage detector positive input 0 pin.
	VDET_P1	PB.1	MFP1	A	Voltage detector positive input 1 pin.
X32	X32_IN	PF.5	MFP10	I	External 32.768 kHz crystal input pin.
	X32_OUT	PF.4	MFP10	O	External 32.768 kHz crystal output pin.
XT1	XT1_IN	PF.3	MFP10	I	External 4~24 MHz (high speed) crystal input pin.
	XT1_OUT	PF.2	MFP10	O	External 4~24 MHz (high speed) crystal output pin.

4.3.2 Multi-function Summary Table Sorted by GPIO

	Pin Name	Type	MFP	Description
PA.0	PA.0	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
	UART0_RXD	I	MFP7	UART0 data receiver input pin.
	UART1_nRTS	O	MFP8	UART1 request to Send output pin.
	LLSI7_OUT	O	MFP10	LED Lighting Strip Interface 7 output pin.
	BPWM0_CH0	I/O	MFP12	BPWM0 channel 0 output/capture input.
	BPWM2_CH5	I/O	MFP13	BPWM2 channel 5 output/capture input.
PA.1	PA.1	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
	UART0_TXD	O	MFP7	UART0 data transmitter output pin.
	UART1_nCTS	I	MFP8	UART1 clear to Send input pin.
	LLSI6_OUT	O	MFP10	LED Lighting Strip Interface 6 output pin.
	BPWM0_CH1	I/O	MFP12	BPWM0 channel 1 output/capture input.
	BPWM2_CH4	I/O	MFP13	BPWM2 channel 4 output/capture input.
PA.2	PA.2	I/O	MFP0	General purpose digital I/O pin.
	SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
	I2C0_SMBSUS	O	MFP7	I2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
	UART1_RXD	I	MFP8	UART1 data receiver input pin.
	I2C1_SDA	I/O	MFP9	I2C1 data input/output pin.
	LLSI5_OUT	O	MFP10	LED Lighting Strip Interface 5 output pin.
	BPWM0_CH2	I/O	MFP12	BPWM0 channel 2 output/capture input.
	BPWM2_CH3	I/O	MFP13	BPWM2 channel 3 output/capture input.
PA.3	PA.3	I/O	MFP0	General purpose digital I/O pin.
	SPI0_SS	I/O	MFP4	SPI0 slave select pin.
	I2C0_SMBAL	O	MFP7	I2C0 SMBus SMBALTER pin
	UART1_TXD	O	MFP8	UART1 data transmitter output pin.
	I2C1_SCL	I/O	MFP9	I2C1 clock pin.
	LLSI4_OUT	O	MFP10	LED Lighting Strip Interface 4 output pin.
	BPWM0_CH3	I/O	MFP12	BPWM0 channel 3 output/capture input.
	BPWM2_CH2	I/O	MFP13	BPWM2 channel 2 output/capture input.
	CLKO	O	MFP14	Clock Out
PA.5	PA.5	I/O	MFP0	General purpose digital I/O pin.
	SPI1_I2SMCLK	I/O	MFP2	SPI1 I^2S master clock output pin

	Pin Name	Type	MFP	Description
	UART0_nCTS	I	MFP7	UART0 clear to Send input pin.
	UART0_TXD	O	MFP8	UART0 data transmitter output pin.
	I2C0_SCL	I/O	MFP9	I2C0 clock pin.
	BPWM0_CH5	I/O	MFP12	BPWM0 channel 5 output/capture input.
	BPWM2_CH0	I/O	MFP13	BPWM2 channel 0 output/capture input.
PA.6	PA.6	I/O	MFP0	General purpose digital I/O pin.
	SPI1_SS	I/O	MFP2	SPI1 slave select pin.
	UART0_RXD	I	MFP7	UART0 data receiver input pin.
	I2C1_SDA	I/O	MFP8	I2C1 data input/output pin.
	BPWM3_CH5	I/O	MFP11	BPWM3 channel 5 output/capture input.
	BPWM1_CH3	I/O	MFP12	BPWM1 channel 3 output/capture input.
	TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
	INT0	I	MFP15	External interrupt 0 input pin.
PA.7	PA.7	I/O	MFP0	General purpose digital I/O pin.
	SPI1_CLK	I/O	MFP2	SPI1 serial clock pin.
	UART0_TXD	O	MFP7	UART0 data transmitter output pin.
	I2C1_SCL	I/O	MFP8	I2C1 clock pin.
	BPWM3_CH4	I/O	MFP11	BPWM3 channel 4 output/capture input.
	BPWM1_CH2	I/O	MFP12	BPWM1 channel 2 output/capture input.
	TM2	I/O	MFP14	Timer2 event counter input/toggle output pin.
	INT1	I	MFP15	External interrupt 1 input pin.
PA.8	PA.8	I/O	MFP0	General purpose digital I/O pin.
	UART1_RXD	I	MFP7	UART1 data receiver input pin.
	BPWM0_CH3	I/O	MFP9	BPWM0 channel 3 output/capture input.
	TM3_EXT	I/O	MFP13	Timer3 external capture input/toggle output pin.
	INT4	I	MFP15	External interrupt 4 input pin.
PA.9	PA.9	I/O	MFP0	General purpose digital I/O pin.
	UART1_TXD	O	MFP7	UART1 data transmitter output pin.
	BPWM0_CH2	I/O	MFP9	BPWM0 channel 2 output/capture input.
	TM2_EXT	I/O	MFP13	Timer2 external capture input/toggle output pin.
PA.10	PA.10	I/O	MFP0	General purpose digital I/O pin.
	BPWM0_CH1	I/O	MFP9	BPWM0 channel 1 output/capture input.
	TM1_EXT	I/O	MFP13	Timer1 external capture input/toggle output pin.
PA.11	PA.11	I/O	MFP0	General purpose digital I/O pin.

	Pin Name	Type	MFP	Description
	BPWM0_CH0	I/O	MFP9	BPWM0 channel 0 output/capture input.
	TM0_EXT	I/O	MFP13	Timer0 external capture input/toggle output pin.
PB.0	PB.0	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH0	A	MFP1	ADC0 channel 0 analog input.
	VDET_P0	A	MFP1	Voltage detector positive input 0 pin.
	SPI0_I2SMCLK	I/O	MFP8	SPI0 I^2S master clock output pin
	I2C1_SDA	I/O	MFP9	I2C1 data input/output pin.
	BPWM2_CH5	I/O	MFP11	BPWM2 channel 5 output/capture input.
	BPWM3_CH5	I/O	MFP12	BPWM3 channel 5 output/capture input.
PB.1	PB.1	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH1	A	MFP1	ADC0 channel 1 analog input.
	VDET_P1	A	MFP1	Voltage detector positive input 1 pin.
	SPI1_I2SMCLK	I/O	MFP2	SPI1 I^2S master clock output pin
	I2C1_SCL	I/O	MFP9	I2C1 clock pin.
	BPWM2_CH4	I/O	MFP11	BPWM2 channel 4 output/capture input.
	BPWM3_CH4	I/O	MFP12	BPWM3 channel 4 output/capture input.
PB.2	PB.2	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH2	A	MFP1	ADC0 channel 2 analog input.
	SPI1_SS	I/O	MFP2	SPI1 slave select pin.
	I2C1_SDA	I/O	MFP4	I2C1 data input/output pin.
	UART1_RXD	I	MFP6	UART1 data receiver input pin.
	BPWM2_CH3	I/O	MFP11	BPWM2 channel 3 output/capture input.
	LLSI7_OUT	O	MFP12	LED Lighting Strip Interface 7 output pin.
	TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
	INT3	I	MFP15	External interrupt 3 input pin.
PB.3	PB.3	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH3	A	MFP1	ADC0 channel 3 analog input.
	SPI1_CLK	I/O	MFP2	SPI1 serial clock pin.
	I2C1_SCL	I/O	MFP4	I2C1 clock pin.
	UART1_TXD	O	MFP6	UART1 data transmitter output pin.
	BPWM2_CH2	I/O	MFP11	BPWM2 channel 2 output/capture input.
	LLSI6_OUT	O	MFP12	LED Lighting Strip Interface 6 output pin.
	TM2	I/O	MFP14	Timer2 event counter input/toggle output pin.
	INT2	I	MFP15	External interrupt 2 input pin.

	Pin Name	Type	MFP	Description
PB.4	PB.4	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH4	A	MFP1	ADC0 channel 4 analog input.
	SPI1_MOSI	I/O	MFP2	SPI1 MOSI (Master Out, Slave In) pin.
	I2C0_SDA	I/O	MFP6	I2C0 data input/output pin.
	BPWM2_CH1	I/O	MFP11	BPWM2 channel 1 output/capture input.
	LLSI5_OUT	O	MFP12	LED Lighting Strip Interface 5 output pin.
	TM1	I/O	MFP14	Timer1 event counter input/toggle output pin.
	INT1	I	MFP15	External interrupt 1 input pin.
PB.5	PB.5	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH5	A	MFP1	ADC0 channel 5 analog input.
	SPI1_MISO	I/O	MFP2	SPI1 MISO (Master In, Slave Out) pin.
	I2C0_SCL	I/O	MFP6	I2C0 clock pin.
	BPWM2_CH0	I/O	MFP11	BPWM2 channel 0 output/capture input.
	LLSI4_OUT	O	MFP12	LED Lighting Strip Interface 4 output pin.
	TM0	I/O	MFP14	Timer0 event counter input/toggle output pin.
	INT0	I	MFP15	External interrupt 0 input pin.
PB.6	PB.6	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH6	A	MFP1	ADC0 channel 6 analog input.
	UART1_RXD	I	MFP6	UART1 data receiver input pin.
	BPWM1_CH5	I/O	MFP10	BPWM1 channel 5 output/capture input.
	BPWM3_CH5	I/O	MFP12	BPWM3 channel 5 output/capture input.
	INT4	I	MFP13	External interrupt 4 input pin.
PB.7	PB.7	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH7	A	MFP1	ADC0 channel 7 analog input.
	UART1_TXD	O	MFP6	UART1 data transmitter output pin.
	BPWM1_CH4	I/O	MFP10	BPWM1 channel 4 output/capture input.
	BPWM3_CH4	I/O	MFP12	BPWM3 channel 4 output/capture input.
	INT5	I	MFP13	External interrupt 5 input pin.
PB.8	PB.8	I/O	MFP0	General purpose digital I/O pin.
	UART0_RXD	I	MFP5	UART0 data receiver input pin.
	UART1_nRTS	O	MFP6	UART1 request to Send output pin.
	I2C1_SMBSUS	O	MFP7	I2C1 SMBus SMBSUS pin (PMBus CONTROL pin)
	I2C0_SDA	I/O	MFP9	I2C0 data input/output pin.
	BPWM1_CH3	I/O	MFP10	BPWM1 channel 3 output/capture input.

	Pin Name	Type	MFP	Description
PB.9	PB.9	I/O	MFP0	General purpose digital I/O pin.
	UART0_TXD	O	MFP5	UART0 data transmitter output pin.
	UART1_nCTS	I	MFP6	UART1 clear to Send input pin.
	I2C1_SMBAL	O	MFP7	I2C1 SMBus SMBALTER pin
	I2C0_SCL	I/O	MFP9	I2C0 clock pin.
	BPWM1_CH2	I/O	MFP10	BPWM1 channel 2 output/capture input.
PB.10	PB.10	I/O	MFP0	General purpose digital I/O pin.
	UART0_nRTS	O	MFP5	UART0 request to Send output pin.
	I2C1_SDA	I/O	MFP7	I2C1 data input/output pin.
	BPWM1_CH1	I/O	MFP10	BPWM1 channel 1 output/capture input.
	LLSI9_OUT	O	MFP11	LED Lighting Strip Interface 9 output pin.
PB.11	PB.11	I/O	MFP0	General purpose digital I/O pin.
	UART0_nCTS	I	MFP5	UART0 clear to Send input pin.
	I2C1_SCL	I/O	MFP7	I2C1 clock pin.
	SPI0_I2SMCLK	I/O	MFP9	SPI0 I^2S master clock output pin
	BPWM1_CH0	I/O	MFP10	BPWM1 channel 0 output/capture input.
	LLSI8_OUT	O	MFP11	LED Lighting Strip Interface 8 output pin.
PB.12	PB.12	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
	UART0_RXD	I	MFP6	UART0 data receiver input pin.
	LLSI3_OUT	O	MFP10	LED Lighting Strip Interface 3 output pin.
	BPWM3_CH3	I/O	MFP11	BPWM3 channel 3 output/capture input.
	TM3_EXT	I/O	MFP13	Timer3 external capture input/toggle output pin.
PB.13	PB.13	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
	UART0_TXD	O	MFP6	UART0 data transmitter output pin.
	LLSI2_OUT	O	MFP10	LED Lighting Strip Interface 2 output pin.
	BPWM3_CH2	I/O	MFP11	BPWM3 channel 2 output/capture input.
	TM2_EXT	I/O	MFP13	Timer2 external capture input/toggle output pin.
PB.14	PB.14	I/O	MFP0	General purpose digital I/O pin.
	SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
	UART0_nRTS	O	MFP6	UART0 request to Send output pin.
	LLSI1_OUT	O	MFP10	LED Lighting Strip Interface 1 output pin.
	BPWM3_CH1	I/O	MFP11	BPWM3 channel 1 output/capture input.

	Pin Name	Type	MFP	Description
	TM1_EXT	I/O	MFP13	Timer1 external capture input/toggle output pin.
	CLKO	O	MFP14	Clock Out
PB.15	PB.15	I/O	MFP0	General purpose digital I/O pin.
	SPI0_SS	I/O	MFP4	SPI0 slave select pin.
	UART0_nCTS	I	MFP6	UART0 clear to Send input pin.
	LLSI0_OUT	O	MFP10	LED Lighting Strip Interface 0 output pin.
	BPWM3_CH0	I/O	MFP11	BPWM3 channel 0 output/capture input.
	TM0_EXT	I/O	MFP13	Timer0 external capture input/toggle output pin.
PC.0	PC.0	I/O	MFP0	General purpose digital I/O pin.
	SPI1_SS	I/O	MFP2	SPI1 slave select pin.
	I2C0_SDA	I/O	MFP9	I2C0 data input/output pin.
	LLSI9_OUT	O	MFP10	LED Lighting Strip Interface 9 output pin.
	BPWM3_CH5	I/O	MFP12	BPWM3 channel 5 output/capture input.
	BPWM3_CH3	I/O	MFP13	BPWM3 channel 3 output/capture input.
PC.1	PC.1	I/O	MFP0	General purpose digital I/O pin.
	SPI1_CLK	I/O	MFP2	SPI1 serial clock pin.
	I2C0_SCL	I/O	MFP9	I2C0 clock pin.
	LLSI8_OUT	O	MFP10	LED Lighting Strip Interface 8 output pin.
	ADC0_ST	I	MFP11	ADC0 external trigger input pin.
	BPWM3_CH4	I/O	MFP12	BPWM3 channel 4 output/capture input.
	BPWM2_CH1	I/O	MFP13	BPWM2 channel 1 output/capture input.
PC.2	PC.2	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MOSI	I/O	MFP2	SPI1 MOSI (Master Out, Slave In) pin.
	I2C0_SMBSUS	O	MFP9	I2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
	BPWM3_CH3	I/O	MFP12	BPWM3 channel 3 output/capture input.
	LLSI3_OUT	O	MFP15	LED Lighting Strip Interface 3 output pin.
PC.3	PC.3	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MISO	I/O	MFP2	SPI1 MISO (Master In, Slave Out) pin.
	I2C0_SMBAL	O	MFP9	I2C0 SMBus SMBALTER pin
	BPWM3_CH2	I/O	MFP12	BPWM3 channel 2 output/capture input.
	LLSI2_OUT	O	MFP15	LED Lighting Strip Interface 2 output pin.
PC.4	PC.4	I/O	MFP0	General purpose digital I/O pin.
	SPI1_I2SMCLK	I/O	MFP2	SPI1 I^2S master clock output pin
	I2C1_SDA	I/O	MFP9	I2C1 data input/output pin.

	Pin Name	Type	MFP	Description
	BPWM3_CH1	I/O	MFP12	BPWM3 channel 1 output/capture input.
	LLSI1_OUT	O	MFP15	LED Lighting Strip Interface 1 output pin.
PC.5	PC.5	I/O	MFP0	General purpose digital I/O pin.
	I2C1_SCL	I/O	MFP9	I2C1 clock pin.
	BPWM3_CH0	I/O	MFP12	BPWM3 channel 0 output/capture input.
	LLSI0_OUT	O	MFP15	LED Lighting Strip Interface 0 output pin.
PC.6	PC.6	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MOSI	I/O	MFP4	SPI1 MOSI (Master Out, Slave In) pin.
	UART0_nRTS	O	MFP7	UART0 request to Send output pin.
	I2C1_SMBSUS	O	MFP8	I2C1 SMBus SMBSUS pin (PMBus CONTROL pin)
	BPWM3_CH3	I/O	MFP11	BPWM3 channel 3 output/capture input.
	BPWM1_CH1	I/O	MFP12	BPWM1 channel 1 output/capture input.
	TM1	I/O	MFP14	Timer1 event counter input/toggle output pin.
	INT2	I	MFP15	External interrupt 2 input pin.
PC.7	PC.7	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MISO	I/O	MFP4	SPI1 MISO (Master In, Slave Out) pin.
	UART0_nCTS	I	MFP7	UART0 clear to Send input pin.
	I2C1_SMBAL	O	MFP8	I2C1 SMBus SMBALTER pin
	BPWM3_CH2	I/O	MFP11	BPWM3 channel 2 output/capture input.
	BPWM1_CH0	I/O	MFP12	BPWM1 channel 0 output/capture input.
	TM0	I/O	MFP14	Timer0 event counter input/toggle output pin.
	INT3	I	MFP15	External interrupt 3 input pin.
PC.14	PC.14	I/O	MFP0	General purpose digital I/O pin.
	SPI1_MOSI	I/O	MFP2	SPI1 MOSI (Master Out, Slave In) pin.
	SPI0_I2SMCLK	I/O	MFP4	SPI0 I^2S master clock output pin
	TM1	I/O	MFP13	Timer1 event counter input/toggle output pin.
PD.0	PD.0	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
	TM2	I/O	MFP14	Timer2 event counter input/toggle output pin.
PD.1	PD.1	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
PD.2	PD.2	I/O	MFP0	General purpose digital I/O pin.
	SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
	UART0_RXD	I	MFP9	UART0 data receiver input pin.

	Pin Name	Type	MFP	Description
PD.3	PD.3	I/O	MFP0	General purpose digital I/O pin.
	SPI0_SS	I/O	MFP4	SPI0 slave select pin.
	UART0_TXD	O	MFP9	UART0 data transmitter output pin.
PD.15	PD.15	I/O	MFP0	General purpose digital I/O pin.
	LLSI7_OUT	O	MFP11	LED Lighting Strip Interface 7 output pin.
	BPWM2_CH5	I/O	MFP12	BPWM2 channel 5 output/capture input.
	TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
	INT1	I	MFP15	External interrupt 1 input pin.
PF.0	PF.0	I/O	MFP0	General purpose digital I/O pin.
	UART1_TXD	O	MFP2	UART1 data transmitter output pin.
	I2C1_SCL	I/O	MFP3	I2C1 clock pin.
	UART0_TXD	O	MFP4	UART0 data transmitter output pin.
	BPWM1_CH0	I/O	MFP12	BPWM1 channel 0 output/capture input.
	ICE_DAT	I/O	MFP14	Serial wired debugger data pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
PF.1	PF.1	I/O	MFP0	General purpose digital I/O pin.
	UART1_RXD	I	MFP2	UART1 data receiver input pin.
	I2C1_SDA	I/O	MFP3	I2C1 data input/output pin.
	UART0_RXD	I	MFP4	UART0 data receiver input pin.
	BPWM1_CH1	I/O	MFP12	BPWM1 channel 1 output/capture input.
	ICE_CLK	I	MFP14	Serial wired debugger clock pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
PF.2	PF.2	I/O	MFP0	General purpose digital I/O pin.
	UART0_RXD	I	MFP3	UART0 data receiver input pin.
	I2C0_SDA	I/O	MFP4	I2C0 data input/output pin.
	XT1_OUT	O	MFP10	External 4~24 MHz (high speed) crystal output pin.
	BPWM1_CH1	I/O	MFP11	BPWM1 channel 1 output/capture input.
PF.3	PF.3	I/O	MFP0	General purpose digital I/O pin.
	UART0_TXD	O	MFP3	UART0 data transmitter output pin.
	I2C0_SCL	I/O	MFP4	I2C0 clock pin.
	XT1_IN	I	MFP10	External 4~24 MHz (high speed) crystal input pin.
	BPWM1_CH0	I/O	MFP11	BPWM1 channel 0 output/capture input.
PF.4	PF.4	I/O	MFP0	General purpose digital I/O pin.
	BPWM2_CH1	I/O	MFP7	BPWM2 channel 1 output/capture input.

	Pin Name	Type	MFP	Description
	BPWM0_CH5	I/O	MFP8	BPWM0 channel 5 output/capture input.
	X32_OUT	O	MFP10	External 32.768 kHz crystal output pin.
PF.5	PF.5	I/O	MFP0	General purpose digital I/O pin.
	BPWM2_CH0	I/O	MFP7	BPWM2 channel 0 output/capture input.
	BPWM0_CH4	I/O	MFP8	BPWM0 channel 4 output/capture input.
	X32_IN	I	MFP10	External 32.768 kHz crystal input pin.
	ADC0_ST	I	MFP11	ADC0 external trigger input pin.
PF.6	PF.6	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MOSI	I/O	MFP5	SPI0 MOSI (Master Out, Slave In) pin.
PF.14	PF.14	I/O	MFP0	General purpose digital I/O pin.
	LLSI3_OUT	O	MFP11	LED Lighting Strip Interface 3 output pin.
	BPWM2_CH4	I/O	MFP12	BPWM2 channel 4 output/capture input.
	CLKO	O	MFP13	Clock Out
	TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
	INT5	I	MFP15	External interrupt 5 input pin.
PF.15	PF.15	I/O	MFP0	General purpose digital I/O pin.
	UART0_nRTS	O	MFP7	UART0 request to Send output pin.
	BPWM1_CH0	I/O	MFP12	BPWM1 channel 0 output/capture input.
	TM2	I/O	MFP13	Timer2 event counter input/toggle output pin.
	CLKO	O	MFP14	Clock Out
	INT4	I	MFP15	External interrupt 4 input pin.

Table 4.3-1 NUC1262 GPIO Multi-function Table

5 BLOCK DIAGRAM

5.1 NuMicro® NUC1262 Block Diagram

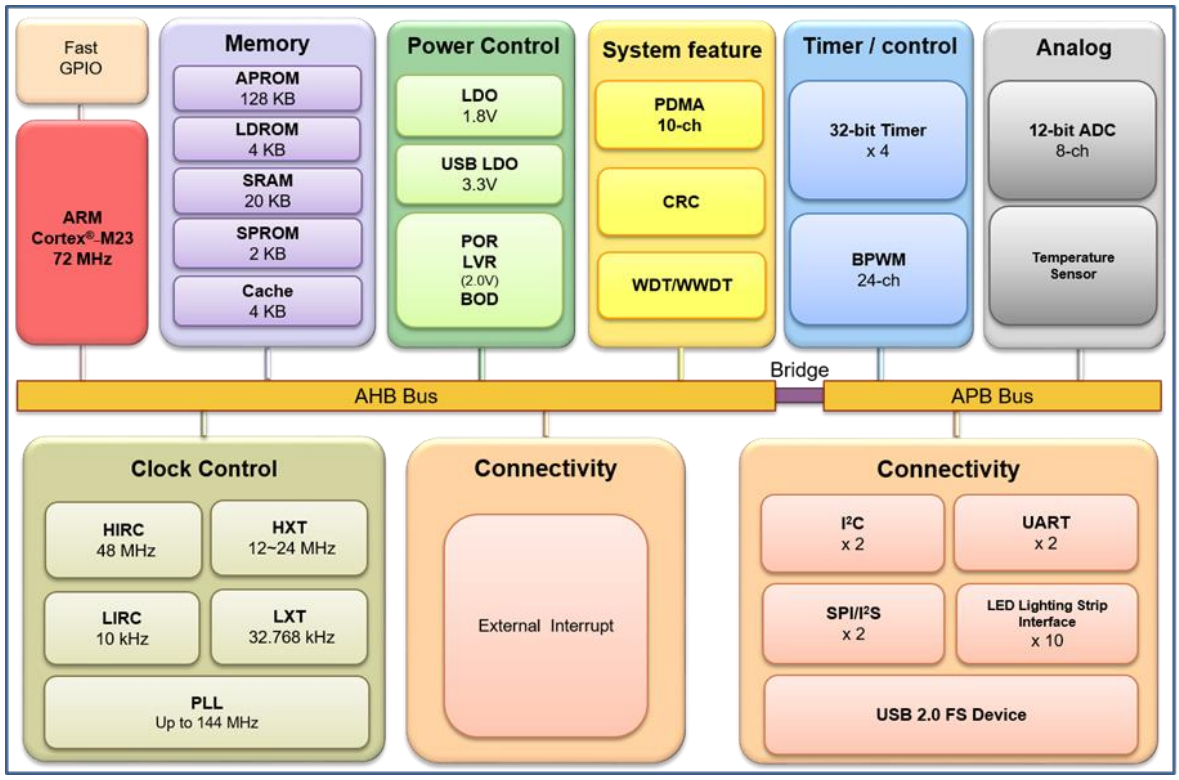


Figure 5.1-1 NuMicro® NUC1262 Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 Arm® Cortex®-M23 Core

The Cortex®-M23 processor is a low gate count, two-stage, and highly energy efficient 32-bit RISC processor, which has an AMBA AHB5 interface supporting Arm® TrustZone® technology, a debug access port supporting serial wire debug and single-cycle I/O ports. It has an NVIC component and MPU for memory-protection functionality. The processor also supports Security Extension. The NuMicro® NUC1262 is embedded with Cortex®-M23 processor. Figure 6.1-1 shows the functional controller of the processor.

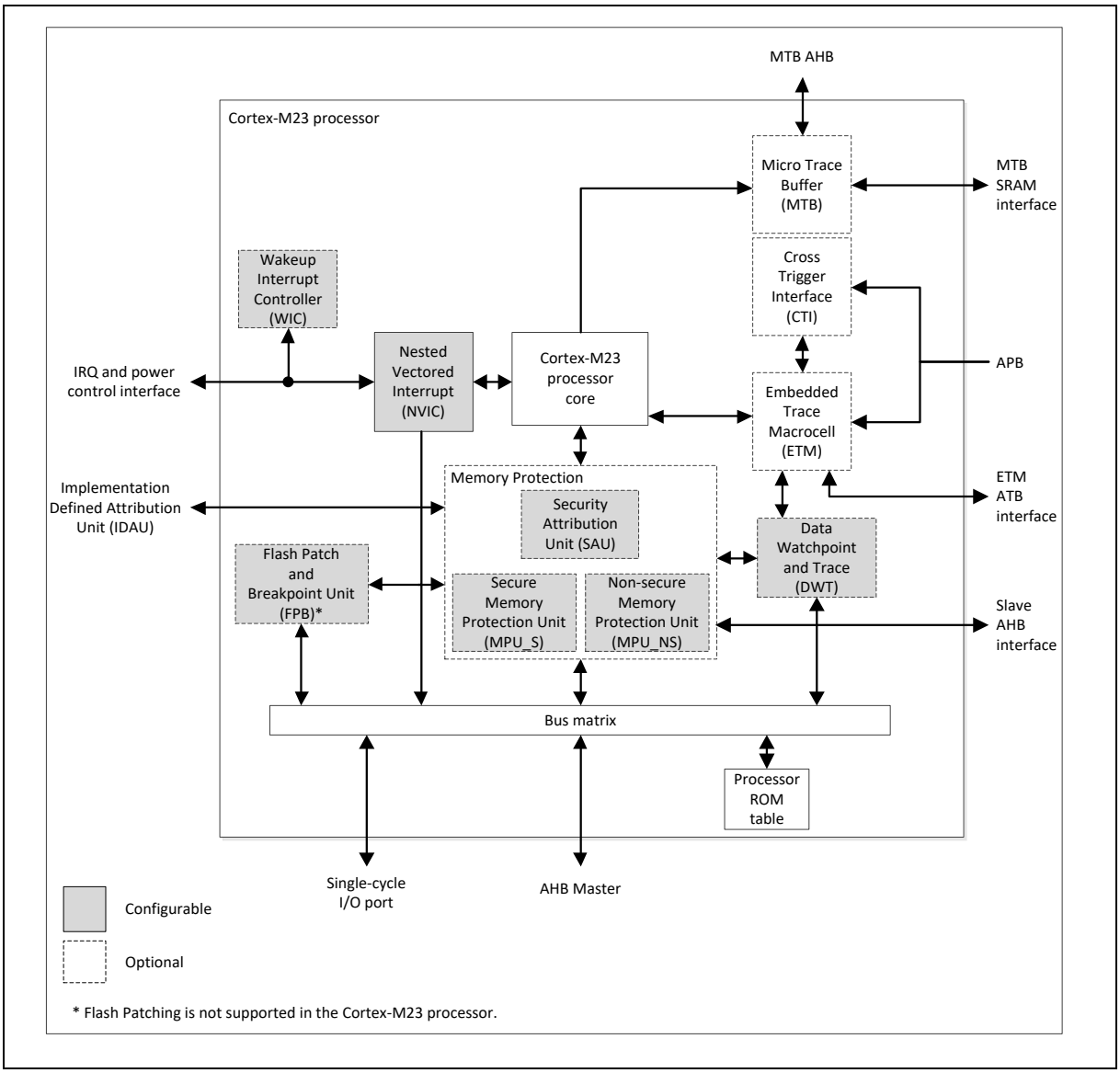


Figure 6.1-1 Cortex®-M23 Block Diagram

Cortex®-M23 processor features:

- Arm®v8-M Baseline architecture.
- Arm®v8-M Baseline Thumb®-2 instruction set that combines high code density with 32-bit performance.
- Support for single-cycle I/O access.

- Power control optimization of system components.
- Integrated sleep modes for low power consumption.
- Optimized code fetching for reduced Flash and ROM power consumption.
- A 32-bit Single cycle Hardware multiplier.
- A 32-bit Hardware divider.
- Deterministic, high-performance interrupt handling for time-critical applications.
- Deterministic instruction cycle timing.
- Support for system level debug authentication.
- Support for Arm® Debug Interface Architecture ADIv5.1 Serial Wire Debug (SWD).
- ETM for instruction trace.
- Separated privileged and unprivileged modes.
- Security Extension supporting a Secure and a Non-secure state.
- Security Attribution Unit (SAU).
- SysTick timers for both Secure and Non-secure states.
- A Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor with up to 240 interrupts.

6.2 System Manager

6.2.1 Overview

The system manager provides the functions of system control, power modes, wake-up sources, reset sources, system memory map, product ID and multi-function pin control. The following sections describe the functions for:

- System Reset
- Power Modes and Wake-up Sources
- System Power Distribution
- SRAM Memory organization
- System Control Register for Part Number ID, Chip Reset and Multi-function Pin Control
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset sources are from peripheral signals. Software reset can trigger reset through setting control registers.

- Hardware Reset Sources
  - Power-on Reset (POR)
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex®-M23 core Only by writing 1 to CPURST (SYS_IPRST0[1])

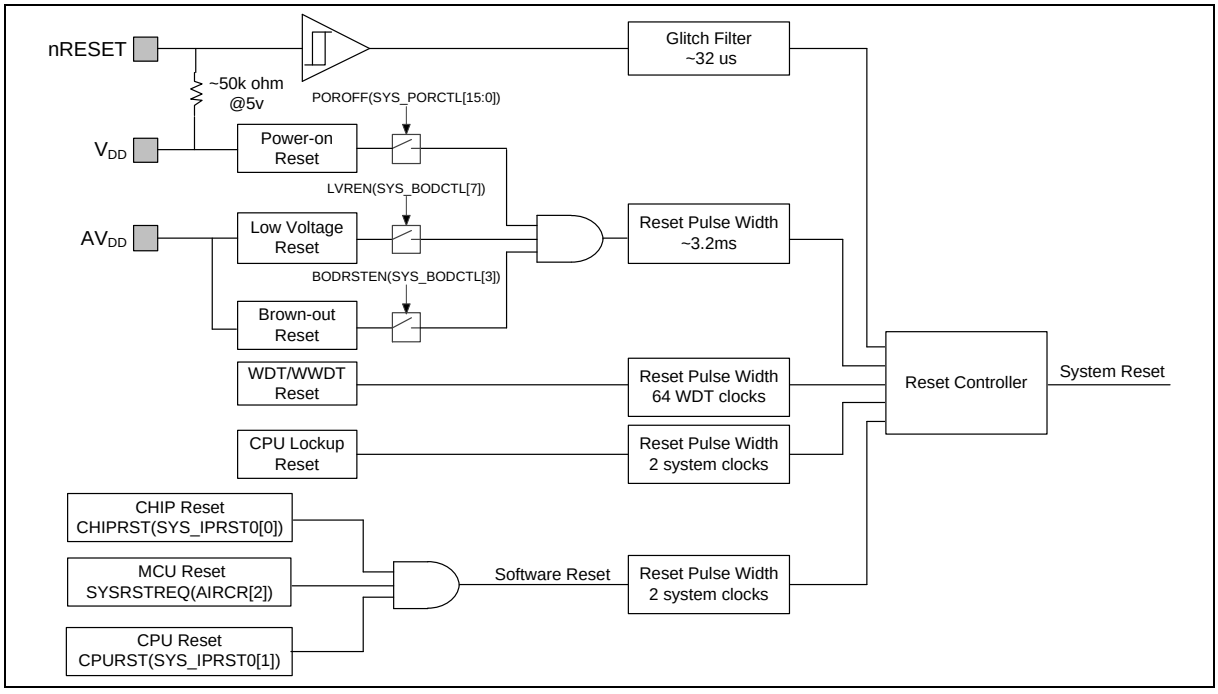


Figure 6.2-1 System Reset Sources

There are a total of 9 reset sources in the NuMicro® family. In general, CPU reset is used to reset Cortex®-M23 only; the other reset sources will reset Cortex®-M23 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6.2-1.

Reset Sources Register	POR	NRESET	WDT	LVR	BOD	Lockup	CHIP	MCU	CPU
SYS_RSTSTS	0x01	Bit 1 = 1	Bit 2 = 1	Bit 3 = 1	Bit 4 = 1	Bit 8 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIPRST (SYS_IPRST0[0])	0x0	-	-	-	-	-	-	-	-
BODEN (SYS_BODCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
BODVL (SYS_BODCTL[2:1])									
BODRSTEN (SYS_BODCTL[3])									
HXTEN (CLK_PWRCTL[0])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
LXTEN (CLK_PWRCTL[1])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
WDTCKEN (CLK_APBCLK0[0])	0x1	-	0x1	-	-	-	0x1	-	-
HCLKSEL (CLK_CLKSEL0[2:0])	0x7	0x7	0x7	0x7	0x7	0x7	0x7	0x7	-
WDTSEL (CLK_CLKSEL1[1:0])	0x3	0x3	-	-	-	-	-	-	-
HXTSTB (CLK_STATUS[0])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
LXTSTB (CLK_STATUS[1])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
PLLSTB (CLK_STATUS[2])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
HIRCSTB (CLK_STATUS[4])	0x0	-	-	-	-	-	-	-	-
CLKSFAIL (CLK_STATUS[7])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
RSTEN (WDT_CTL[1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
WDTEN (WDT_CTL[7])									
WDT_CTL except bit 1 and bit 7.	0x0700	0x0700	0x0700	0x0700	0x0700	-	0x0700	-	-
WDT_ALTCTL	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-

Reset Sources Register	POR	NRESET	WDT	LVR	BOD	Lockup	CHIP	MCU	CPU
WWDT_RLDCNT	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CTL	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	-	0x3F0800	-	-
WWDT_STATUS	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CNT	0x3F	0x3F	0x3F	0x3F	0x3F	-	0x3F	-	-
Other Peripheral Registers	Reset Value								-
Note: '-' means that the value of register keeps original setting.									

Table 6.2-1 Reset Value of Registers

6.2.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 V_{DD} and the state keeps longer than 32 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 V_{DD} and the state keeps longer than 32 us (glitch filter). The PINRF(SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6.2-2 shows the nRESET reset waveform.

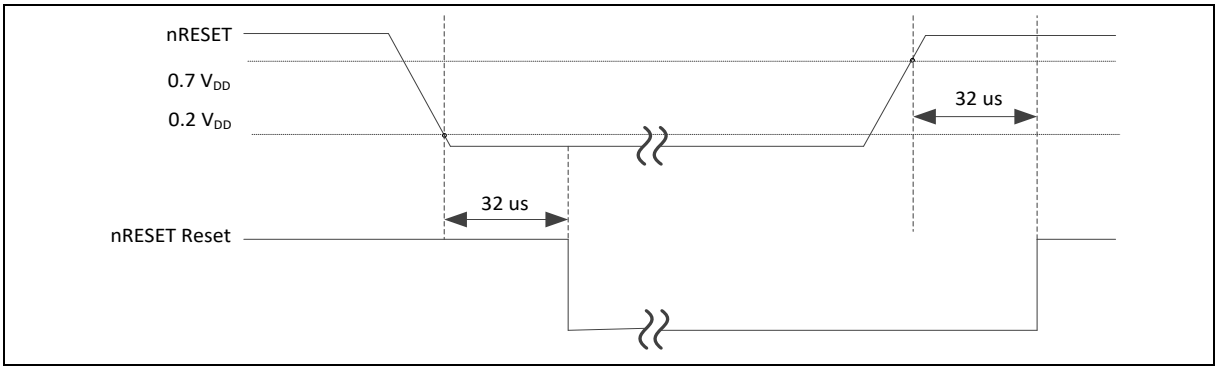


Figure 6.2-2 nRESET Reset Waveform

6.2.2.2 Power-on Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF(SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.2-3 shows the power-on reset waveform.

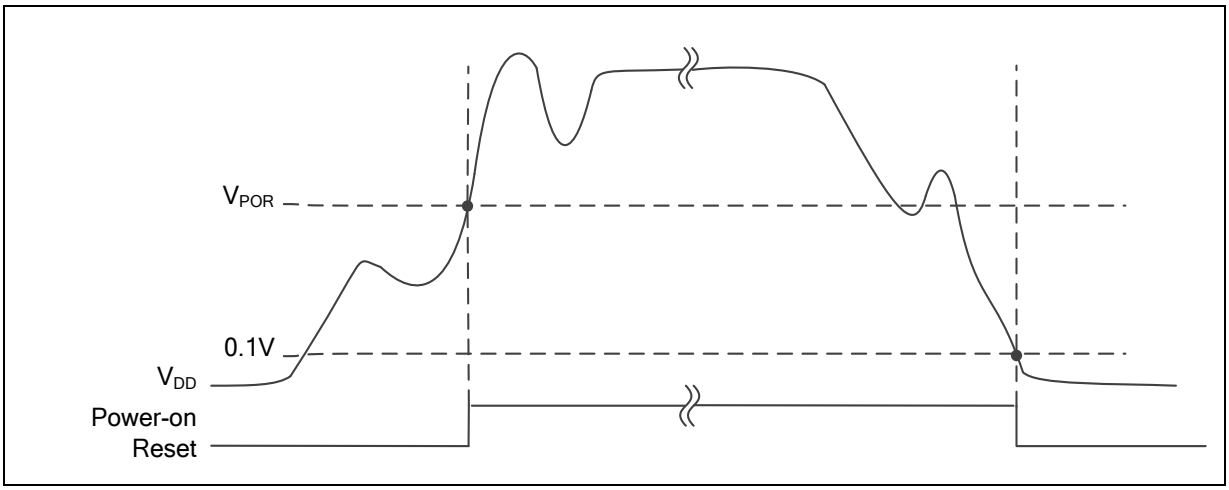


Figure 6.2-3 Power-on Reset (POR) Waveform

6.2.2.3 Low Voltage Reset (LVR)

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_BODCTL[7]) to 1, after 200us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6.2-4 shows the Low Voltage Reset waveform.

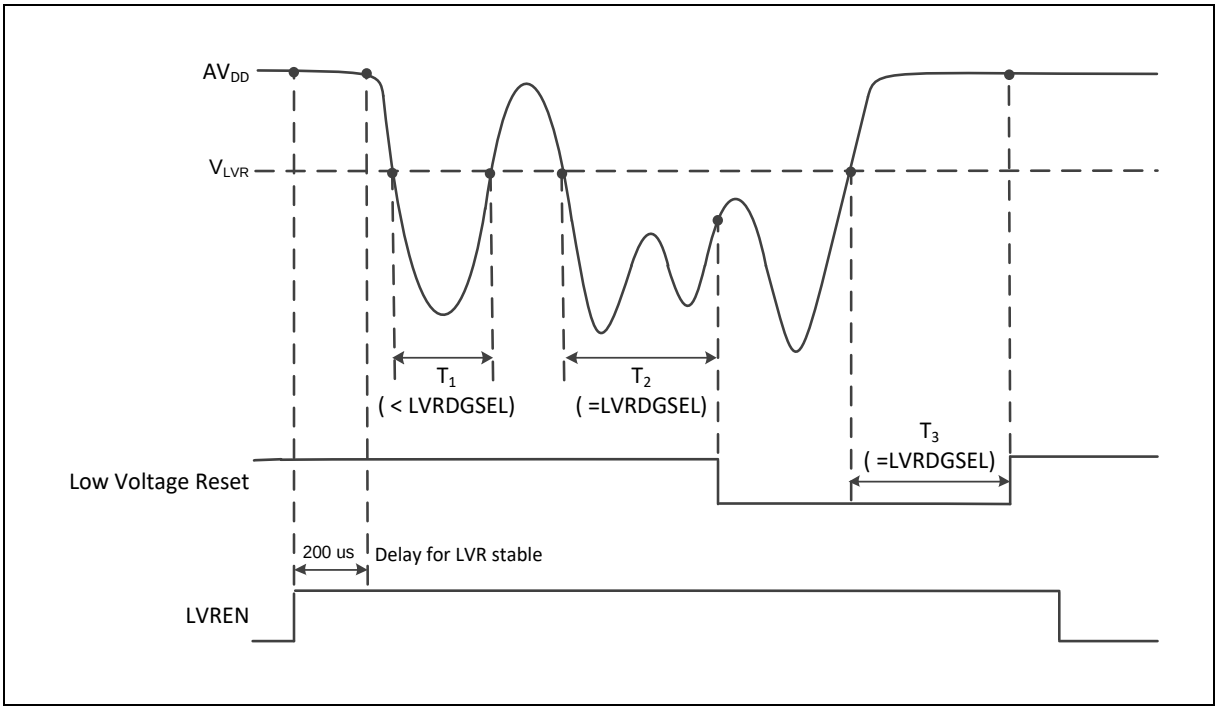


Figure 6.2-4 Low Voltage Reset (LVR) Waveform

6.2.2.4 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), Brown-out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} which is decided by BODEN (SYS_BODCTL[0]) and BODVL (SYS_BODCTL[2:1]) and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[10:8]), chip will be reset. The BOD reset will control the chip in reset state until the AV_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[10:8]). The default value of BODEN, BODVL and BODRSTEN (SYS_BODCTL[3]) is set by Flash controller user configuration register CBODEN (CONFIG0 [23]), CBOV (CONFIG0 [22:21]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6.2-5 shows the Brown-out Detector waveform.

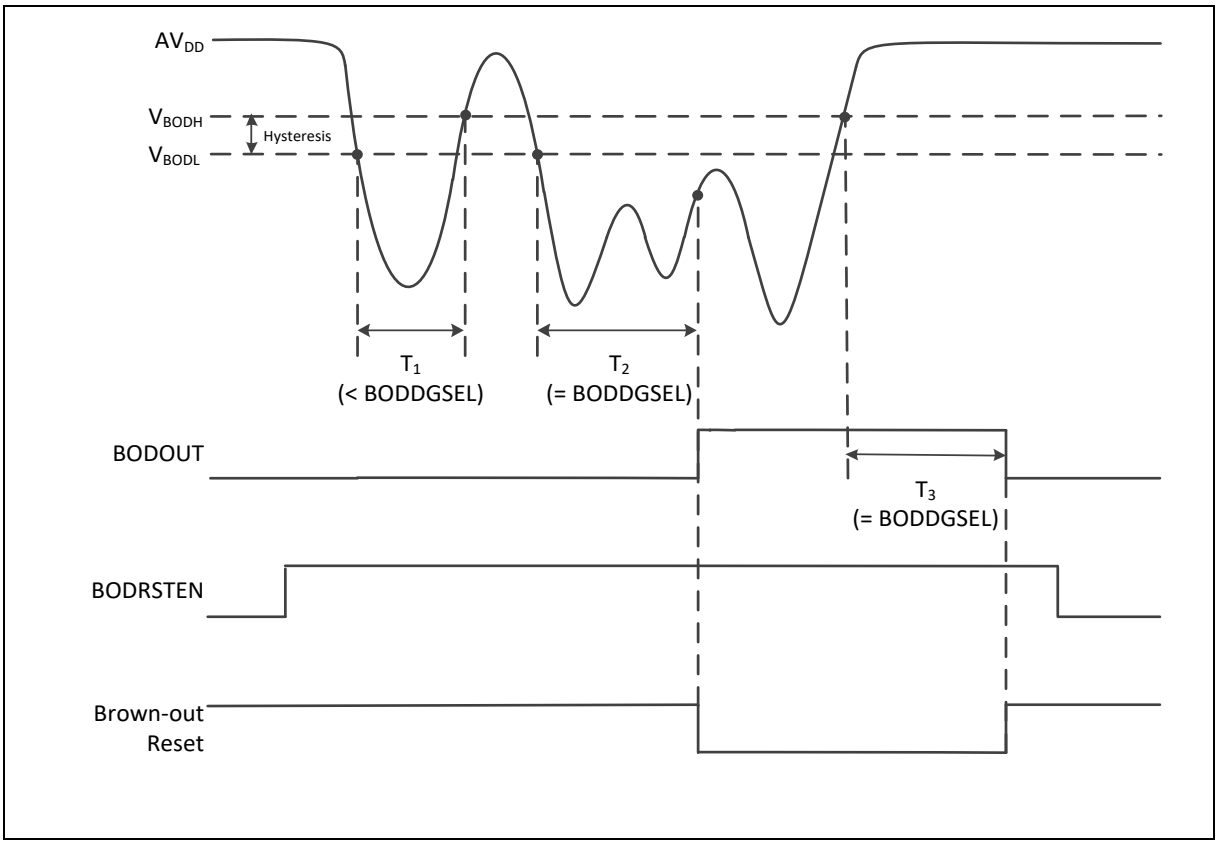


Figure 6.2-5 Brown-out Detector (BOD) Waveform

6.2.2.5 Watchdog Timer Reset (WDT)

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer(WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS_RSTSTS[2]).

6.2.2.6 CPU Lockup Reset

CPU enters lockup status after CPU produces hardfault at hardfault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an unrecoverable exception following the activation of the processor's built in system state protection

hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

6.2.2.7 CPU Reset, CHIP Reset and MCU Reset

The CPU Reset means only Cortex®-M23 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST(SYS_IPRST0[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is same with Power-on Reset. The CPU and all peripherals are reset and BS(FMC_ISPCTL[1]) bit is automatically reloaded from CONFIG0 setting. User can set the CHIPRST(SYS_IPRST0[1]) to 1 to assert the CHIP Reset signal.

The MCU Reset is similar with CHIP Reset. The difference is that BS(FMC_ISPCTL[1]) will not be reloaded from CONFIG0 setting and keep its original software setting for booting from APROM or LDROM. User can set the SYSRESETREQ(AIRCR[2]) to 1 to assert the MCU Reset.

6.2.3 Power Modes and Wake-up Sources

There are several wake-up sources in Idle mode and Power-down mode. Table 6.2-2 lists the available clocks for each power mode.

Power Mode	Normal Mode	Idle Mode	Power-Down Mode
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content retended.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	WDT, I²C, Timer, UART, BOD, GPIO, EINT, USBD and VDET.
Available Clocks	All	All except CPU clock	LXT and LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 6.2-2 Power Mode Difference Table

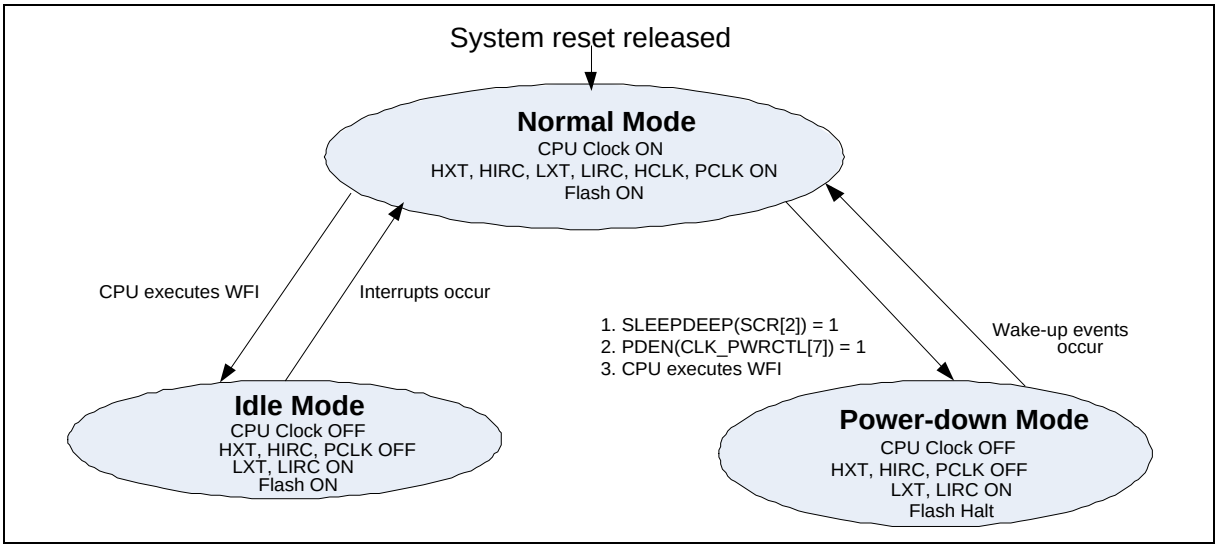


Figure 6.2-6 NuMicro® NUC1262 Power Mode State Machine

1. LXT (32768 Hz XTL) ON or OFF depends on SW setting in normal mode.
2. LIRC (10 kHz OSC) ON or OFF depends on SOFTWARE setting in normal mode.
3. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is on.
4. If WDT clock source is selected as LIRC and LIRC is on.
5. If UART clock source is selected as LXT and LXT is on.
6. FMC clock source ON or OFF depends on SOFTWARE setting in idle mode.

	Normal Mode	Idle Mode	Power-Down Mode
HXT (4~24 MHz XTL)	ON	ON	Halt
HIRC (48 MHz OSC)	ON	ON	Halt
LXT (32768 Hz XTL)	ON	ON	ON/OFF[1]
LIRC (10 kHz OSC)	ON	ON	ON/OFF[2]
PLL	ON	ON	Halt
LDO	ON	ON	ON
CPU	ON	Halt	Halt
HCLK/PCLK	ON	ON	Halt
SRAM retention	ON	ON	ON
FLASH	ON	ON/OFF[6]	Halt
GPIO	ON	ON	Halt
PDMA	ON	ON	Halt
TIMER	ON	ON	ON/OFF[3]
BPWM	ON	ON	Halt
WDT	ON	ON	ON/OFF[4]
WWDT	ON	ON	Halt
UART	ON	ON	ON/OFF[5]
I²C	ON	ON	Halt
SPI	ON	ON	Halt
USBD	ON	ON	Halt
ADC	ON	ON	Halt
LLSI	ON	ON	Halt

Table 6.2-3 Clocks in Power Modes

Wake-up sources in Power-down mode:

WDT, I²C, Timer, UART, BOD, VDET, GPIO, and USBD.

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 6.2-4 lists the condition about how to enter Power-down mode again for each peripheral.

*User needs to wait this condition before setting PDEN(CLK_PWRCTL[7]) and execute WFI to enter Power-down mode.

Wake-Up Source	Wake-Up Condition	System Can Enter Power-Down Mode Again Condition*
BOD	Brown-Out Detector Interrupt	After software writes 1 to clear BODIF (SYS_BODCTL[4]).
VDET	Voltage Detector Interrupt	After software writes 1 to clear VDETIF (SYS_BODCTL[19]).
GPIO	GPIO Interrupt	After software write 1 to clear the Px_INTSRC[n] bit.
TIMER	Timer Interrupt	After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]).

WDT	WDT Interrupt	After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect).
UART	nCTS wake-up	After software writes 1 to clear CTSWKF (UARTx_WKSTS[0]).
	RX Data wake-up	After software writes 1 to clear DATWKF (UARTx_WKSTS[1]).
	Received FIFO Threshold Wake-up	After software writes 1 to clear RFRTWKF (UARTx_WKSTS[2]).
	RS-485 AAD Mode Wake-up	After software writes 1 to clear RS485WKF (UARTx_WKSTS[3]).
	Received FIFO Threshold Time-out Wake-up	After software writes 1 to clear TOUTWKF (UARTx_WKSTS[4]).
I^2C	Address match wake-up	After software writes 1 to clear WKAKDONE (I2C_WKSTS[1]). Then software writes 1 to clear WKIF(I2C_WKSTS[0]).
USBD	Remote Wake-up	After software writes 1 to clear BUSIF (USBD_INTSTS[0]).

Table 6.2-4 Condition of Entering Power-down Mode Again

6.2.4 System Power Distribution

In this chip, power distribution is divided into four segments:

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.8 V power for digital operation and I/O pins.
- USB transceiver power from V_{BUS} offers the power for operating the USB transceiver.

The outputs of internal voltage regulators, LDO and VDD33, require an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}). Figure 6.2-7 shows the NUC1262 series power distribution.

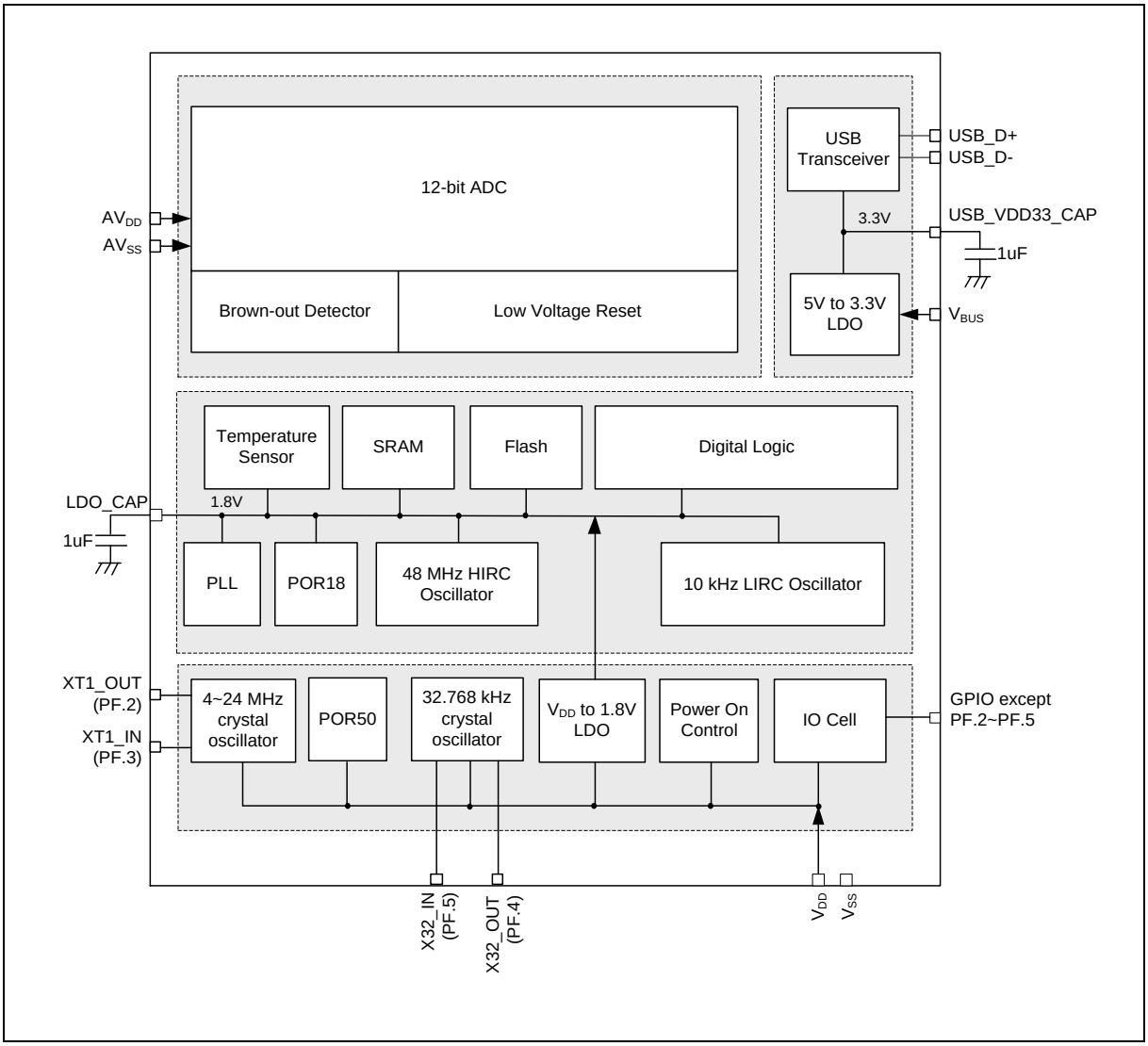


Figure 6.2-7 NuMicro® NUC1262 Power Distribution Diagram

6.2.5 System Memory Map

This chip provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.2-5. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. This chip only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0001_FFFF	FLASH_BA	Flash Memory Space (128 KB)
0x0002_0000 – 0x0005_FFFF	Reserved	Reserved
0x0006_0000 – 0x0007_FFFF	Reserved	Reserved
0x0010_0000 – 0x0010_0FFF	FMC_LDROM_BASE	Flash LDROM Memory Space (4 KB)
0x0020_0000 – 0x0020_07FF	FMC_SPROM_BASE	Flash SPROM Memory Space (2 KB)
0x2000_0000 – 0x2000_4FFF	SRAM_BA	SRAM Memory Space (20 KB)
0x2000_5000 – 0x2000_BFFF	Reserved	Reserved
0x2000_C000 – 0x2000_FFFF	Reserved	Reserved
AHB Controllers Space (0x5000_0000 – 0x501F_FFFF)		
0x5000_0000 – 0x5000_01FF	SYS_BA	System Control Registers
0x5000_0200 – 0x5000_02FF	CLK_BA	Clock Control Registers
0x5000_0300 – 0x5000_03FF	INT_BA	Interrupt Multiplexer Control Registers
0x5000_4000 – 0x5000_7FFF	GPIO_BA	GPIO Control Registers
0x5000_8000 – 0x5000_BFFF	PDMA_BA	Peripheral DMA Control Registers
0x5000_C000 – 0x5000_FFFF	FMC_BA	Flash Memory Control Registers
0x5001_0000 – 0x5001_7FFF	Reserved	Reserved
0x5001_8000 – 0x5001_FFFF	CRC_BA	CRC Generator Registers
Peripheral Controllers Space (0x4000_0000 – 0x401F_FFFF)		
0x4000_4000 – 0x4000_7FFF	WDT_BA	Watchdog Timer Control Registers
0x4000_8000 – 0x4000_BFFF	Reserved	Reserved
0x4001_0000 – 0x4001_3FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4002_0000 – 0x4002_3FFF	I2C0_BA	I2C0 Interface Control Registers
0x4003_0000 – 0x4003_3FFF	SPI0_BA	SPI0 with master/slave function Control Registers
0x4003_4000 – 0x4003_7FFF	SPI1_BA	SPI1 with master/slave function Control Registers
0x4004_0000 – 0x4004_3FFF	BPWM0_BA	BPWM0 Control Registers
0x4004_4000 – 0x4004_7FFF	BPWM2_BA	BPWM2 Control Registers
0x4005_0000 – 0x4005_3FFF	UART0_BA	UART0 Control Registers
0x4005_4000 – 0x4005_41FF	LLSI0_BA	LLSI0 Control Registers

0x4005_4200 – 0x4005_43FF	LLSI2_BA	LLSI2 Control Registers
0x4005_4400 – 0x4005_45FF	LLSI4_BA	LLSI4 Control Registers
0x4005_4600 – 0x4005_47FF	LLSI6_BA	LLSI6 Control Registers
0x4005_4800 – 0x4005_49FF	LLSI8_BA	LLSI8 Control Registers
0x4006_0000 – 0x4006_3FFF	USBD_BA	USB 2.0 FS device Controller Registers
0x400D_4000 – 0x400D_7FFF	Reserved	Reserved
0x400E_0000 – 0x400E_FFFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
0x4010_0000 – 0x4010_3FFF	Reserved	Reserved
0x4011_0000 – 0x4011_3FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4012_0000 – 0x4012_3FFF	I2C1_BA	I2C1 Interface Control Registers
0x4014_0000 – 0x4014_3FFF	BPWM1_BA	BPWM1 Control Registers
0x4014_4000 – 0x4014_7FFF	BPWM3_BA	BPWM3 Control Registers
0x4015_0000 – 0x4015_3FFF	UART1_BA	UART1 Control Registers
0x4015_4000 – 0x4015_41FF	LLSI1_BA	LLSI1 Control Registers
0x4015_4200 – 0x4015_43FF	LLSI3_BA	LLSI3 Control Registers
0x4015_4400 – 0x4015_45FF	LLSI5_BA	LLSI5 Control Registers
0x4015_4600 – 0x4015_47FF	LLSI7_BA	LLSI7 Control Registers
0x4015_4800 – 0x4015_49FF	LLSI9_BA	LLSI9 Control Registers
0x4017_4000 – 0x4017_7FFF	Reserved	Reserved
0x401A_0000 – 0x401A_3FFF	Reserved	Reserved
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6.2-5 Address Space Assignments for On-Chip Controllers

6.2.6 SRAM Memory Organization

This chip supports embedded SRAM with total 20 Kbytes size in one bank.

- Supports total 20 Kbytes SRAM
- Supports byte / half word / word write
- Supports oversize response error

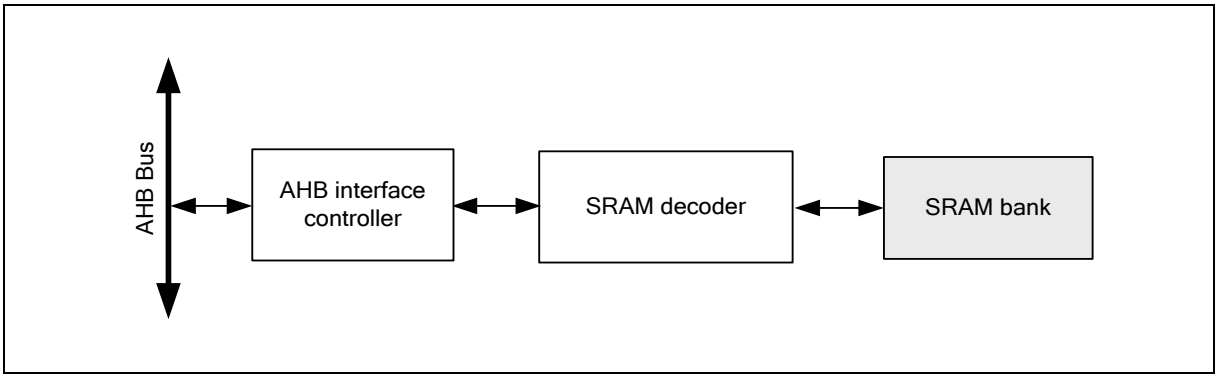


Figure 6.2-8 SRAM Block Diagram

Figure 6.2-9 shows the NUC1262 series SRAM organization. There is one SRAM bank in this chip and addressed to 20 Kbytes. The address space is from 0x2000_0000 to 0x2000_4FFF. The address between 0x2000_5000 to 0x3FFF_FFFF is illegal memory space and chip will enter hardfault if CPU accesses these illegal memory addresses.

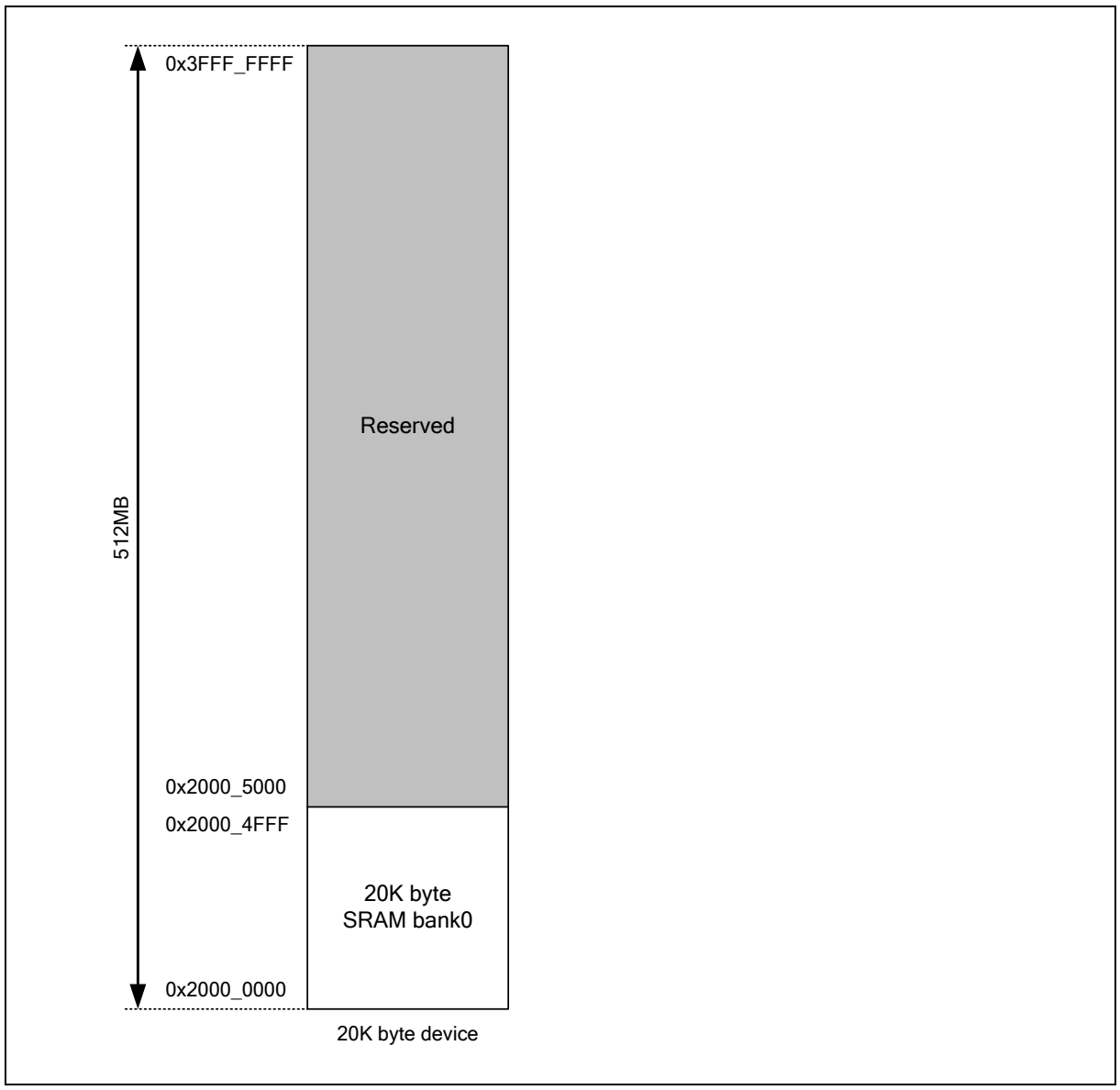


Figure 6.2-9 SRAM Memory Organization

6.2.7 Register Lock

Some of the system control registers need to be protected to avoid inadvertent write and disturb the chip operation. These system control registers are protected after the power-on reset till user to disable register protection. For user to program these protected registers, a register protection disable sequence needs to be followed by a special programming. The register protection disable sequence is writing the data “59h”, “16h” “88h” to the register SYS_REGLCTL address at 0x5000_0100 continuously. Any different data value, different sequence or any other write to other address during these three data writing will abort the whole sequence.

After the protection is disabled, user can check the protection disable bit at address 0x5000_0100 bit0, 1 is protection disable, and 0 is protection enable. Then user can update the target protected register value and then write any data to the address “0x5000_0100” to enable register protection.

6.2.8 Auto Trim

This chip supports auto-trim function: the HIRC trim (48 MHz RC oscillator), according to the accurate

LXT (32.768 kHz crystal oscillator) or USB synchronous mode, automatically gets accurate HIRC output frequency, 0.25 % deviation within all temperature ranges.

For instance, the system needs an accurate 48 MHz clock. In such case, if users do not want to use PLL as the system clock source, they need to solder 32.768 kHz crystal in system, and set FREQSEL (SYS_IRCTCTL0[1:0] trim frequency selection) to “01”, set REFCKSEL (SYS_IRCTCTL0[9] reference clock selection) to “0”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_IRCTISTS[0] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within 0.25% deviation. To get better results, it is recommended to set both LOOPSEL (SYS_IRCTCTL[5:4] trim calculation loop) and RETRYCNT (SYS_IRCTCTL[7:6] trim value update limitation count) to “11”.

Another example is that the system needs an accurate 48 MHz clock for USB application. In such case, if neither using PLL as the system clock source nor soldering 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_IRCTCTL1[10] reference clock selection) to “1”, set FREQSEL (SYS_IRCTCTL1[1:0] trim frequency selection) to “10”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK1 (SYS_IRCTISTS[8] HIRC frequency lock status) “1” indicates the HIRC1 output frequency is accurate within 0.25% deviation.

HIRC trim can only work properly when the clock sources are stable. When the RC clock or the reference clock is not stable or the system goes into power down, HIRC trim needs to wait until the clock is stable or system wakes up, and then it can be enabled or will get a clock error flag. RC trim provides a hardware function to detect the clock is stable or the system is in Power-down mode or not.

6.2.9 UART1_TXD Modulation with BPWM

This chip supports UART1_TXD to modulate with BPWM channel. User can set MODPWMSEL(SYS_MODCTL[6:4]) to choose which BPWM0 channel to modulate with UART1_TXD and set MODEN(SYS_MODCTL[0]) to enable modulation function. User can set TXDINV(UART_LINE[8]) to inverse UART1_TXD before modulating with BPWM.

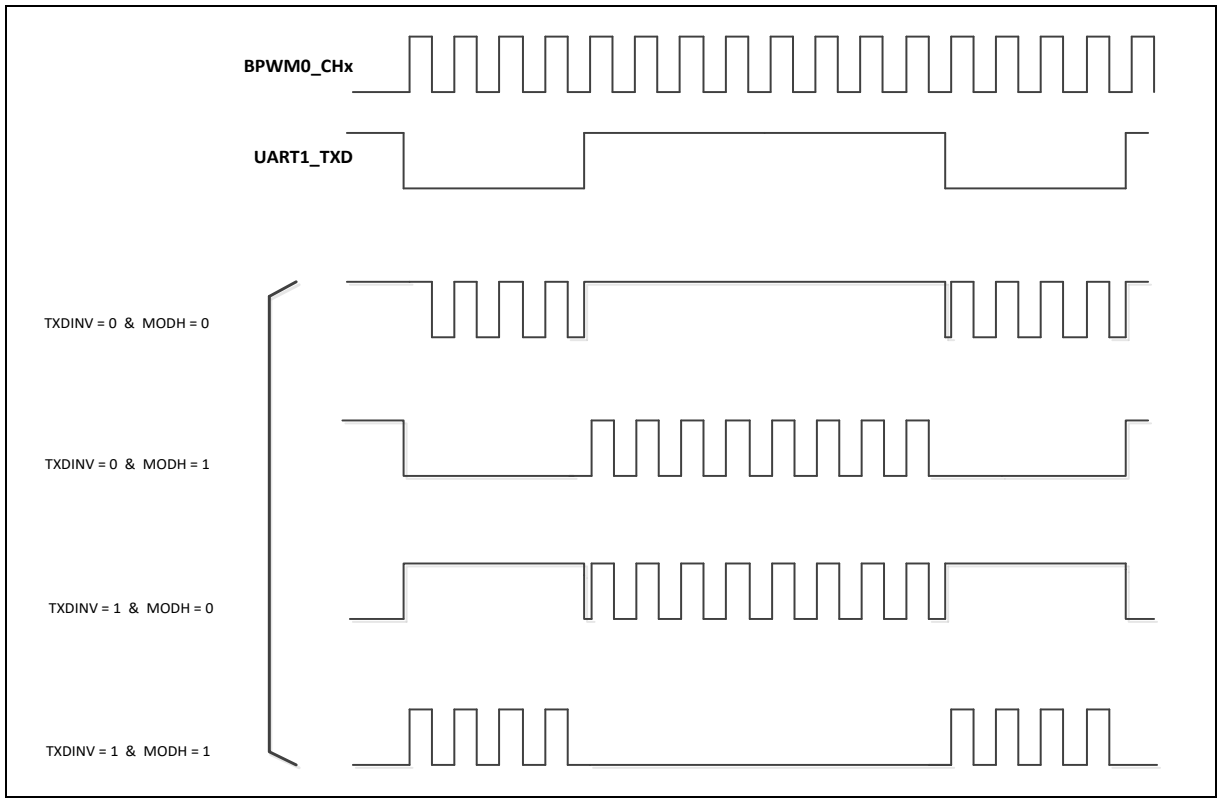


Figure 6.2-10 UART1_TXD Modulated with BPWM Channel

6.2.10 Voltage Detector (VDET)

This chip supports low power comparator to detect external voltage. User can control Band-gap active interval and comparator active interval to achieve low power detection purpose. There is no debounce function in Power-down mode since no HCLK is available in Power-down mode.

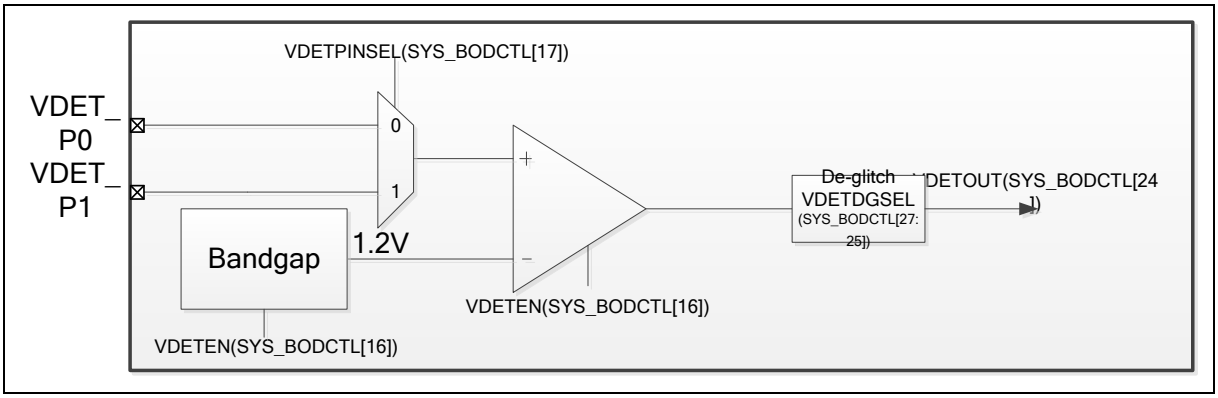


Table 6.2-6 VDET Block Diagram

6.2.11 System Timer (SysTick)

The Cortex®-M23 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to 0, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock cycle, then decrement on subsequent clocks. When the counter transitions to 0, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to 0 before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is 0, the timer will be maintained with a current value of 0 after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the "*Arm® Cortex®-M23 Technical Reference Manual*" and "*Arm® v6-M Architecture Reference Manual*".

6.2.11.1 *System Timer Control Register Map*

R: read only, **W**: write only, **R/W**: both read and write

Register	Offset	R/W	Description	Reset Value
SYST Base Address: **SCS_BA = 0xE000_E000**				
SYST_CSR	SCS_BA+0x10	R/W	SysTick Control and Status Register	0x0000_0000
SYST_RVR	SCS_BA+0x14	R/W	SysTick Reload Value Register	0xXXXX_XXXX
SYST_CVR	SCS_BA+0x18	R/W	SysTick Current Value Register	0xXXXX_XXXX

6.2.11.2 *System Timer Control Register Description*

SysTick Control and Status Register (SYST_CSR)

Register	Offset	R/W	Description	Reset Value
SYST_CSR	SCS_BA+0x10	R/W	SysTick Control and Status Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							**COUNTFLAG**
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					**CLKSRC**	**TICKINT**	**ENABLE**

Bits	Description	
[31:17]	**Reserved**	Reserved.
[16]	**COUNTFLAG**	**System Tick Counter Flag** Returns 1 if timer counted to 0 since last time this register is read. COUNTFLAG is set by a count transition from 1 to 0. COUNTFLAG is cleared on read or by a write to the Current Value register.
[15:3]	**Reserved**	Reserved.
[2]	**CLKSRC**	**System Tick Clock Source Selection** 0 = Clock source is the (optional) external reference clock. 1 = Core clock used for SysTick.
[1]	**TICKINT**	**System Tick Interrupt Enabled** 0 = Counting down to 0 does not cause the SysTick exception to be pended. Software can use COUNTFLAG to determine if a count to zero has occurred. 1 = Counting down to 0 will cause the SysTick exception to be pended. Clearing the SysTick current value register by a register write in software will not cause SysTick to be pended.
[0]	**ENABLE**	**System Tick Counter Enabled** 0 = Counter Disabled. 1 = Counter will operate in a multi-shot manner.

SysTick Reload Value Register (SYST_RVR)

Register	Offset	R/W	Description	Reset Value
SYST_RVR	SCS_BA+0x14	R/W	SysTick Reload Value Register	0xXXXX_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
RELOAD[23:16]							
15	14	13	12	11	10	9	8
RELOAD[15:8]							
7	6	5	4	3	2	1	0
RELOAD[7:0]							

Bits	Description	
[31:24]	**Reserved**	Reserved.
[23:0]	**RELOAD**	**System Tick Reload Value** Value to load into the Current Value register when the counter reaches 0.

SysTick Current Value Register (SYST_CVR)

Register	Offset	R/W	Description	Reset Value
SYST_CVR	SCS_BA+0x18	R/W	SysTick Current Value Register	0xXXXX_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
CURRENT [23:16]							
15	14	13	12	11	10	9	8
CURRENT [15:8]							
7	6	5	4	3	2	1	0
CURRENT[7:0]							

Bits	Description	
[31:24]	**Reserved**	Reserved.
[23:0]	**CURRENT**	**System Tick Current Value** Current counter value. This is the value of the counter at the time it is sampled. The counter does not provide read-modify-write protection. The register is write-clear. A software write of any value will clear the register to 0.

6.2.12 Nested Vectored Interrupt Controller (NVIC)

The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked, or nested, interrupts to enable tail-chaining of interrupts. You can only fully access the NVIC from privileged mode, but you can cause interrupts to enter a pending state in user mode if you enable the Configuration and Control Register. Any other user mode access causes a bus fault. You can access all NVIC registers using byte, halfword, and word accesses unless otherwise stated. NVIC registers are located within the SCS (System Control Space). All NVIC registers and system debug registers are little-endian regardless of the endianness state of the processor.

The NVIC supports:

- An implementation-defined number of interrupts, in the range 1-42 interrupts.
- A programmable priority level of 0-3 for each interrupt; a higher level corresponds to a lower priority, so level 0 is the highest interrupt priority.
- Level and pulse detection of interrupt signals.
- Dynamic reprioritization of interrupts.
- Grouping of priority values into group priority and subpriority fields.
- Interrupt tail-chaining.
- An external Non Maskable Interrupt (NMI)
- WIC with Ultra-low Power Sleep mode support

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead. This provides low latency exception handling.

6.2.12.1 *Exception Model and System Interrupt Map*

Table 6.2-7 lists the exception model supported by the NUC1262 series. Software can set 4 levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0x00” and the lowest priority is denoted as “0xC0” (The 6-LSB always 0). The default priority of all the user-configurable interrupts is “0x00”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

When any interrupts is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. On system reset, the vector table is fixed at address 0x00000000. Privileged software can write to the VTOR to relocate the vector table start address to a different memory location, in the range 0x00000080 to 0x3FFFFF80.

The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Exception Type	Vector Number	Vector Address	Priority
Reset	1	0x00000004	-3
NMI	2	0x00000008	-2
Hard Fault	3	0x0000000C	-1
Reserved	4~ 10		Reserved
SVCall	11	0x0000002C	Configurable
Reserved	12~13		Reserved

PendSV	14	0x00000038	Configurable
SysTick	15	0x0000003C	Configurable
Interrupt (IRQ0 ~ IRQ41)	16 ~ 57	0x00000000 + (Vector Number)*4	Configurable

Table 6.2-7 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Interrupt Description
0 ~ 15	-	-	System exceptions
16	0	BOD_INT	Brown-out low voltage detected interrupt
17	1	WDT_INT	Window Watchdog Timer interrupt
18	2	EINT024	External interrupt from INT0/INT2/INT4 pin
19	3	EINT135	External interrupt from INT1/INT3/INT5 pin
20	4	GPAB_INT	External signal interrupt from PA[3:0]/PA[11:5]/PB[15:0]
21	5	GPCDF_INT	External interrupt from PC[7:0]/PC[14]/PD[3:0]/PD[15]/PF[6:0]/PF[15:14]
22	6	BPWM0_INT	BPWM0 interrupt
23	7	BPWM1_INT	BPWM1 interrupt
24	8	TMR0_INT	Timer 0 interrupt
25	9	TMR1_INT	Timer 1 interrupt
26	10	TMR2_INT	Timer 2 interrupt
27	11	TMR3_INT	Timer 3 interrupt
28	12	UART0_INT	UART0 interrupt
29	13	UART1_INT	UART1 interrupt
30	14	SPI0_INT	SPI0 interrupt
31	15	SPI1_INT	SPI1 interrupt
32	16	BPWM2_INT	BPWM2 interrupt
33	17	BPWM3_INT	BPWM3 interrupt
34	18	I2C0_INT	I2C0 interrupt
35	19	I2C1_INT	I2C1 interrupt
36	20		Reserved
37	21		Reserved
38	22		Reserved
39	23	USBD_INT	USB Device interrupt
40	24		Reserved
41	25		Reserved

42	26	PDMA_INT	PDMA interrupt
43	27		Reserved
44	28	PWRWU_INT	Clock controller interrupt for chip wake-up from Power-down state
45	29	ADC_INT	ADC interrupt
46	30	CLKDIRC_INT	Clock fail detect and IRC TRIM interrupt
47	31		Reserved
48	32	LLSI0_INT	LED Lighting Strip Interface 0 interrupt
49	33	LLSI1_INT	LED Lighting Strip Interface 1 interrupt
50	34	LLSI2_INT	LED Lighting Strip Interface 2 interrupt
51	35	LLSI3_INT	LED Lighting Strip Interface 3 interrupt
52	36	LLSI4_INT	LED Lighting Strip Interface 4 interrupt
53	37	LLSI5_INT	LED Lighting Strip Interface 5 interrupt
54	38	LLSI6_INT	LED Lighting Strip Interface 6 interrupt
55	39	LLSI7_INT	LED Lighting Strip Interface 7 interrupt
56	40	LLSI8_INT	LED Lighting Strip Interface 8 interrupt
57	41	LLSI9_INT	LED Lighting Strip Interface 9 interrupt

Table 6.2-8 Interrupt Number Table

6.2.12.2 *Operation Description*

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in the next section.

6.2.13 System Control

The Cortex®-M23 status and operating mode control are managed by System Control Registers. Including CPUID, Cortex®-M23 interrupt priority and Cortex®-M23 power management can be controlled through these system control registers.

For more detailed information, please refer to the "*Arm® Cortex®-M23 Technical Reference Manual*" and "*Arm® v8-M Architecture Reference Manual*".

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(CLK_PWRCTL[7]) and Cortex®-M23 core executes the WFI instruction. After that, chip enters Power-down mode and waits for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT) and 48 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. Figure 6.3-1 shows the clock generator and the overview of the clock source control.

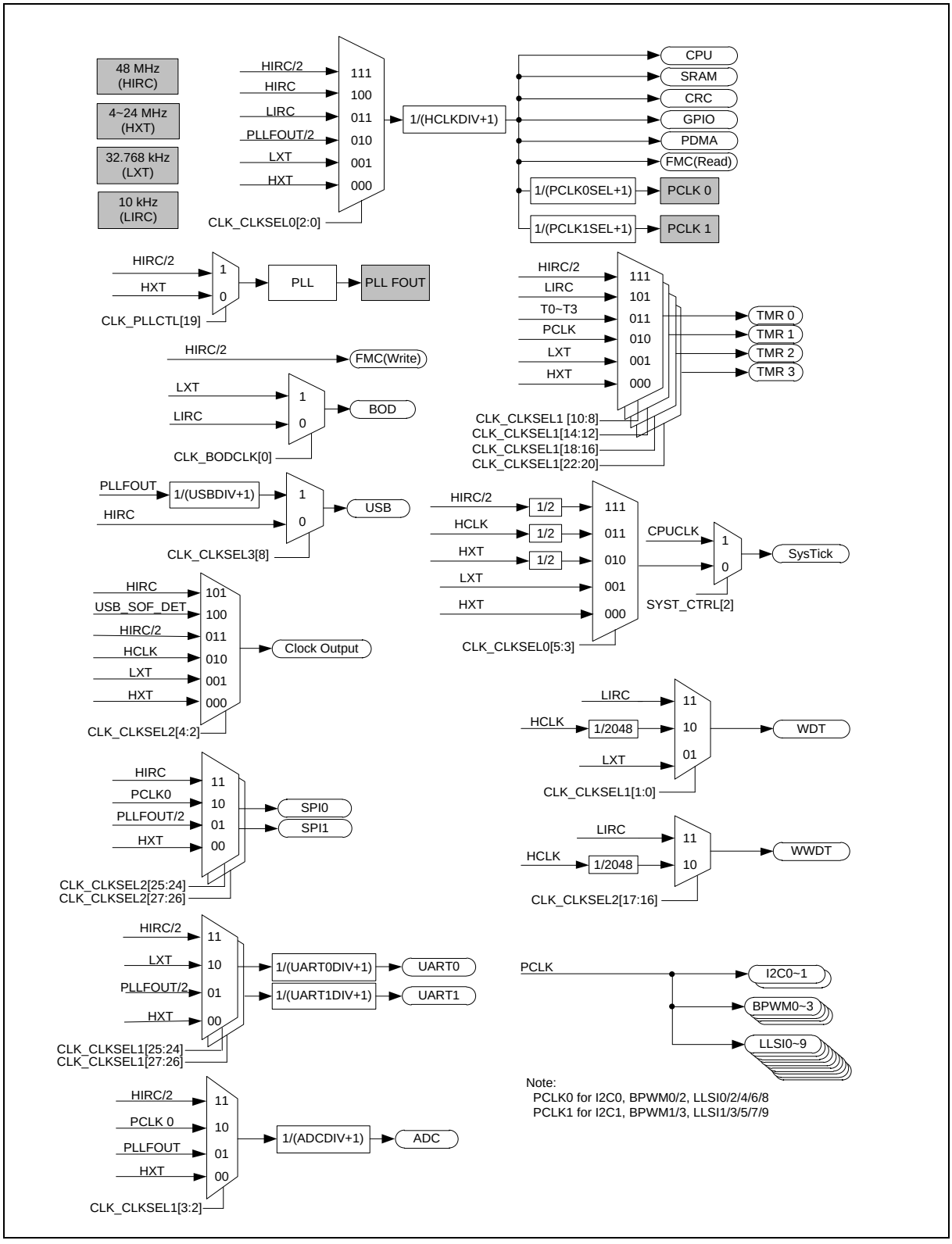


Figure 6.3-1 Clock Generator Global View Diagram

6.3.2 Clock Generator

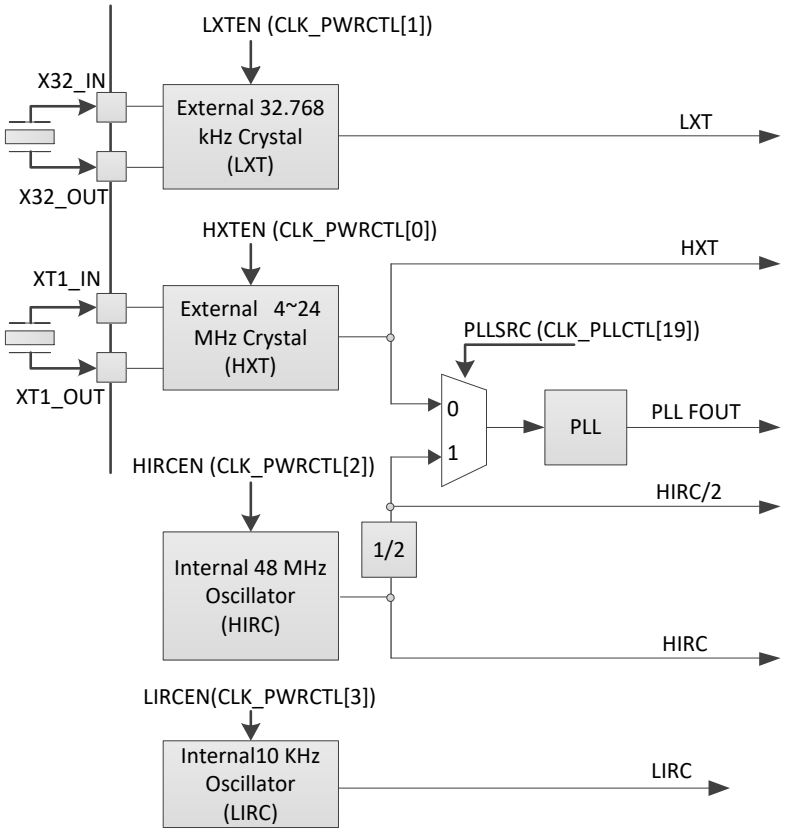
The clock generator consists of 5 clock sources, which are listed below:

- 32.768 kHz external low-speed crystal oscillator (LXT)
- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLLFOUT), PLL source can be selected from external 4~24 MHz external high speed crystal (HXT) or 48 MHz internal high speed oscillator divided by 2 (HIRC/2)
- 48 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

Each of these clock sources has certain stable time to wait for clock operating at stable frequency. When clock source is enabled, a stable counter starts counting and correlated clock stable index (HIRCSTB(CLK_STATUS[4]), LIRCSTB(CLK_STATUS[3]), PLLSTB(CLK_STATUS[2]), LXTSTB(CLK_STATUS[1]) and HXTSTB(CLK_STATUS[0]) are set to 1 after stable counter value reaches a define value as shown in Table 6.3-1. System and peripheral can use the clock as its operating clock only when correlate clock stable index is set to 1. The clock stable index will automatically cleared when user disables the clock source (LIRCEN(CLK_PWRCTL[3]), HIRCEN(CLK_PWRCTL[2]), HXTEN(CLK_PWRCTL[0]), PD(CLK_PLLCTL[16]) and LXTEN(CLK_PWRCTL[1])). Besides, the clock stable index of HXT, HIRC and PLL will be automatically cleared when chip enters power-down and clock stable counter will re-count after chip wake-up if correlate clock is enabled.

Clock Source	Clock Stable Count Value	Clock Stable Time
HXT	4096 HXT clock	341.33 uS for 12 MHz
PLL	It's based on the value of STBSEL (CLK_PLLCTL[23]) STBSEL = 0, stable count is 6144 clocks of PLL clock source. STBSEL = 1, stable count is 12288 clocks of PLL clock source. (Default)	STBSEL = 0, 512 uS for 12 MHz STBSEL = 1, 1024 uS for 12 MHz
HIRC	512 HIRC clock	10.67 uS for 48 MHz
LIRC	1 LIRC clock	100 uS for 10 kHz
LXT	16384 LXT clock	500mS for 32.768 kHz

Table 6.3-1 Clock Stable Count Value Table

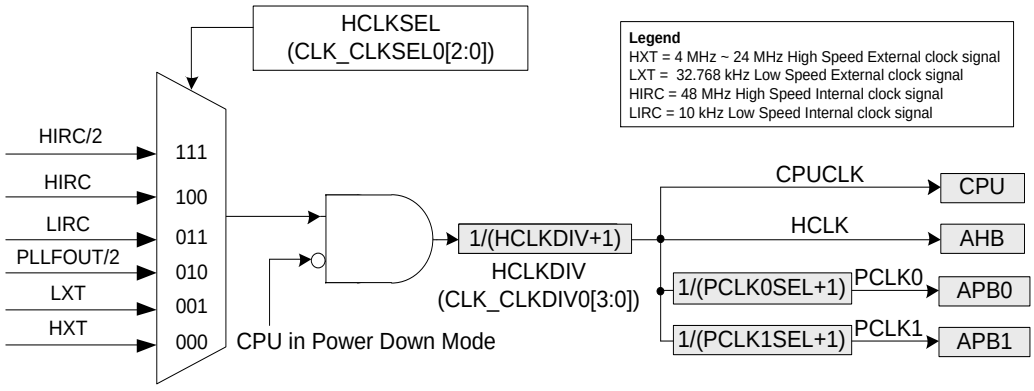


Note: Before clock switching, both the pre-selected and newly selected clock source must be turned on and stable.

Figure 6.3-2 Clock Generator Block Diagram

6.3.3 System Clock and SysTick Clock

The system clock has 6 clock sources, which were generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0 [2:0]). The block diagram is shown in Figure 6.3-3.



Note: Before clock switching, both the pre-selected and newly selected clock source must be turned on and stable.

Figure 6.3-3 System Clock Block Diagram

There are two clock fail detectors to observe HXT and LXT clock source and they have individual enable and interrupt control. When HXT detector is enabled, the HIRC clock is enabled automatically. When LXT detector is enabled, the LIRC clock is enabled automatically.

When HXT clock detector is enabled, the system clock will automatically switch to HIRC/2 if HXT clock stop being detected on the following condition: system clock source comes from HXT or system clock source comes from PLL with HXT as the input of PLL. If HXT clock stop condition is detected, the HXTFIF (CLK_CLKDSTS[0]) is set to 1 and chip will enter interrupt if HXTFIEN (CLK_CLKDCTL[5]) is set to 1. HXT clock source stable flag, HXTSTB (CLK_STATUS[0]), will be cleared if HXT stops when using HXT fail detector function. User can try to recover HXT by disabling HXT and enabling HXT again to check if the clock stable bit is set to 1 or not. If HXT clock stable bit is set to 1, it means HXT is recovered to oscillate after re-enable action and user can switch system clock to HXT again.

When LXT clock detector is enabled, the system clock will automatically switch to LIRC if LXT clock stops being detected on the following condition: system clock source comes from LXT. If LXT clock stop condition is detected, the LXTFIF (CLK_CLKDSTS[1]) is set to 1 and chip will enter interrupt if LXTFIE (CLK_CLKDCTL[5]) is set to 1. LXT clock source stable flag, LXTSTB (CLK_STATUS[1]), will be cleared if LXT stops when using LXT fail detector function. User can try to recover LXT by disabling LXT and enabling LXT again to check if the clock stable bit is set to 1 or not. If LXT clock stable bit is set to 1, it means LXT is recovered to oscillate after re-enable action and user can switch system clock to LXT again.

The HXT clock stop detect and system clock switch to HIRC/2 procedure is shown in Figure 6.3-4.

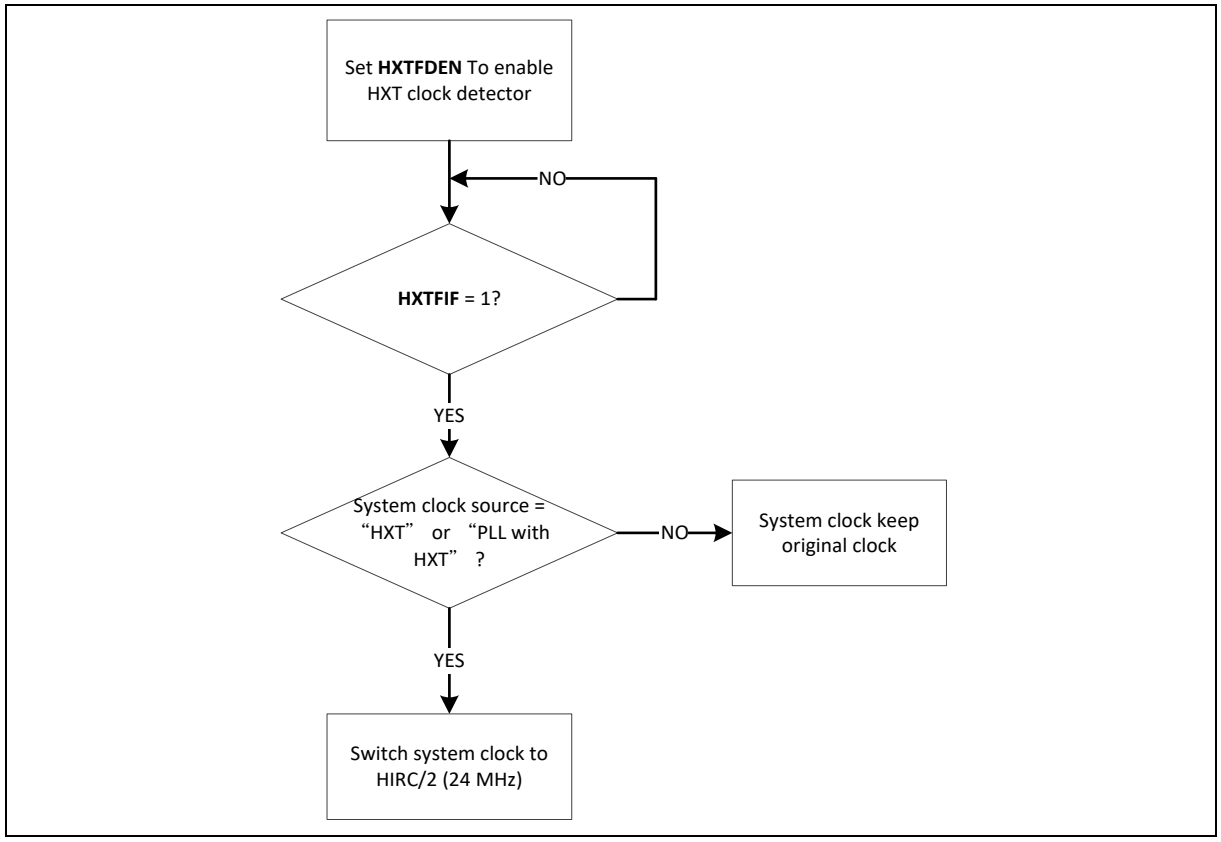


Figure 6.3-4 HXT Stop Protect Procedure

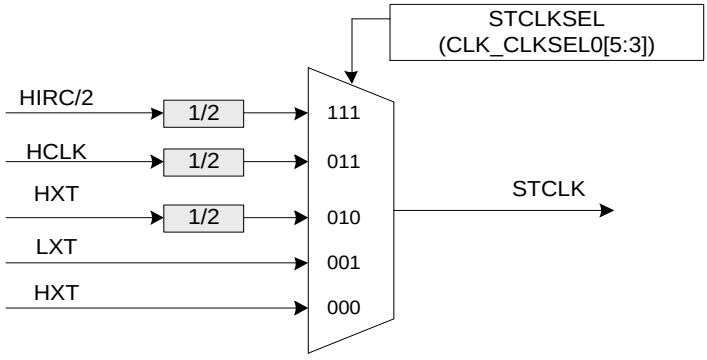
Besides, user can also monitor HXT CLK frequency range by HIRC clock. User can set UPERBD (CLK_CDUPB[9:0]) and LOWERBD (CLK_CDLOWB[9:0]) to decide monitoring frequency window. If target clock speed is greater than UPERBD or less than LOWERBD, the HXT Clock Frequency Range Detector Interrupt Flag HXTFQIF(CLK_CLKDSTS[8]) will be set to 1.

The formula of UPERBD and LOWERBD is listed below.

HIRC_period* 1024 < HXT_period* UPERBD

HIRC_period* 1024 > HXT_period* LOWERBD

The clock source of SysTick in Cortex®-M23 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in Figure 6.3-5.



Note: Before clock switching, both the pre-selected and newly selected clock source must be turned on and stable.

Figure 6.3-5 SysTick Clock Control Block Diagram

6.3.4 Peripherals Clock

The peripherals clock had different clock source switch setting, which depends on the different peripheral. Please refer to the CLK_CLKSEL1, CLK_CLKSEL2 and CLK_CLKSEL3 description in Register Description section.

6.3.5 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources, and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

The clocks, which still keep active, are listed below:

- Clock Generator
  - 10 kHz internal low-speed RC oscillator (LIRC) clock
  - 32.768 kHz external low-speed crystal oscillator (LXT) clock
- Peripherals Clock (When the modules adopt LXT or LIRC as clock source)

6.3.6 Clock Output

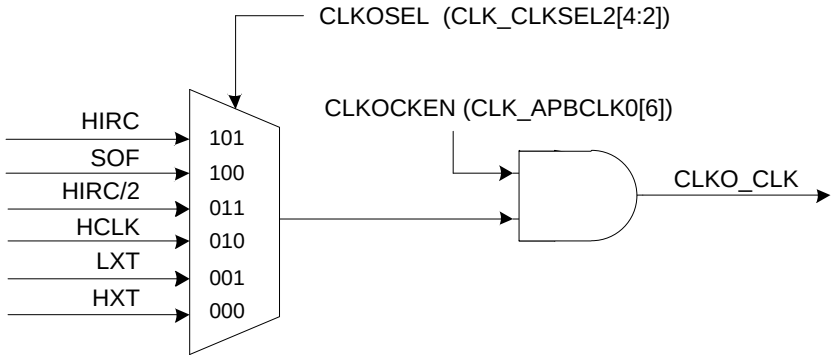
This device is equipped with a power-of-2 frequency divider composed by 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]).

When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stays in low state.

If DIVI1EN(CLK_CLKOCTL[5]) is set to 1, the clock output clock (CLKO_CLK) will bypass power-of-2 frequency divider. The clock output clock will be output to CLKO pin directly.

When entering Power-down mode, clock output does not output clock even if the CKO clock source is LXT.



Note: Before clock switching, both the pre-selected and newly selected clock source must be turned on and stable.

Figure 6.3-6 Clock Source of Clock Output

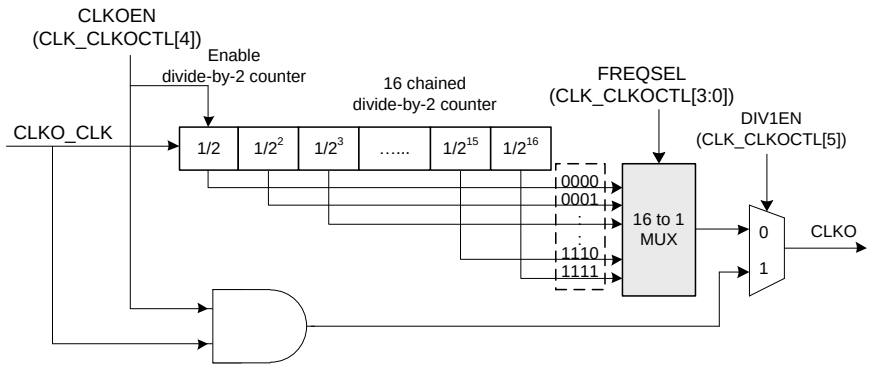


Figure 6.3-7 Clock Output Block Diagram

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

This chip is equipped with 128 Kbytes on-chip embedded Flash for application and configurable Data Flash to store some application dependent data. A User Configuration block provides for system initiation. A 4 Kbytes loader ROM (LDROM) is used for In-System-Programming (ISP) function. A 2 Kbytes security protection ROM (SPROM) can conceal user program. A 4 Kbytes cache with zero wait cycle is used to improve Flash access performance. This chip also supports In-Application-Programming (IAP) function, user switches the code executing without the chip reset after the embedded Flash updated.

6.4.2 Features

- Supports 128 Kbytes application ROM (APROM).
- Supports 4 Kbytes loader ROM (LDROM).
- Supports 2 Kbytes security protection ROM (SPROM) to conceal user program.
- Supports Data Flash with configurable memory size.
- Supports 12 bytes User Configuration block to control system initiation.
- Supports 2 Kbytes page erase for all embedded Flash.
- Supports 32-bit/64-bit and multi-word Flash programming function.
- Supports CRC-32 checksum calculation function.
- Supports Flash all one verification function.
- Supports embedded SRAM remap to system vector memory.
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded Flash memory.
- Supports cache memory to improve Flash access performance and reduce power consumption.

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

This chip has up to 50 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 50 pins are arranged in 5 ports named as PA, PB, PC, PD and PF. PA has 11 pins on port. PB has 16 pins on port. PC has 9 pins on port. PD has 5 pins on port. PF has 9 pins on port. Each of the 50 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins are depending on CIOIN (CONFIG0[10]).

6.5.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports High Drive and High Slew Rate I/O mode
- Configurable default I/O mode of all pins after reset by CIOINI (CONFIG0[10]) setting
  - CIOIN = 0, all GPIO pins in input tri-state mode after chip reset
  - CIOIN = 1, all GPIO pins in Quasi-bidirectional mode after chip reset
- Supports independent pull-up control
- Enabling the pin interrupt function will also enable the wake-up function

6.6 PDMA Controller (PDMA)

6.6.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. The PDMA controller has a total of 5 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

6.6.2 Features

- Supports 5 independently configurable channels
- Supports selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Request source can be from software,PSIO , SPI/I^{2}S, UART, USCI, EADC,DAC,PWM capture event and TIMER
- Supports Scatter-gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports time-out function on channel 0 and channel1

6.7 Timer Controller (TMR)

6.7.1 Overview

The timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.7.2 Features

- Four sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter
- Supports internal capture triggered while LIRC transition
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Supports Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger ADC, PDMA, BPWM function
- Supports Inter-Timer trigger mode

6.8 Watchdog Timer (WDT)

6.8.1 Overview

The Watchdog Timer (WDT) is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, the Watchdog Timer supports the function to wake up system from Idle/Power-down mode.

6.8.2 Features

- Supports 18-bit free running up counter
- Selectable time-out interval (2^4 ~ 2^{18}) and the time-out interval is 1.6 ms ~ 26.214s if WDT_CLK is 10 kHz
- Supports selectable WDT reset delay period between WDT time-out event to WDT reset system event, and it includes 1026, 130, 18 or 3 * WDT_CLK delay period
- System kept in reset state about 63 * WDT_CLK period time after system reset event occurred
- Supports to force WDT function enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as LIRC or LXT

6.9 Window Watchdog Timer (WWDT)

6.9.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset while WWDT counter is not reloaded within a specified window period when application program runs to uncontrollable status by any unpredictable condition.

6.9.2 Features

- Supports 6-bit down counter value CNTDAT (WWDT_CNT[5:0]) and maximum 6-bit compare value CMPDAT (WWDT_CTL[21:16]) to adjust the WWDT compare time-out window period flexibly
- Supports PSCSEL (WWDT_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode
- WWDT counter only can be reloaded within the valid window period to prevent system reset

6.10 Basic PWM Generator and Capture Timer (BPWM)

6.10.1 Overview

The chip provides four BPWM generators — BPWM0, BPWM1, BPWM2 and BPWM3 as shown in n BPWM Generator Overview Block Diagram. Each BPWM supports 6 channels of BPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit BPWM counter with 16-bit comparator. The BPWM counter supports up, down and up-down counter types, all 6 channels share one counter. BPWM uses the comparator compared with counter to generate events. These events are used to generate BPWM pulse, interrupt and trigger signal for ADC to start conversion. For BPWM output control unit, it supports polarity output, independent pin mask and tri-state output enable.

The BPWM generator also supports input capture function to latch BPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened.

6.10.2 Features

6.10.2.1 BPWM Function Features

- Supports maximum clock frequency up to 72 MHz frequency.
- Supports up to four BPWM modules; each module provides 6 output channels
- Supports independent mode for BPWM output/Capture input channel
- Supports 12-bit prescalar from 1 to 4096
- Supports 16-bit resolution BPWM counter; each module provides 1 BPWM counter
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each BPWM pin
- Supports interrupt in the following events:
  - BPWM counter matches 0, period value or compared value
- Supports trigger ADC in the following events:
  - BPWM counter matches 0, period value or compared value

6.10.2.2 Capture Function Features

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

6.11 UART Interface Controller (UART)

6.11.1 Overview

This chip provides two channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs serial-to-parallel conversion on data received from the peripheral and parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports nine types of interrupts. The UART controller supports flow control function. The UART controller also supports IrDA SIR and RS-485 function modes and auto-baud rate measuring function.

6.11.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16 bytes entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART_TOUT [15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - 3/16 bit duration for normal mode
- Supports RS-485 function mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Supports PDMA transfer function

6.12 Serial Peripheral Interface (SPI)

6.12.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. This chip contains up to two sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each SPI controller can be configured as a master or a slave device.

This controller also supports the PDMA function to access the data buffer. The SPI controller also support I^2S mode to connect external audio CODEC.

6.12.2 Features

- SPI Mode
  - Up to two sets of SPI controllers
  - Supports Master or Slave mode operation
  - Configurable bit length of a transaction word from 8 to 32-bit
  - Provides separate 4-level depth transmit and receive FIFO buffers
  - Supports MSB first or LSB first transfer sequence
  - Supports Byte Reorder function
  - Supports PDMA transfer
  - Supports one data channel half-duplex transfer
  - Supports receive-only mode
- I^2S Mode
  - Supports Master or Slave
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Provides separate 4-level depth transmit and receive FIFO buffers
  - Supports monaural and stereo audio data
  - Supports PCM mode A, PCM mode B, I^2S and MSB justified data format
  - Supports PDMA transfer

6.13 I²C Serial Interface Controller (I²C)

6.13.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are two sets of I²C controllers that support Power-down wake-up function.

6.13.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports up to two I²C ports
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflow
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing and 10-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Supports PDMA with one buffer capability
- Supports setup/hold time programmable
- Supports Bus Management (SM/PM compatible) function

6.14 USB 2.0 Full-Speed Device Controller (USBD)

6.14.1 Overview

There is USB 2.0 full-speed device controller. It is compliant with USB 2.0 full-speed device specification and supports control/bulk/interrupt/isochronous transfer types.

In this device controller, there are two main interfaces: APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 512 bytes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SI.E. User needs to set the effective starting address of SRAM for each endpoint buffer through buffer segmentation register (USBD_BUFSEGx).

There are 8 endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of “Endpoint Control” is also used to manage the data sequential synchronization, endpoint states, current start address, transaction status, and data buffer status for each endpoint.

There are five different interrupt events in this controller. They are no-event-wake-up, device plug-in or plug-out event, USB events, such as IN ACK, OUT ACK, etc., and BUS events, such as suspend and resume, etc. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USBD_INTSTS) to acknowledge what kind of interrupt occurred, and then check the related USB Endpoint Status Register (USBD_EPSTS) to acknowledge what kind of event occurred in this endpoint.

A software-disconnect function is supported for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables SE0 bit (USBD_SE0[0]), the USB controller will force the output of USB_D+ and USB_D- to level low and its function is disabled. After disabling the SE0 bit, the host will enumerate the USB device again.

For more information on the Universal Serial Bus, please refer to *Universal Serial Bus Specification Revision 1.1.*

6.14.2 Features

- Compliant with USB 2.0 Full-Speed specification
- Provides 1 interrupt vector with 5 different interrupt events (SOF, NEVWK, VBUSDET, USB and BUS)
- Supports Control/Bulk/Interrupt/Isochronous transfer type
- Supports suspend function when no bus activity existing for 3 ms
- Supports 8 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 512 bytes buffer size
- Provides remote wake-up capability

6.15 CRC Controller (CRC)

6.15.1 Overview

The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32 settings.

6.15.2 Features

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-8: $X^8 + X^2 + X + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Programmable seed value
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1's complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports using PDMA to program DATA (CRC_DAT[31:0]) to perform CRC operation

6.16 LED Lighting Strip Interface (LLSI)

6.16.1 Overview

The LLSI is a RGB LED strip controller that can convert the RGB data for hundreds of LEDs per strip into T0 and T1 code output. There are ten sets of LLSI that can be used.

6.16.2 Features

- 10 sets of LLSI channels with IDLE polarity control
- Each LLSI has 4x32-bit TX FIFO
- Configurable transfer period and frame reset length
- Configurable T0H and T1H duty cycle
- Supports RGB and GRB output format
- Supports Software mode and PDMA base mode transfer

6.17 Analog-to-Digital Converter (ADC)

6.17.1 Overview

This chip contains one 12-bit successive approximation analog-to-digital converter (SAR A/D converter) with eight input channels. The A/D converter supports four operation modes: Single, Burst, Single-cycle Scan and Continuous Scan mode. The A/D converter can be started by software, external pin STADC (PC.1/PF.5), timer0~3 overflow pulse trigger and BPWM trigger.

6.17.2 Features

- Analog input voltage range: 0 ~ AV_{DD}.
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 8 single-end analog input channels or differential analog input channels
- Maximum ADC peripheral clock frequency is 16 MHz
- Up to 800 KSPS sampling rate
- Configurable ADC internal sampling time
- Four operation modes:
  - Single mode: A/D conversion is performed one time on a specified channel.
  - Burst mode: A/D converter samples and converts the specified single channel and sequentially stores the result in FIFO.
  - Single-cycle Scan mode: A/D conversion is performed only one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel.
  - Continuous Scan mode: A/D converter continuously performs Single-cycle Scan mode until software stops A/D conversion.
- An A/D conversion can be started by:
  - Software Write 1 to ADST bit
  - External pin (STADC)
  - Timer 0~3 overflow pulse trigger
  - BPWM trigger with optional start delay period
- Each conversion result is held in data register of each channel with valid and overrun indicators.
- Conversion result can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting.
- Two internal channels, band-gap voltage (V_{BG}) and temperature sensor (V_{TEMP}).
- Supports PDMA transfer mode.

Note1: ADC sampling rate = (ADC peripheral clock frequency) / (total ADC conversion cycle)

Note2: If the internal channel (V_{TEMP}) is selected to convert, the sampling rate needs to be less than 300 KSPS for accurate result.

Note3: If the internal channel for band-gap voltage is active, the maximum sampling rate will be 300 KSPS.

7 APPLICATION CIRCUIT

7.1 Power Supply Scheme

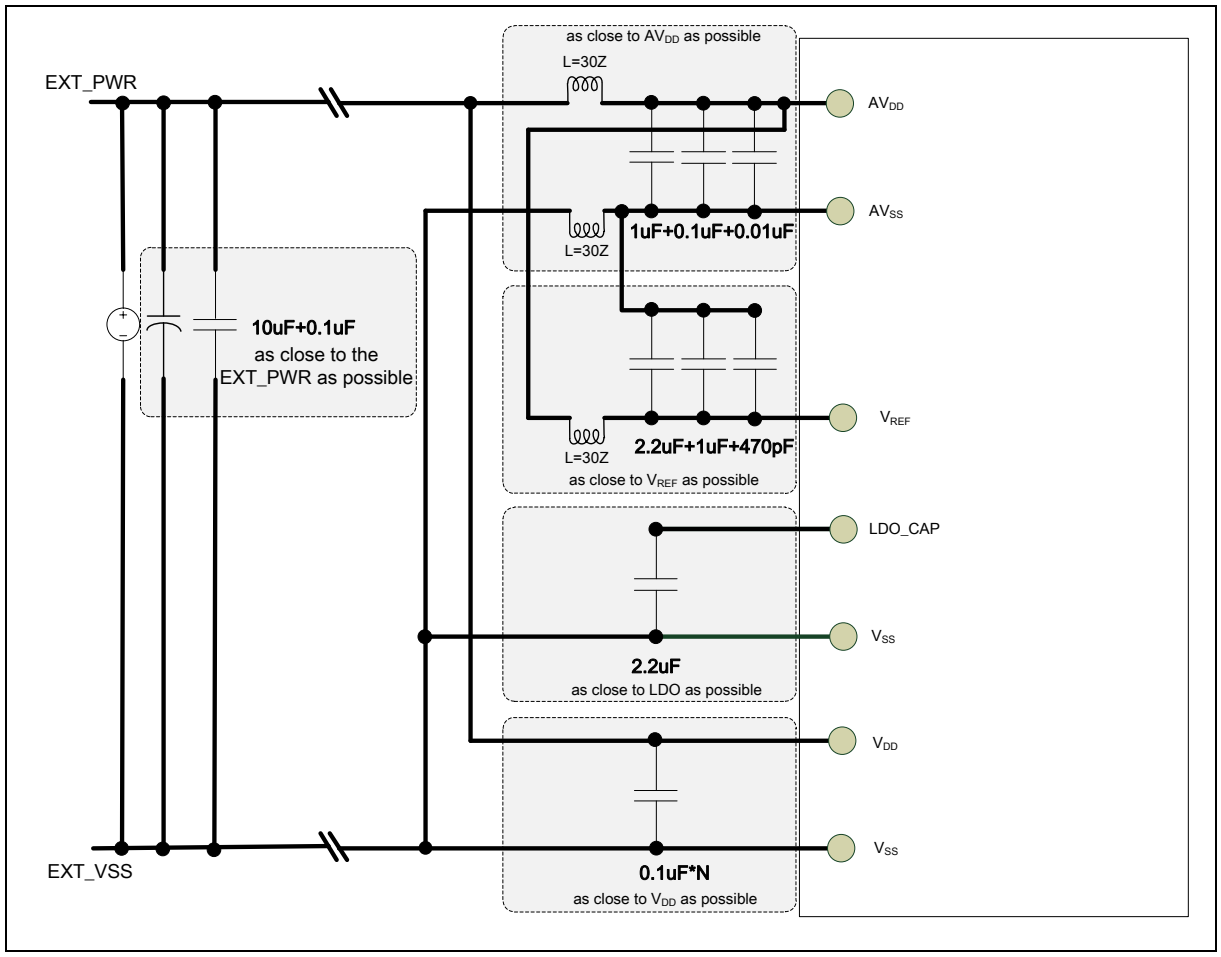
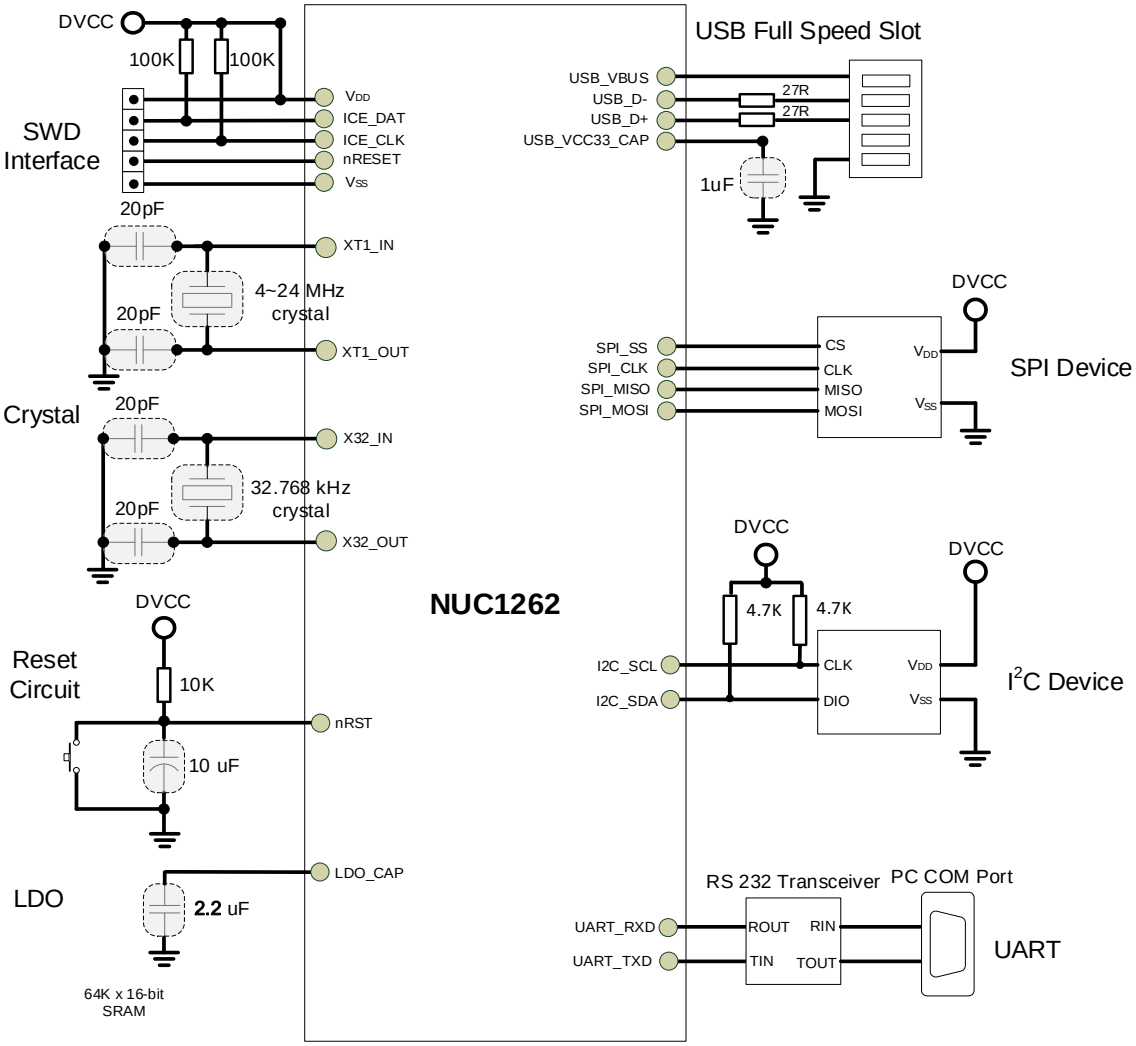


Figure 7.1-1 Power supply scheme

7.2 Peripheral Application Scheme



Note 1: It is recommended to use 100 kΩ pull-up resistor on both ICE_DAT and ICE_CLK pin

Note 2: It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.

Figure 7.2-1 Peripheral application scheme

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Stresses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

8.1.1 Absolute Maximum Ratings

Symbol	PARAMETER	MIN	MAX	UNIT
DC Power Supply	V_{DD}-V_{SS}	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS} – 0.3	V_{DD} + 0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	T_A	-40	+105	°C
Storage Temperature	T_{ST}	-55	+150	°C
Maximum Current into V_{DD}	I_{DD}	-	120	mA
Maximum Current out of V_{SS}	I_{SS}	-	120	mA
Maximum Current sunk by a I/O Pin	I_{IO}	-	35	mA
Maximum Current Sourced by a I/O Pin		-	35	mA
Maximum Current Sunk by Total I/O Pins		-	100	mA
Maximum Current Sourced by Total I/O Pins		-	100	mA

Table 8.1-1 Absolute Maximum Ratings

8.1.2 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA})$

T_A = ambient temperature (°C)

θ_{JA} = thermal resistance junction-ambient (°C/Watt)

P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	105	°C
T_J	Operating junction temperature	-40	-	125	
T_{ST}	Storage temperature	-65	-	150	
	Thermal resistance junction-ambient 48-pin QFN(7x7 mm)	-	30.9	-	°C/Watt
	Thermal resistance junction-ambient 48-pin LQFP(7x7 mm)	-	60	-	°C/Watt
	Thermal resistance junction-ambient 64-pin LQFP(7x7 mm)	-	58	-	°C/Watt

Note:

1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions

Table 8.1-2 Thermal Characteristics

8.1.3 EMC Characteristics

8.1.3.1 *Electrostatic discharge (ESD)*

For the Nuvoton MCU products, there are ESD protection circuits built into chips to avoid any damage that can be caused by typical levels of ESD.

8.1.3.2 *Static latchup*

Two complementary static tests are required on six parts to assess the latchup performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

8.1.3.3 *Electrical Fast Transients (EFT)*

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system..

- Inductive loads:

  Relays, switch contactors

  Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International ElectrotechnicalCommission (IEC).

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[*1]	Electrostatic discharge,human body mode	-7000	-	+7000	V
V_{CDM}[*2]	Electrostatic discharge,charge device model	-750	-	+750	
V_{MM}	Electrostatic discharge,machine model	-300	-	+300	
LU[*3]	Pin current for latch-up[*3]	-100 Class II	-	+100 Class II	mA
V_{EFT}[*4] [*5]	Fast transient voltage burst	-4.4	-	+4.4	kV

Notes:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test.
5. The performace cretia class is 4A.

Table 8.1-3 EMC Characteristics

8.1.4 Package Moisture Sensitivity(MSL)

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing.

Pacakge	MSL
48-pin QFN(7x7 mm) [*1]	MSL 3
48-pin LQFP(7x7 mm) [*1]	MSL 3
64-pin LQFP(7x7 mm) [*1]	MSL 3
Note: Determined according to IPC/JEDEC J-STD-020	

Table 8.1-4 Package Moisture Sensitivity (MSL)

8.1.5 Soldering Profile

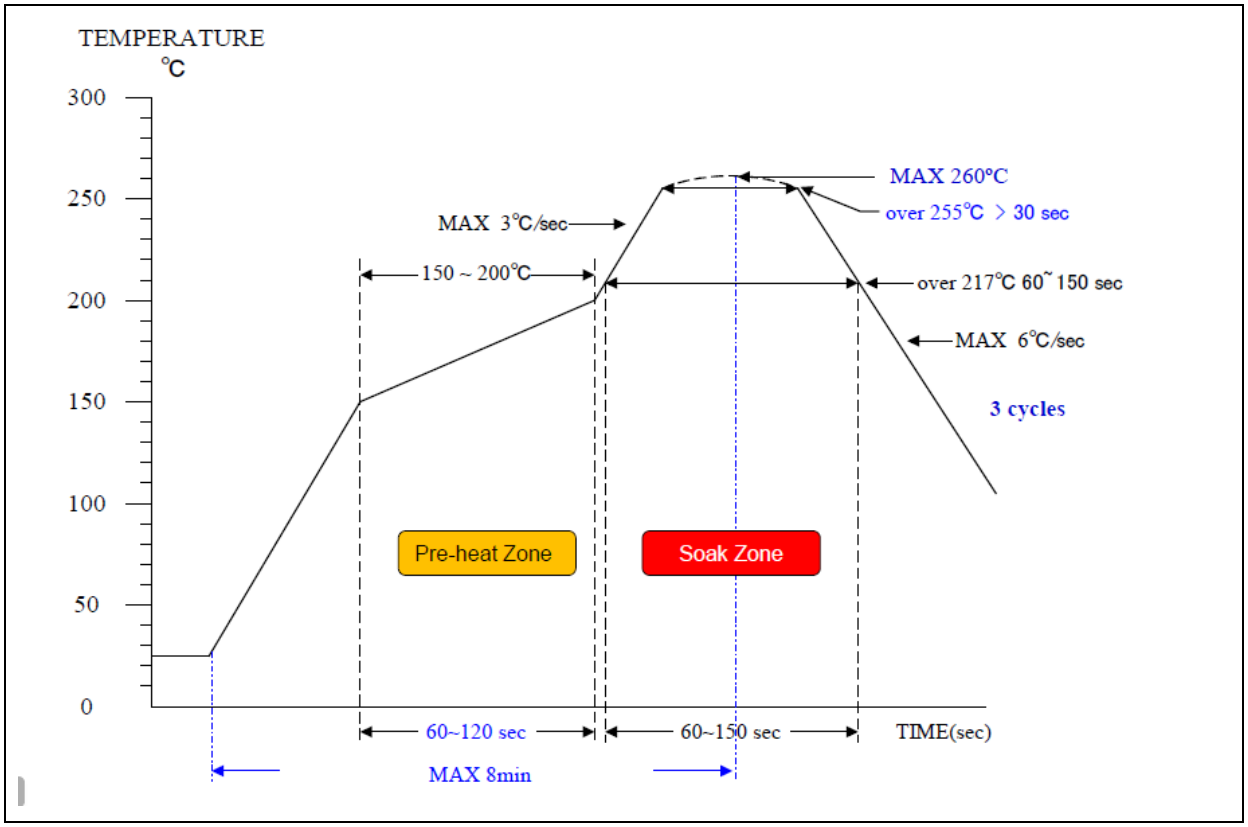


Figure 8.1-1 Soldering profile from J-STD-020C

Porfile Feature	Pb Free Package
Average ramp-up rate (217°C to peak)	3°C/sec. max
Preheat temperature 150°C ~200°C	60 sec. to 120 sec.
Temperature maintained above 217°C	60 sec. to 150 sec.
Time with 5°C of actual peak temperature	> 30 sec.

Porfile Feature	Pb Free Package
Peak temperature range	260°C
Ramp-down rate	6°C/sec ax.
Time 25°C to peak temperature	8 min. max

Note:

1. Determined according to J-STD-020C

Table 8.1-5 Soldering Profile

8.2 General Operating Conditions

(V_{DD}-V_{SS} = 2.5 ~ 5.5V, T_A = 25°C, HCLK = 48 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	˚C	
V_{DD}	Operation voltage	2.5	-	5.5	V	
AVDD[*1]	Analog operation voltage	V_{DD}			V	
V_{LDO}	LDO output voltage	-	1.8	-		
V_{BG}	Band-gap voltage	1.10	1.21	1.30	V	
T_{VBG_ADC}[*3]	ADC sampling time when reading the band-gap voltage	10	-	-	µS	
C_{LDO}[*2]	LDO output capacitor on each pin	2.2			µF	
R_{ESR}[*3]	ESR of C_{LDO} output capacitor	-	-	0.5	Ω	
I_{RUSH}[*3]	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	100	-	mA	
E_{RUSH}[*3]	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	-	3.96	-	µC	V_{DD} = 1.8 V, T_A = 25 °C

Note:

1. It is recommended to power V_{DD} and AV_{DD} from the same source. A maximum difference of 0.3 V between V_{DD} and AV_{DD} can be tolerated during power-on and power-off operation .
2. To ensure stability, an external 2.2 µF output capacitor, C_{LDO} must be connected between the LDO_CAP pin and the closest GND pin of the device. Solid tantalum and multilayer ceramic capacitors are suitable as output capacitor. Additional 100 nF bypass capacitor between LDO_CAP pin and the closest GND pin of the device helps decrease output noise and improves the load transient response.
3. Guaranteed by design, not tested in production.

Table 8.2-1 General Operating Conditions

8.3 DC Electrical Characteristics

8.3.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in condition and table below to inform test characterization result.

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for V_{DD} = 5.5V and maximum ambient temperature (TA), and the typical values for TA= 25 °C and V_{DD} = 2.5 ~ 5.5 V unless otherwise specified.
- $V_{DD} = AV_{DD}$
- When the peripherals are enabled HCLK is the system clock, fPCLK0, 1 = fHCLK.
- Program run CoreMark® code in Flash.

Symbol	Conditions	HCLK	F_{HCLK}	Typ [*1]	Max[*1][*2]			Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_OP}	Normal run mode, executed from Flash, all peripherals disable HIRC, PLL, HXT or or LIRC clock	PLL (HIRC/2)	72 MHz	20.8	23.9	24.6	25.2	mA
		HIRC	48 MHz	12.5	14.4	15	15.5	
		HXT	24 MHz	9.2	10.6	11.1	11.6	
		HIRC/4	12 MHz	4.3	5	5.4	5.9	
		HIRC/12	4 MHz	2.5	2.9	3.3	3.7	
		HIRC/2/12	2 MHz	2	2.3	2.7	3.2	
		LXT	32.768 kHz	0.1	0.1	0.5	0.9	
		LIRC	10 kHz	0.1	0.2	0.5	09	
	Normal run mode, executed from Flash, all peripherals enable HIRC, PLL, HXT or LIRC clock	PLL (HIRC24)	72 MHz	36.78	42.3	43.3	44.2	
		HIRC48	48 MHz	26.51	26.5	27.4	28.1	
		HXT	24 MHz	16.26	16.3	16.9	17.5	
		HIRC48/4	12 MHz	8.68	8.7	9.2	9.7	
		HIRC48/12	4 MHz	4.69	4.7	5.1	5.6	
		HIRC24/12	2 MHz	3.66	3.7	4.1	4.6	
		LXT	32.768 kHz	0.14	0.1	0.5	0.9	
		LIRC	10 kHz	0.15	0.1	0.5	0.9	

Notes:

1. When analog peripheral blocks such as POR, LVR, USB, ADC, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-1 Current Consumption in Normal Run Mode

Symbol	Conditions	HCLK	F_{HCLK}	Typ [*1]	Max[*1][*2]			Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_IDLE}	Idle mode, all peripherals disable HIRC, PLL, HXT or LIRC clock	PLL (HIRC/2)	72 MHz	6.87	7.9	8.4	8.9	mA
		HIRC48	48 MHz	3.21	3.7	4.1	4.6	
		HXT	24 MHz	4.58	5.3	5.6	6.1	
		HIRC48/4	12 MHz	1.99	2.3	2.7	3.1	
		HIRC48/12	4 MHz	1.71	2	2.3	2.8	
		HIRC/2/12	2 MHz	1.6	1.8	2.2	2.7	
		LXT	32.768 kHz	0.1	0.2	0.5	0.9	
		LIRC	10 kHz	0.1	0.2	0.5	0.9	
	Idle mode, all peripherals enable HIRC, PLL, HXT or LIRC clock	PLL (HIRC/2)	72 MHz	23.7	27.3	28.3	29	
		HIRC48	48 MHz	16.3	17.1	17.7	16.3	
		HXT	24 MHz	11.5	12.1	12.6	11.5	
		HIRC48/4	12 MHz	5.7	6.2	6.7	5.7	
		HIRC48/12	4 MHz	3.3	3.7	4.2	3.3	
		HIRC/2/12	2 MHz	2.7	3.1	3.5	2.7	
		LXT	32.768 kHz	0.11	0.2	0.5	0.9	
		LIRC	10 kHz	0.10	0.2	0.5	0.9	

Notes:

1. When analog peripheral blocks such as USB, ADC, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-2 Current Consumption in Idle Mode

Symbol	Test Conditions	LXT[*1] 32.768 kHz	LIRC 10 kHz	Typ[*2]	Max[*3][*4]			Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_PD}	Power-down mode, all peripherals disable	-	-	9.69	22.2	350.2	761.3	µA
	Power-down mode, all peripherals disable	-	V	10.81	23.8	351.9	772.7	
	Power-down mode, all peripherals disable	V	-	12.71	25.8	354.2	780.4	
	Power-down mode, all peripherals disable	V	V	13.65	27.1	355.7	784.1	
	Power-down mode, all peripherals disable Except WDT/Timer	-	V	11.29	24.6	353.3	783.8	
	Power-down mode, all peripherals disable Except WDT/Timer/UART	V	-	13.96	27.4	357.1	788.9	
	Power-down mode, all peripherals disable Except WDT/Timer/UART	V	V	14.81	28.5	358.1	791.2	

Notes:

1. Crystal used: AURUM XF66RU000032C0 with a C_L of 20 pF for L7 gain level.
2. V_{DD} = AV_{DD} = V_{BAT} = 3.3V, LVR17 enabled, POR disabled and BOD disabled.
3. Based on characterization, not tested in production unless otherwise specified.
4. When analog peripheral blocks such as USB, ADC and are ON, an additional power consumption should be considered.
5. Based on characterization, tested in production.

Table 8.3-3 Chip Current Consumption in Power-down Mode

8.3.2 On-Chip Peripheral Current Consumption

- The typical values for T_A= 25 °C and V_{DD} = AV_{DD} = 5V unless otherwise specified.
- All GPIO pins are set as output high of push pull mode without multi-function.
- HCLK is the system clock, f_{HCLK} = 48 MHz, $f_{PCLK0, 1}$ = f_{HCLK}.
- The result value is calculated by measuring the difference of current consumption between all peripherals clocked off and only one peripheral clocked on

Peripheral	I_{DD}[*1]	Unit
PDMA	647	
ISP	0	
CRC	90	
FMCIDLE	1452	
GPA	227	
GPB	303	
GPC	189	
GPD	122	
GPF	197	
WDT	374	
TMR0	511	
TMR1	489	
TMR2	467	
TMR3	462	
CLKO	62	uA
I2C0	287	
I2C1	261	
SPI0	726	
SPI1	713	
UART0	720	
UART1	734	
BPWM0	374	
BPWM1	389	
BPWM2	391	
BPWM3	374	
USBD	1206	
ADC	616	
LLSI0	457	
LLSI1	450	
LLSI2	439	

LLSI3	417	
LLSI4	448	
LLSI5	462	
LLSI6	443	
LLSI7	454	
LLSI8	431	
LLSI9	419	

Notes:
1. Guaranteed by characterization results, not tested in production.
2. When the ADC is turned on, add an additional power consumption per ADC for the analog part.
3. When the USB is turned on, add an additional power consumption per USB for the analog part.

Table 8.3-4 Peripheral Current Consumption

8.3.3 Wakeup Time from Low-Power Modes

The wakeup times given in Table 8.3-5 is measured on a wakeup phase with a 48 MHz HIRC oscillator.

Symbol	Parameter	Typ	Max	Unit
t_{WU_IDLE}	Wakeup from IDLE mode	-	10	cycles
t_{WU_NPD}[*1][*2]	Wakeup from normal Power-down mode	-	84.09	us

Notes:
1. Based on test during characterization, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.

Table 8.3-5 Low-power Mode Wake-up Timings

8.3.4 I/O Current Injection Characteristics

In general, I/O current injection due to external voltages below V_{SS} or above V_{DD} should be avoided

during normal product operation. However, the analog compoenent of the MCU is most likely to be affected by the injection current , but it is not easily clarified when abnormal injection accidentally happens. It is recommended to add a Schottky diode (pin to ground or pin to V_{DD}) to pins that include analog function which may potentially injection currents.

Symbol	Parameter	Negative Injection	Positive Injection	Unit	Test Condition
$I_{INJ(PIN)}$	Injected current by a I/O Pin	-0	0	mA	Injected current on nReset pins
		-0	0		Injected current on PF2~PF5, PA10, PA11 and PB0~PB15 for analog input function
		-5	+5		Injected current on any other I/O except analog input pin

Table 8.3-6 I/O Current Injection Characteristics

8.3.5 I/O DC Characteristics

8.3.5.1 *PIN Input Characteristics*

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low voltage (Schmitt trigger)	0	-	$0.3*V_{DD}$	V	
	Input low voltage (TTL trigger)	0	-	0.8		V_{DD} = 4.5 V
		0	-	0.7		V_{DD} = 2.7 V
		0	-	0.5		V_{DD} = 2.5 V
V_{IH}	Input high voltage (Schmitt trigger)	$0.7*V_{DD}$	-	V_{DD}	V	
	Input high voltage (TTL trigger)	2	-	V_{DD}		V_{DD} = 5.5 V
		1.5	-	V_{DD}		V_{DD} = 3.3 V
		1.2	-	V_{DD}		V_{DD} = 2.5 V
V_{HY}[*1]	Hysteresis voltage of schmitt input	-	$0.2*V_{DD}$	-	V	
I_{LK}[*2]	Input leakage current	-1	-	1	µA	$V_{SS} < V_{IN} < V_{DD}$, Open-drain or input only mode
		-1	-	1		$V_{DD} < V_{IN} < 5$ V, Open-drain or input only mode on any other 5v tolerance pins
R_{PU}[*1]	Pull up resistor	66.96	78.5	249	kΩ	VDD=5.5V

Notes:
1. Guaranteed by characterization result, not tested in production.
2. Leakage could be higher than the maximum value, if abnormal injection happens.

Table 8.3-7 I/O input Characteristics

8.3.5.2 *I/O Output Characteristics*

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions

I_{SR}[*1] [*2]	Source current for quasi-bidirectional mode and high level	-	-109.7	-	µA	V_{DD} = 4.5 V V_{IN}=(V_{DD}-0.4) V
		-	-67.4	-	µA	V_{DD} = 2.7 V V_{IN}=(V_{DD}-0.4) V
		-	-61.4	-	µA	V_{DD} = 2.5 V V_{IN}=(V_{DD}-0.4) V
	Source current for push-pull mode and high level	-	-7.8	-	mA	V_{DD} = 4.5 V V_{IN}=(V_{DD}-0.4) V
		-	-4.7	-	mA	V_{DD} = 2.7 V V_{IN}=(V_{DD}-0.4) V
		-	-4.3	-	mA	V_{DD} = 2.5 V V_{IN}=(V_{DD}-0.4) V
I_{SK}[*1] [*2]	Sink current for push-pull mode and low level	-	13.8	-	mA	V_{DD} = 4.5 V V_{IN}= 0.4 V
		-	8.5	-	mA	V_{DD} = 2.7 V V_{IN}= 0.4 V
		-	7.8	-	mA	V_{DD} = 2.5 V V_{IN}= 0.4 V
I_{SK}[*1] [*2]	High-Sink current for push-pull mode and low level(PA.0/PA.1/PA2/PA.3/ PA.5/PA.6/PA.7/PF.2/PF.15)	-	47.1	-	mA	V_{DD} = 4.5 V V_{IN}= 0.4 V
		-	29.3	-	mA	V_{DD} = 2.7 V V_{IN}= 0.4 V
		-	27.0	-	mA	V_{DD} = 2.5 V V_{IN}= 0.4 V
C_{IO}[*1]	I/O pin capacitance	-	5	-	pF	

Notes:

1. Guaranteed by characterization result, not tested in production.
2. The I_{SR} and I_{SK} must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.

Table 8.3-8 I/O Output Characteristics

8.3.5.3 *nRESET Input Characteristics*

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{ILR}	Negative going threshold, nRESET	-	-	0.3*V_{DD}	V	

V_{IHR}	Positive going threshold, nRESET	$0.7*V_{DD}$	-	-	V	
R_{RST}[*1]	Internal nRESET pull up resistor	35.36	42.2	125.1	kΩ	VDD=2.5V ~ 5.5V
t_{FR}[*1]	nRESET input filtered pulse time	-	32	-	µS	Normal run and Idle mode
		-	179	-		Power-down mode
Notes: 1. Guaranteed by characterization result, not tested in production. 2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.						

Table 8.3-9 nRESET Input Characteristics

8.4 AC Electrical Characteristics

8.4.1 48 MHz Internal High Speed RC Oscillator (HIRC)

The 48 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.5	-	5.5	V	
f_{HRC}	Oscillator frequnecy	47.52	48	48.48	MHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-1	-	1	%	T_A = 25 °C, V_{DD} = 3.3V
		-2[*1]	-	2[*1]	%	T_A = -40°C ~ +105 °C, V_{DD} = 2.5 ~ 5.5V
		-0.25	-	+0.25	%	T_A = -40°C ~ +105°C, V_{DD} = 2.5 ~ 5.5V Auto trimmed by LXT
I_{HRC}[*1]	Operating current	-	500	-	µA	
T_S[*2]	Stable time	-	-	5	µS	T_A = -40°C ~ +105 °C, V_{DD} = 2.5 ~ 5.5V

Notes:
1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design.

Table 8.4-148 MHz Internal High Speed RC Oscillator(HIRC) Characteristics

8.4.2 10 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{DD}	Operating voltage	2.5	-	5.5	V	
F_{LRC} [*2]	Oscillator frequnecy	-	10	-	kHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge Operating current	-40	-	40	%	T_A=-40~105°C VDD=2.5V~5.5V Without software calibration
		-	-	1.4	µA	V_{DD} = 3.3V
T_S	Stable time	-	100	-	µS	T_A=-40~105°C VDD=2.5V~5.5V

Table 8.4-238.4 kHz Internal Low Speed RC Oscillator(LIRC) Characteristics

8.4.3 External 4~24 MHz High Speed Crystal/Ceramic Resonator (HXT) Characteristics

The high-speed external (HXT) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the XT1_IN and XT1_Out pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
V_{DD}	Operating voltage	2.5	-	5.5	V	
R_f	Internal feedback resister	-	250	-	kΩ	
f_{HXT}	Oscillator frequency	4	-	24	MHz	
I_{HXT}	Current consumption (Crystal type)	-	0.3	1	mA	4 MHz, Gain = L0, C_L = 12.5 pF
		-	1	4		12 MHz, Gain = L1, C_L = 12.5 pF
		-	1.5	6.7		16 MHz, Gain = L2, C_L = 12.5 pF
		-	2.2	9		24 MHz, Gain = L3, C_L = 12.5 pF
I_{HXT}	Current consumption (Resonator type)	-	0.45	2	mA	4 MHz, Gain = L0, C_L = 30 pF
		-	0.8	3.2		12 MHz, Gain = L1, C_L = 20 pF
		-	1.5	8		16 MHz, Gain = L2, C_L = 10 pF
		-	2	9		24 MHz, Gain = L3, C_L = 10 pF
T_S	Stable time (Crystal type)	-	4.5	8.5	mS	4 MHz, Gain = L0, C_L = 12.5 pF
		-	3	3.5		12 MHz, Gain = L1, C_L = 12.5 pF
		-	2.5	2.8		16 MHz, Gain = L2, C_L = 12.5 pF
		--	1.5	2		24 MHz, Gain = L3, C_L = 12.5 pF
T_S	Stable time (Resonator type)	-	1.04	1.1	mS	4 MHz, Gain = L0, C_L = 30 pF
		-	0.35	0.4		12 MHz, Gain = L1, C_L = 20 pF
		-	0.26	0.3		16 MHz, Gain = L2, C_L = 10 pF
		--	0.21	0.25		24 MHz, Gain = L3, C_L = 10 pF
Du_{HXT}	Duty cycle	40	-	70	%	
V_{PP}	Swing Amplitude	0.3*V_{DD}	50	70	V	

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
Notes: 1. Guaranteed by characterization, not tested in production.						

Table 8.4-3 External 4~32 MHz High Speed Crystal (HXT) Oscillator

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
Rs	Equivalent series resisotr(ESR) (Crystal type)	-	-	150	Ω	Crystal at 4 MHz, C_L = 12.5 pF, Gain = L0
		-	-	120		Crystal at 12 MHz, C_L = 12.5 pF, Gain = L1
		-	-	100		Crystal at 16 MHz, C_L = 12.5 pF, Gain = L2
		-	-	80		Crystal at 24 MHz, C_L = 12.5 pF, Gain = L3
	Equivalent series resisotr(ESR) (Resonator type)	-	-	40		Ceramic Resonator at 4 MHz, C_L = 30 pF, Gain = L0
		-	-	20		Ceramic Resonator at 12 MHz, C_L = 20 pF, Gain = L1
		-	-	60		Ceramic Resonator at 16 MHz, C_L = 10 pF, Gain = L2
		-	-	60		Ceramic Resonator at 24 MHz, C_L = 10 pF, Gain = L3

Notes:

1. Guaranteed by characterization, not tested in production.
2. Safety factor (S_f) must be higher than 5 for HXT to determine the oscillator safe operation during the application life. If Safety factor isn't enough, the HXT gain need be changed to higher driving level.

$$S_f = \frac{-R}{Crystal\ ESR} = \frac{R_{ADD} + R_S}{R_S}$$

R_{ADD}: The value of smallest series resistance preventing the oscillator from starting up successfully. This resistance is only used to measure Safety factor (S_f) of crystal in engineer stage, not for mass produciton.

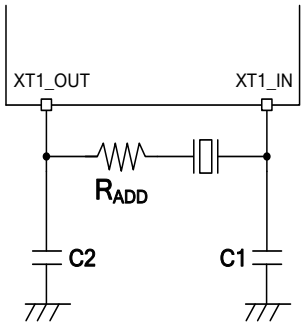


Table 8.4-4 External 4~32 MHz High Speed Crystal Characteristics

8.4.3.1 *Typical Crystal Application Circuits*

For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 10 pF ~ 20 pF

range, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. The crystal manufacturer typically specifies a load capacitance which is the series combination of C1 and C2. PCB and MCU pin capacitance must be included (8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

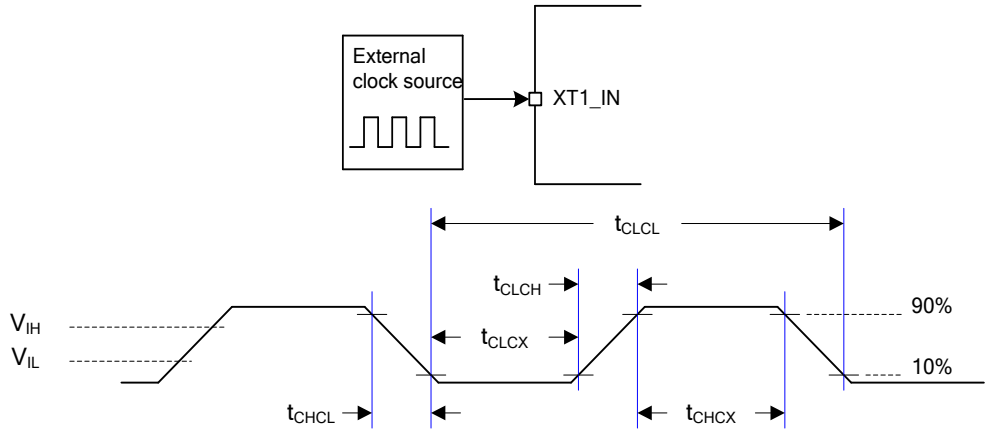
CRYSTAL	C1	C2	R1
4 MHz ~ 24 MHz	10 ~ 20 pF	10 ~ 20 pF	without

Table 8.4-5 Typical Crystal Application Circuit

8.4.4 External 4~24 MHz High Speed Clock Input Signal Characteristics

For clock input mode the HXT oscillator is switched off and XT1_IN is a standard input pin to receive external clock. The external clock signal needs to follow Table 8.4-6. The characteristics result from tests performed uses a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{HXT_ext}	External user clock source frequency	1	-	24	MHz	
t_{CHCX}	Clock high time	8	-	-	nS	
t_{CLCX}	Clock low time	8	-	-	nS	
t_{CLCH}	Clock rise time	-	-	10	nS	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	10	nS	High (90%) to low level (10%) fall time
Du_{E_HXT}	Duty cycle	40	-	60	%	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
V_{IL}	Input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Note: Guaranteed by characterization, not tested in production.

Table 8.4-6 External 4~24 MHz High Speed Clock Input Signal

8.4.5 External 32.768 kHz Low Speed Crystal/Ceramic Resonator (LXT) Characteristics

The low-speed external (LXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the X32_OUT and X32_IN pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{DD}	Operation voltage	2.5	-	5.5	V	
T_{LXT}	Temperature range	-40	-	105	°C	
R_f	Internal feedback resistor	-	6	-	MΩ	
F_{LXT}	Oscillator frequency		32.768		kHz	
I_{LXT}	Current consumption	-	600	4400	nA	ESR=35 kΩ, C_L = 12.5 pF, Gain = L0
		-	750	4600		ESR=35 kΩ, C_L = 12.5 pF, Gain = L1
		-	800	4800		ESR=35 kΩ, C_L = 12.5 pF, Gain = L2
		-	950	5200		ESR=70 kΩ, C_L = 12.5 pF, Gain = L3
		-	1050	5400		ESR=70 kΩ, C_L = 12.5 pF, Gain = L4
		-	1400	5600		ESR=70 kΩ, C_L = 12.5 pF, Gain = L5
		-	1600	6000		ESR=90 kΩ, C_L = 12.5 pF, Gain = L6
		-	1900	6600		ESR=90 kΩ, C_L = 12.5 pF, Gain = L7
Ts_{LXT}	Stable time	-	1	-	S	
Du_{LXT}	Duty cycle	30	-	70	%	
V_{pp}	Peak-to-peak amplitude	0.35	0.5	-	V	

Notes:
1. Guaranteed by characterization, not tested in production.

Table 8.4-7 External 32.768 kHz Low Speed Crystal (LXT) Oscillator

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Rs	Equivalnet Series Resisotr(ESR)	-	35	90	kΩ	Crystal @32.768 kHz

Table 8.4-8 External 32.768 kHz Low Speed Crystal Characteristics

8.4.5.1 *Typical Crystal Application Circuits*

CRYSTAL	C1	C2	R1

32.768 kHz, ESR < 70 KΩ	5 ~ 20 pF	5 ~ 20 pF	without

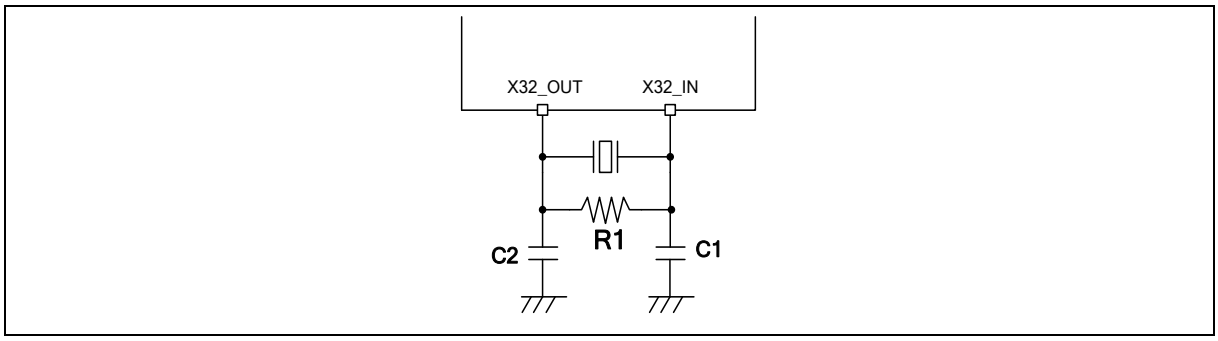
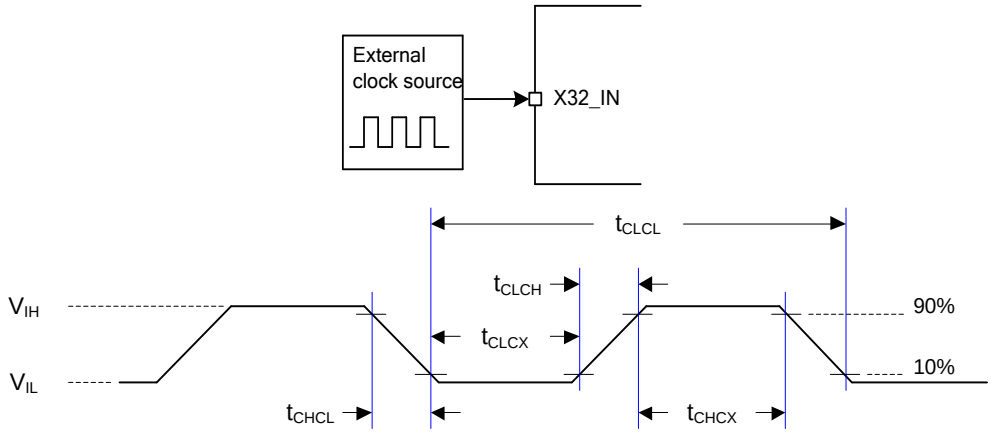


Figure 8.4-1 Typical 32.768 kHz Crystal Application Circuit

8.4.6 External 32.768 kHz Low Speed Clock Input Signal Characteristics

For clock input mode the LXT oscillator is switched off and X32_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{LXT_ext}	External clock source frequency	-	32.768	-	kHz	
t_{CHCX}	Clock high time	450	-	-	nS	
t_{CLCX}	Clock low time	450	-	-	nS	
t_{CLCH}	Clock rise time	-	-	50	nS	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	50	nS	High (90%) to low level (10%) fall time
Du_{E_LXT}	Duty cycle	30	-	70	%	
Xin_VIH	LXT input pin input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
Xin_VIL	LXT input pin input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Note: Guaranteed by design, not tested in production

Table 8.4-9 External 32.768 kHz Low Speed Clock Input Signal

8.4.7 PLL Characteristics

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
f_{PLL_in}	PLL input clock	4	-	24	MHz	
f_{PLL_OUT}	PLL multiplier output clock	16	-	144	MHz	
f_{PLL_REF}	PLL reference clock	4	-	8	MHz	
f_{PLL_VCO}	PLL voltage controlled oscillator	200	-	480	MHz	
T_L	PLL locking time	-	-	500	µS	
Jitter[*2]	Cycle-to-cycle Jitter	500	-	-	pS	
I_{DD}	Power consumption	-	-	16	mA	VDD=5.5V @ f_{PLL_VCO} = 288 MHz

Notes:

1.Guaranteed by characterization, not tested in production.

2.Guaranteed by design, not tested in production.

Table 8.4-10 PLL Characteristics

8.4.8 I/O AC Characteristics

Symbol	Parameter	Typ.	Max[*1].	Unit	Test Conditions[*2]
$t_{f(I/O)out}$	Output high (90%) to low level (10%) fall time (Normal Slew Rate)	7.0	-	nS	C_L = 30 pF, V_{DD} >= 4.5 V
		5.2	-		C_L = 10 pF, V_{DD} >= 4.5 V
		12.0	-		C_L = 30 pF, V_{DD} >= 2.7 V
		9.2	-		C_L = 10 pF, V_{DD} >= 2.7 V
		13.0	-		C_L = 30 pF, V_{DD} >= 2.5 V
		10.0	-		C_L = 10 pF, V_{DD} >= 2.5 V
	Output high (90%) to low level (10%) fall time (High Slew Rate)	4.3	-		C_L = 30 pF, V_{DD} >= 4.5 V
		3.0	-		C_L = 10 pF, V_{DD} >= 4.5 V
		6.4	-		C_L = 30 pF, V_{DD} >= 2.7 V
		4.6	-		C_L = 10 pF, V_{DD} >= 2.7 V
		7.0	-		C_L = 30 pF, V_{DD} >= 2.5 V
		4.9	-		C_L = 10 pF, V_{DD} >= 2.5 V
$t_{r(I/O)out}$	Output low (10%) to high level (90%) rise time (Normal Slew Rate)	6.1	-	nS	C_L = 30 pF, V_{DD} >= 4.5 V
		4.2	-		C_L = 10 pF, V_{DD} >= 4.5 V
		10.3	-		C_L = 30 pF, V_{DD} >= 2.7 V
		6.9	-		C_L = 10 pF, V_{DD} >= 2.7 V
		11.6	-		C_L = 30 pF, V_{DD} >= 2.5 V
		7.6	-		C_L = 10 pF, V_{DD} >= 2.5 V
	Output low (10%) to high level (90%) rise time (High Slew Rate)	4.7	-	nS	C_L = 30 pF, V_{DD} >= 4.5 V
		2.9	-		C_L = 10 pF, V_{DD} >= 4.5 V
		7.9	-		C_L = 30 pF, V_{DD} >= 2.7 V
		4.7	-		C_L = 10 pF, V_{DD} >= 2.7 V
		8.5	-		C_L = 30 pF, V_{DD} >= 2.5 V

		5.2	-		C_L = 10 pF, V_{DD} >= 2.5 V
$f_{max(I/O)out}$[*3]	I/O maximum frequency (Normal Slew Rate)	51.2	-	MHz	C_L = 30 pF, V_{DD} >= 4.5 V
		72.0	-		C_L = 10 pF, V_{DD} >= 4.5 V
		30.2	-		C_L = 30 pF, V_{DD} >= 2.7 V
		41.6	-		C_L = 10 pF, V_{DD} >= 2.7 V
		27.3	-		C_L = 30 pF, V_{DD} >= 2.5 V
		38.2	-		C_L = 10 pF, V_{DD} >= 2.5 V
	I/O maximum frequency (High Slew Rate)	74.8	-	MHz	C_L = 30 pF, V_{DD} >= 4.5 V
		115.2	-		C_L = 10 pF, V_{DD} >= 4.5 V
		46.7	-		C_L = 30 pF, V_{DD} >= 2.7 V
		72.6	-		C_L = 10 pF, V_{DD} >= 2.7 V
		43.2	-		C_L = 30 pF, V_{DD} >= 2.5 V
		67.2	-		C_L = 10 pF, V_{DD} >= 2.5 V
I_{DIO}[*4]	I/O dynamic current consumption	2.8	-	mA	C_L = 30 pF, V_{DD} = 3.3 V, $f_{(I/O)out}$ = 24 MHz
		1.2	-		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(I/O)out}$ = 24 MHz
		0.7	-		C_L = 30 pF, V_{DD} = 3.3 V, $f_{(I/O)out}$ = 6 MHz
		0.3	-		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(I/O)out}$ = 6 MHz

Notes:

1. Guaranteed by characterization result, not tested in production.
2. C_L is a external capacitive load to simulate PCB and device loading.
3. The maximum frequency is defined by $f_{max} = \frac{2}{3 \times (t_f + t_r)}$.
4. The I/O dynamic current consumption is defined by $I_{DIO} = V_{DD} \times f_{IO} \times (C_{IO} + C_L)$

Table 8.4-11 I/O AC Characteristics

8.5 Analog Characteristics

8.5.1 LDO

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	Power supply	2.5	3.3	5.5	V	
V_{LDO}	Output voltage	1.6	1.8	2.0	V	
T_A	Temperature	-40	-	105	°C	

Notes:

1.It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.

2.For ensuring power stability, a 2.2μF capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device.

3.V_{LDO} is only used to supply internal power.

8.5.2 Reset and Power Control Block Characteristics

The parameters in below table are derived from tests performed under ambient temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{POR}[*1]	POR operating current	-	-	5.5	μA	AV_{DD} = 5.5V
I_{LVR}[*1]	LVR operating current	-	0.7	1.65		V_{DD} = 5.5V
I_{BOD}[*1]	BOD operating current	-	90	150		AV_{DD} = 5.5V, Normal mode
		-	0.5	1.5		AV_{DD} = 5.5V, Low Power mode
V_{POR}	POR reset voltage	1.13	1.75	2.5	V	
	POR Hysteresis	0.1	0.24	-		
V_{LVR}	LVR reset voltage	1.5	2.0	2.4		
V_{BOD}	BOD brown-out detect voltage	2.1	2.2	2.3		BODVL = 0
		2.6	2.7	2.8		BODVL = 1
		3.6	3.7	3.8		BODVL = 2
		4.4	4.5	4.6		BODVL = 3
V_{HYSn}	BOD Hysteresis	50	100	110	mV	
T_{LVR_SU}[*1]	LVR startup time	-	150	250	μS	-
T_{LVR_RE}[*1]	LVR respond time	-	90	100		-
T_{BOD_SU}[*1]	BOD startup time	-	1000	1200		-
T_{BOD_RE}[*1]	BOD respond time	-	60	100		Normal mode
		-	-	15000		Low Power mode
R_VDD_R[*1]	V_{DD} rise time rate	10	-	-	μS/V	POR Enabled
R_VDD_F[*1]	V_{DD} fall time rate	10000	-	-		POR Enabled
		2000	-	-		LVR Enabled

		500	-	-		BOD 2.2V Enabled, Normal mode
		150	-	-		BOD 2.7V Enabled, Normal mode
		60	-	-		BOD 3.7 Enabled, Normal mode
		40	-	-		BOD 4.5V Enabled, Normal mode
		75			mS/V	BOD 2.2V Enabled, Low Power mode
		25				BOD 2.7V Enabled, Low Power mode
		9				BOD 3.7 Enabled, Low Power mode
		6				BOD 4.5V Enabled, Low Power mode
Notes: 1.Guaranteed by characterization, not tested in production. 2.Design for specified applcaiton.						

Table 8.5-1 Reset and Power Control Unit

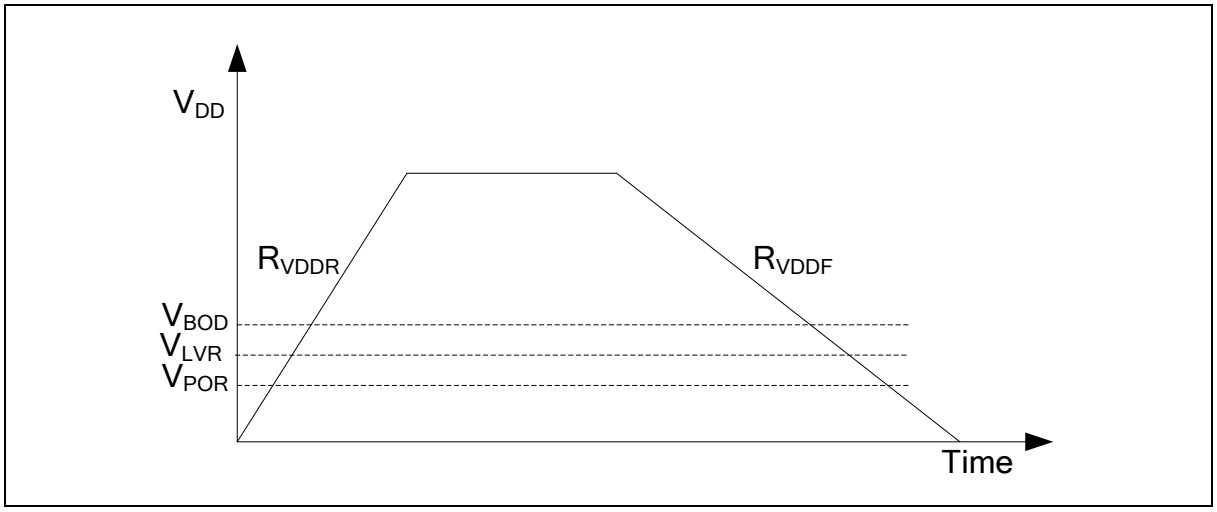


Figure 8.5-1 Power Ramp Up/Down Condition

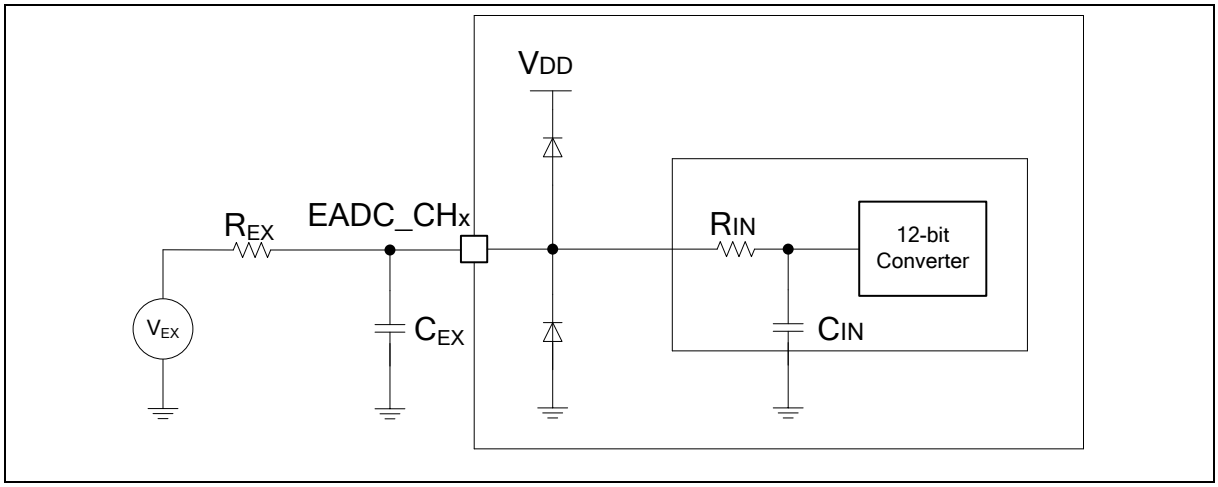
8.5.3 12-bit SAR Analog To Digital Converter (ADC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
AV_{DD}	Analog operating voltage	3.0	-	5.5	V	$V_{DD} = AV_{DD}$
V_{REF}	Reference voltage	3.0	-	AV_{DD}	V	
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
I_{ADC}[*1]	ADC Operating current (AV_{DD} + V_{REF} current)	-	-	4	mA	$AV_{DD} = V_{DD} = V_{REF}$ = 5 V F_{ADC} = 16 MHz $T_{CONV} = 16 * T_{ADC}$
N_R	Resolution	12			Bit	
F_{ADC}[*1] $1/T_{ADC}$	ADC Clock frequency	4	-	16	MHz	
T_{SMP}	Sampling Time	4	-	11	$1/F_{ADC}$	T_{SMP} = (SMPTSEL(ADC_ADCR[18:16]) + 4) * T_{ADC}
T_{CONV}	Conversion time	16	-	23	$1/F_{ADC}$	$T_{CONV} = T_{SMP} + 12 * T_{ADC}$
F_{SPS}[*1]	Sampling Rate	222	-	800	KSPS	FSPS = FADC / TCONV 800ksps = 16M/20, 222ksps = 4M/18
T_{EN}	Enable to ready time	5	-	-	µS	
INL[*1]	Integral Non-Linearity Error	-2	-	+2	LSB	$V_{REF} = AV_{DD}$,
DNL[*1]	Differential Non-Linearity Error	-1	-	+2	LSB	$V_{REF} = AV_{DD}$,
E_G[*1]	Gain error	-4	-2	+4	LSB	$V_{REF} = AV_{DD}$,
E_O[*1]$_T$	Offset error	-4	2	+4	LSB	$V_{REF} = AV_{DD}$,
E_A[*1]	Absolute Error	-4	-	+4	LSB	$V_{REF} = AV_{DD}$,
ENOB[*1]	Effective number of bits	-	9.75	-	bits	F_{ADC} = 16 MHz $AV_{DD} = V_{DD} = V_{REF}$ = 3.3 V Input Frequency = 20 kHz T_A = 25 °C
SINAD[*1]	Signal-to-noise and distortion ratio	-	60.5	-	dB	
SNR[*1]	Signal-to-noise ratio	-	62.6	-		
THD[*1]	Total harmonic distortion	-	-64	-		
C_{IN}[*1]	Internal Capacitance	-	3.85	-	pF	
R_{IN}[*1]	Internal Switch Resistance	-	-	1.36	kΩ	
R_{EX}[*1]	External input impedance	-	-	30	kΩ	

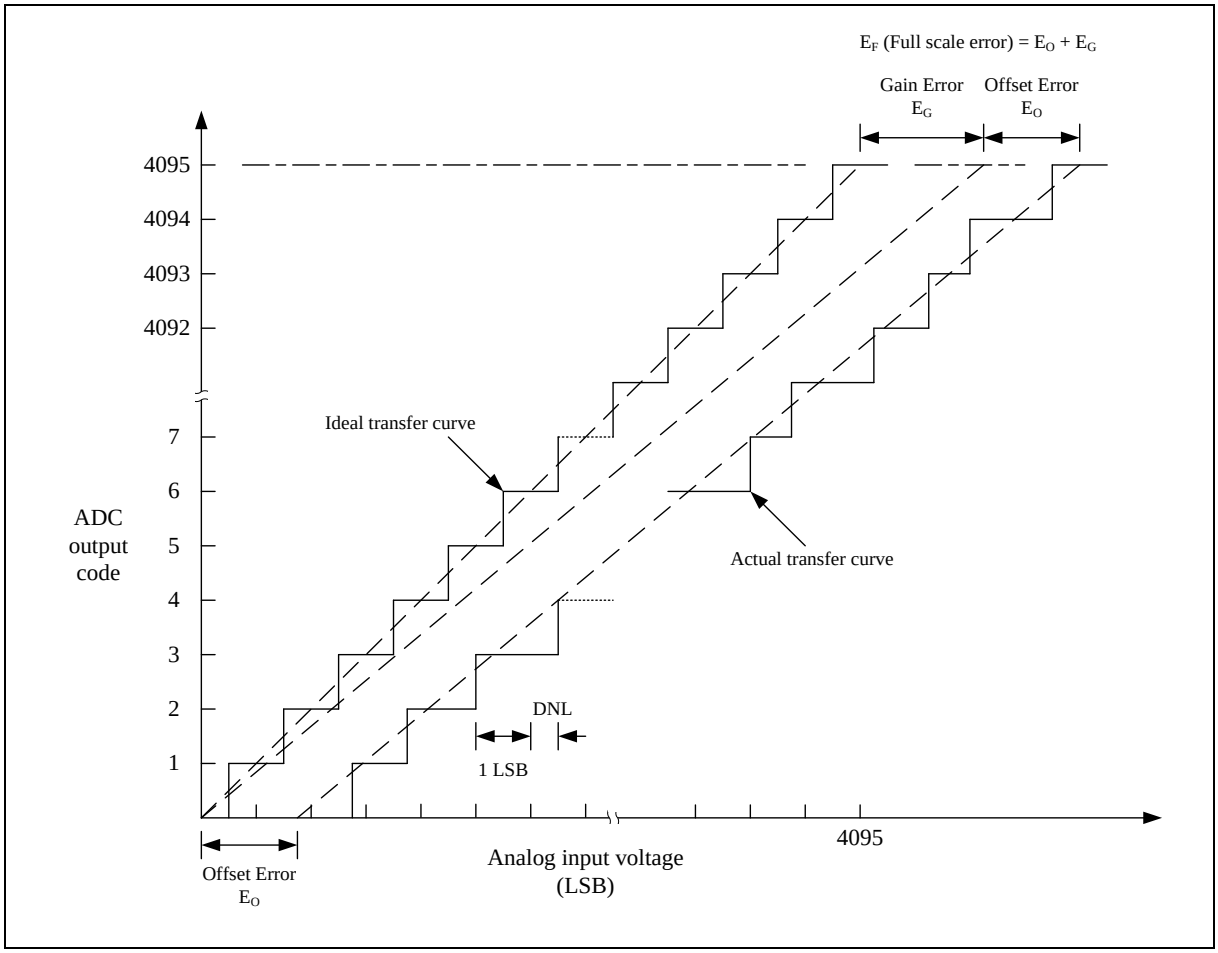
Notes:

1. Guaranteed by characterization result, not tested in production.
2. R_{EX} max formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resoluton) and k is the number of sampling clocks (T_{SMP}). C_{EX} represents the capacitance of PCB and pad and is combined with R_{EX} into a low-pass filter. Once the R_{EX} and C_{EX} values are too large, it is possible to filter the real signal and reduce the ADC accuracy.

$$R_{EX} = \frac{k}{f_{ADC} \times (C_{IN} + C_{EX}) \times \ln(2^{N+2})} - R_{IN}$$



Note: Injection current is a important topic of ADC accuracy. Injecting current on any analog input pins should be avoided to protect the conversion being performed on another analog input. It is recommended to add Schottky diodes (pin to ground and pin to power) to analog pins which may potentially inject currents.



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

8.5.4 Temperature Sensor

The maximum values are obtained for V_{DD} = 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{TEMP_OS}[*1]	Temperature sensor offset voltage	741	749	759	mV	T_A = 0°C
T_C[*1]	Temperature Coefficient	-1.64	-1.698	-1.74	mV/°C	
T_S[*2]	Stable time	-	-	2	µS	
T_{TEMP_ADC}[*1]	ADC sampling time when reading the temperature	5	-	-	µS	
I_{TEMP}[*1]	Temperature sensor operating current	-	16	30	µA	

Note:

1. Guaranteed by characterization, not tested in production
2. Guaranteed by design, not tested in production
3. V_{TEMP} (mV) = T_C (mV/°C) x Temperature (°C) + V_{TEMP_OS} (mV)

Table 8.5-2 Temperature Sensor Characteristics

8.6 Communications Characteristics

8.6.1 SPI Dynamic Characteristics

Symbol	Parameter	Specificaitons[*1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	27	MHz	4.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	15		2.7 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	13		2.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			nS	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			nS	
t_{DS}	Data input setup time	2	-	-	nS	
t_{DH}	Data input hold time	4	-	-	nS	
t_V	Data output valid time	-	-	4.1	nS	4.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	4.1	nS	2.7 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	4.1	nS	2.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
Note: Guaranteed by design.						

Table 8.6-1 SPI Master Mode Characteristics

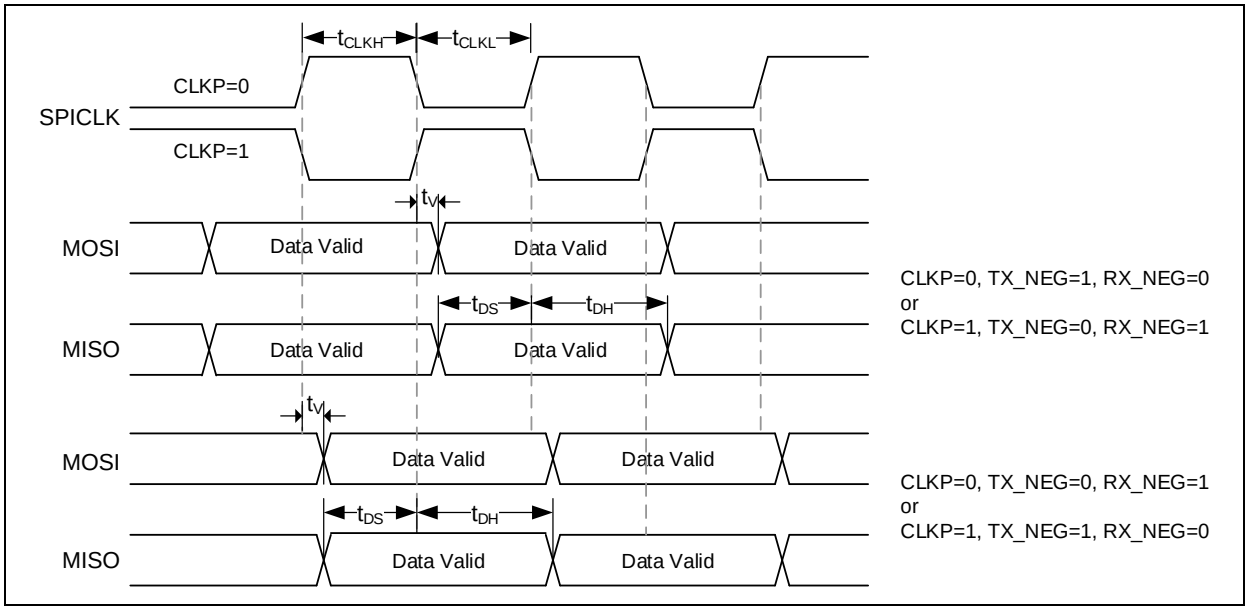


Figure 8.6-1 SPI Master Mode Timing Diagram

Symbol	Parameter	Specificaitons[*1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	12.8	MHz	4.5 V ≤ V_{DD} ≤ 5.5 V, CL = 30 pF
		-	-	9		2.7 V ≤ V_{DD} ≤ 5.5 V, CL = 30 pF
		-	-	8.3		2.5 V ≤ V_{DD} ≤ 5.5 V, CL = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			nS	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			nS	
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	nS	4.5 V ≤ V_{DD} ≤ 5.5 V, CL = 30 pF
		1 T_{SPICLK} + 3ns	-	-		2.7 V ≤ V_{DD} ≤ 5.5 V, CL = 30 pF
		1 T_{SPICLK} + 3ns	-	-		2.5 V ≤ V_{DD} ≤ 5.5 V, CL = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	nS	
t_{DS}	Data input setup time	1.5	-	-	nS	
t_{DH}	Data input hold time	3.5	-	-	nS	
t_V	Data output valid time	-	-	39	nS	4.5 V ≤ V_{DD} ≤ 5.5 V, CL = 30 pF
		-	-	55		2.7 V ≤ V_{DD} ≤ 5.5 V, CL = 30 pF
		-	-	60		2.5 V ≤ V_{DD} ≤ 5.5 V, CL = 30 pF
Note: Guaranteed by design.						

Table 8.6-2 SPI Slave Mode Characteristics

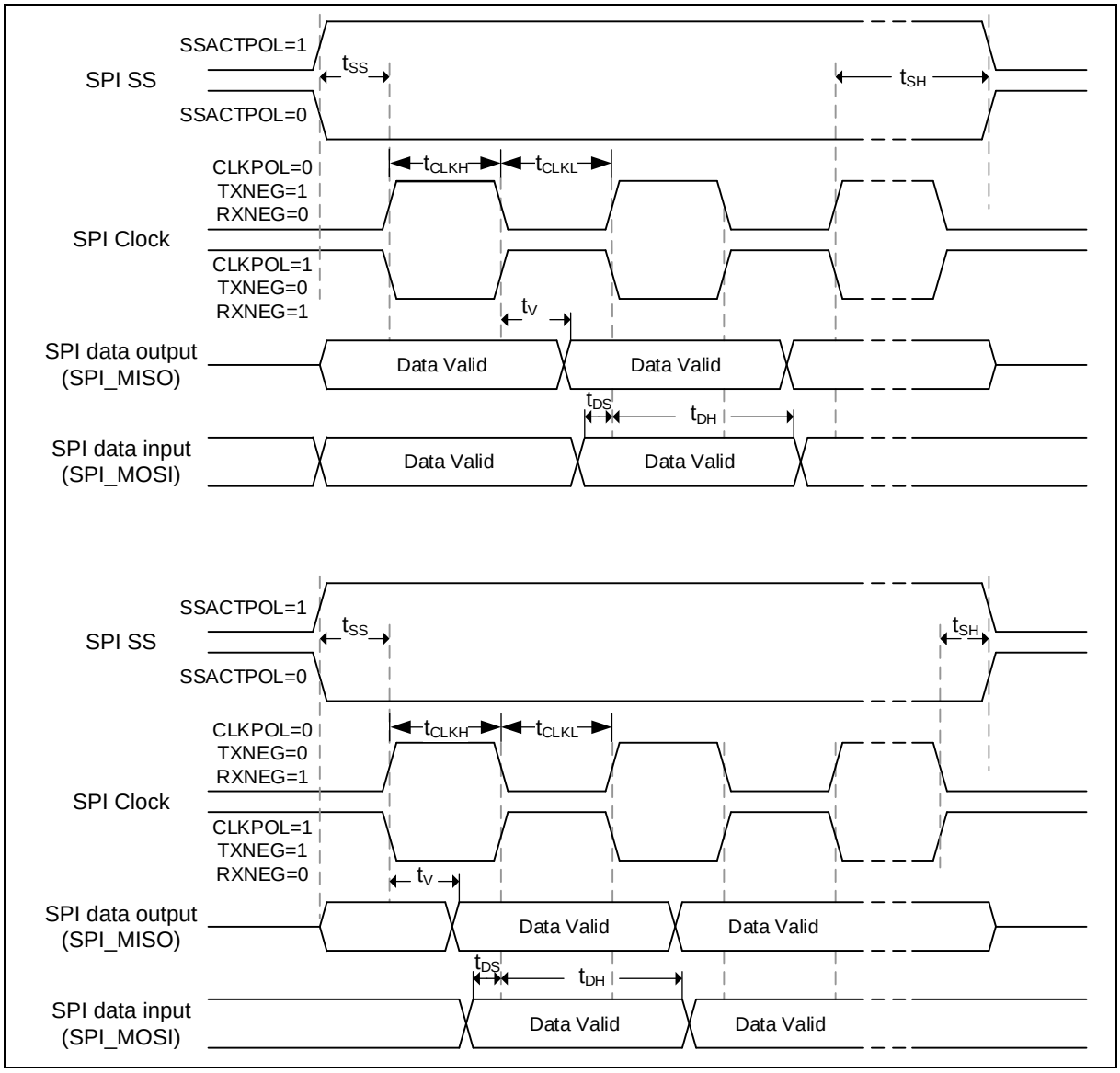


Figure 8.6-2 SPI Slave Mode Timing Diagram

8.6.2 SPI - I²S Dynamic Characteristics

Symbol	Parameter	Min [*1]	Max [*1]	Unit	Test Conditions
$t_{w(CKH)}$	I²S clock high time	80	-	nS	Master f_{PCLK} = 48 MHz, data: 24 bits, audio frequency = 128 kHz
$t_{w(CKL)}$	I²S clock low time	80	-		
$t_{v(WS)}$	WS valid time	2	6		Master mode
$t_{h(WS)}$	WS hold time	2	-		Master mode
$t_{su(WS)}$	WS setup time	24	-		Slave mode
$t_{h(WS)}$	WS hold time	0	-		Slave mode
$DuCy_{(SCK)}$	I²S slave input clock duty cycle	30	70	%	Slave mode
$t_{su(SD\_MR)}$	Data input setup time	10	-	nS	Master receiver
$t_{su(SD\_SR)}$		7	-		Slave receiver
$t_{h(SD\_MR)}$	Data input hold time	7	-		Master receiver
$t_{h(SD\_SR)}$		4	-		Slave receiver
$t_{v(SD\_ST)}$	Data output valid time	-	25		Slave transmitter (after enable edge)
$t_{h(SD\_ST)}$	Data output hold time	4	-		Slave transmitter (after enable edge)
$t_{v(SD\_MT)}$	Data output valid time	-	4		Master transmitter (after enable edge)
$t_{h(SD\_MT)}$	Data output hold time	0	-		Master transmitter (after enable edge)

Note:

1. Guaranteed by design.

Table 8.6-3 I²S Characteristics

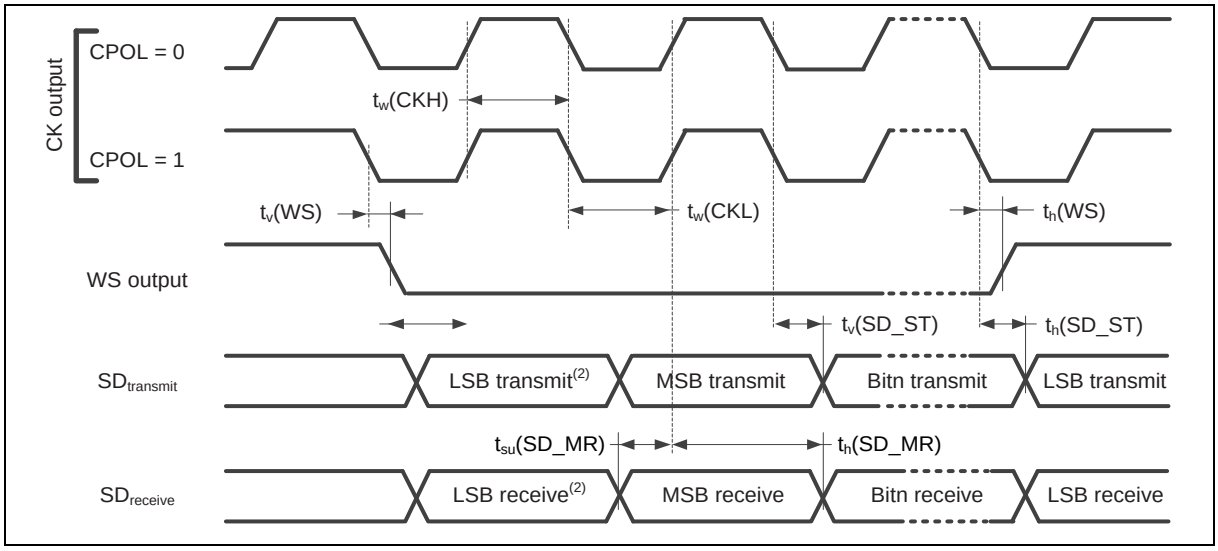


Figure 8.6-3 I²S Master Mode Timing Diagram

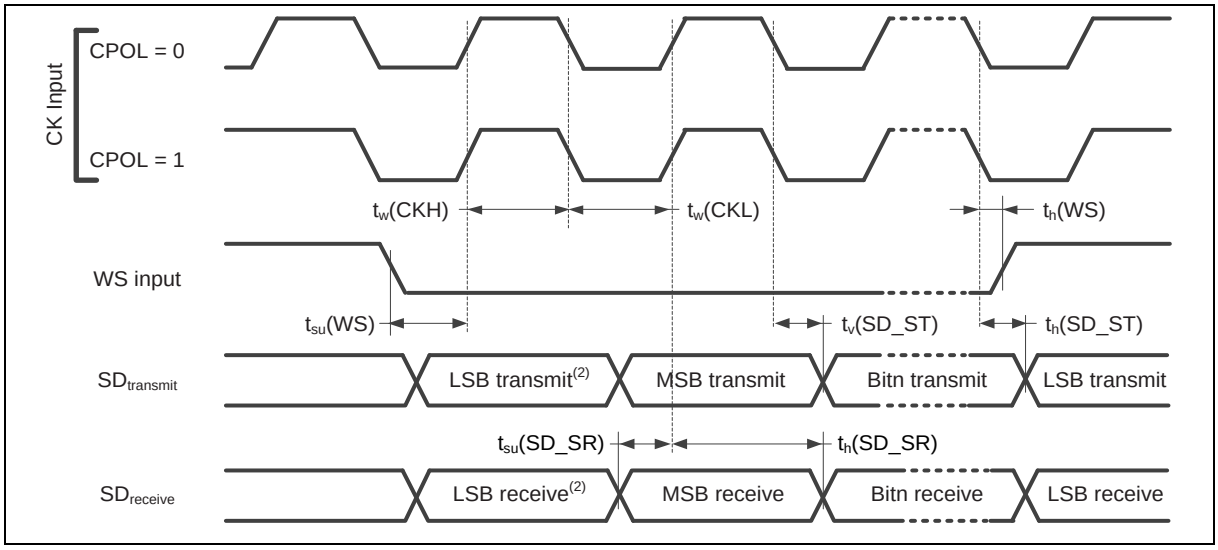


Figure 8.6-4 I²S Slave Mode Timing Diagram

8.6.3 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	μS
t_{HIGH}	SCL high period	4	-	0.6	-	μS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	μS
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	μS
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	μS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	μS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	μS
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Notes:

1. Guaranteed by characteristic, not tested in production.
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I²C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-4 I²C Characteristics

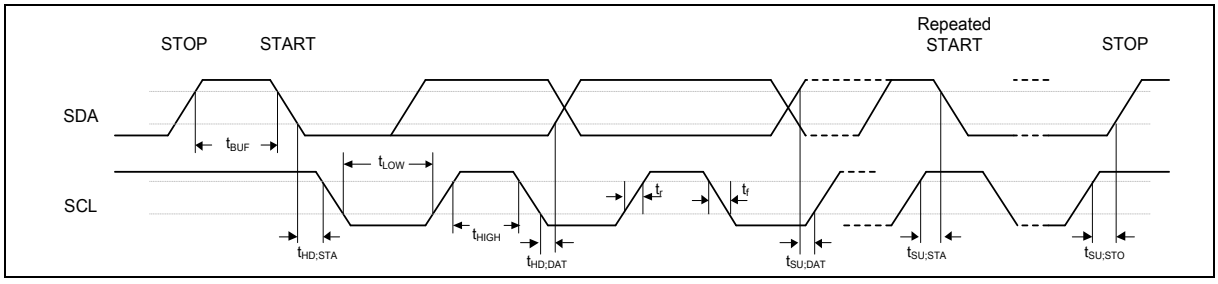


Figure 8.6-5 I²C Timing Diagram

8.6.4 USB Characteristics

8.6.4.1 *USB Full-Speed Characteristics*

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{BUS}	USB full speed transceiver operating voltage	4.4	-	5.25	V	
VDD_{33}[*2]	USB Internal power regulator output	3.0	3.3	3.6	V	
V_{IH}	Input high (driven)	2.0	-	-	V	-
V_{IL}	Input low	-	-	0.8	V	-
V_{DI}	Differential input sensitivity	0.2	-	-	V	|(USB_D+) - (USB_D-)|
V_{CM}	Differential common-mode range	0.8	-	2.5	V	Includes V_{DI} range
V_{SE}	Single-ended receiver threshold	0.8	-	2.0	V	-
	Receiver hysteresis	-	200	-	mV	-
V_{OL}	Output low (driven)	0	-	0.3	V	-
V_{OH}	Output high (driven)	2.8	-	3.6	V	-
V_{CRS}	Output signal cross voltage	1.3	-	2.0	V	-
R_{PU}	Pull-up resistor	1.19	-	1.9	kΩ	-
V_{TRM}	Termination voltage for upstream port pull-up (RPU)	3.0	-	3.6	V	
Z_{DRV}[*3]	Driver output resistance	-	10	-	Ω	Steady state drive
C_{IN}	Transceiver capacitance	-	-	26	pF	Pin to GND

Notes:

1. Guaranteed by characterization result, not tested in production.
2. To ensure stability, an external 1 μF output capacitor, 1uF external capacitor must be connected between the USB_VDD33_CAP pin and the closest GND pin of the device.
3. USB_D+ and USB_D- must be connected with external series resistors to fit USB Full-speed spec request (28 ~ 44Ω).

Table 8.6-5 USB Full-Speed Characteristics

8.6.4.2 *USB Full-Speed PHY characteristics*

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
T_{FR}	rise time	4	-	20	nS	C_L=50 pF
T_{FF}	fall time	4	-	20	nS	C_L=50 pF
T_{FRFF}	rise and fall time matching	90	-	111.11	%	$T_{FRFF} = T_{FR}/T_{FF}$

Note:

1.Guaranteed by characterization result, not tested in production.

Table 8.6-6 USB Full-Speed PHY Characteristics

8.7 Flash DC Electrical Characteristics

The devices are shipped to customers with the Flash memory erased.

Symbol	Parameter	Min[3]	Typ	Max	Unit	Test Condition
V_{FLA}[1]	Supply voltage	-	1.8	-	V	T_A = 25°C
T_{ERASE}	Page erase time	-	20	-	mS	
T_{PROG}	Program time	-	60	-	µS	
I_{DD1}	Read current	-	7	-	mA	
I_{DD2}	Program current	-	8	-	mA	
I_{DD3}	Erase current	-	12	-	mA	
N_{ENDUR}	Cycling Endurance	20,000	-	-	cycles[2]	
T_{RET}	Data retention	10	-	-	year	20 kcycle[2], T_J = 85°C
		100	-	-	year	20 kcycle[2], T_J = 25°C

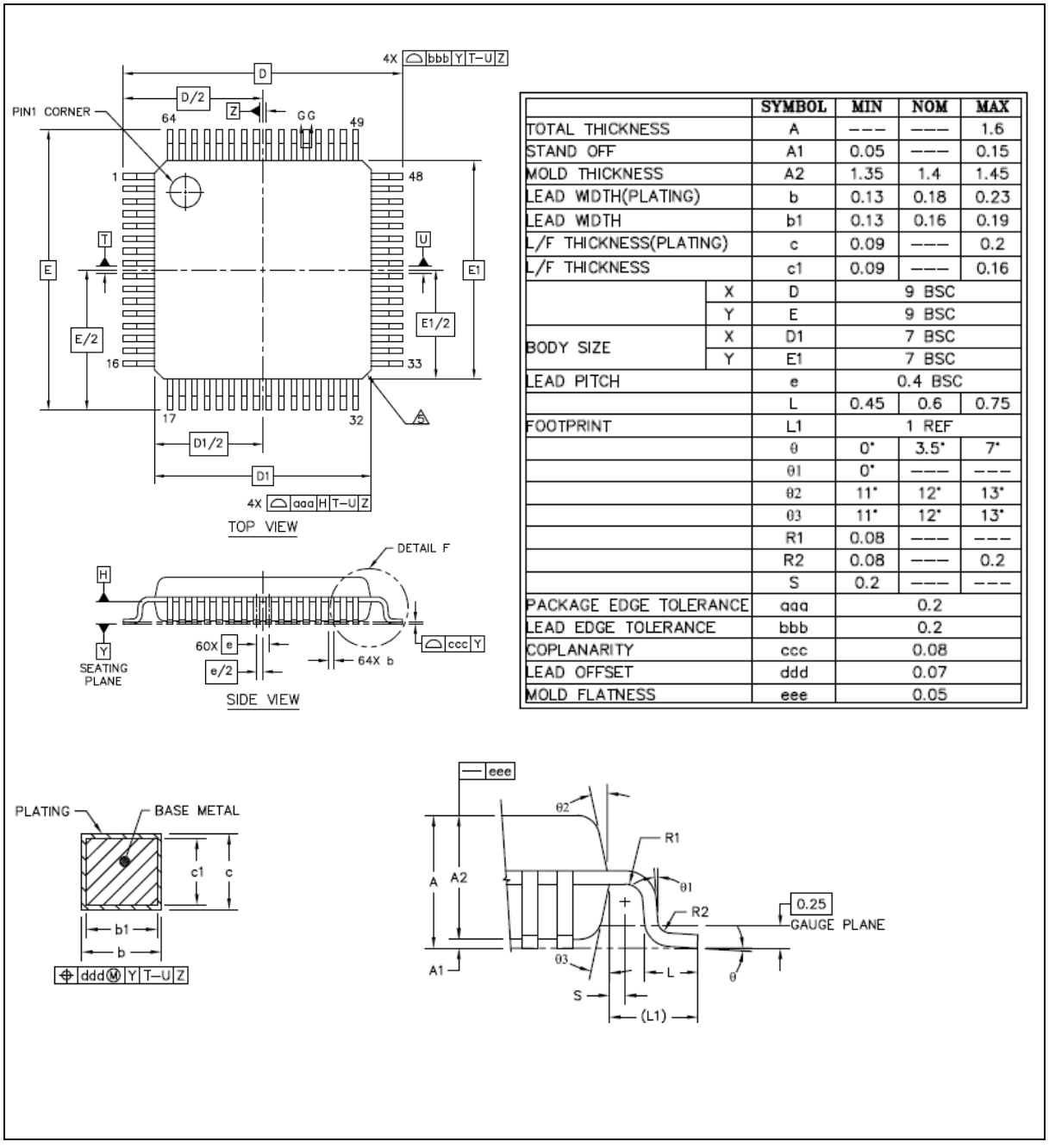
Notes:

1. V_{FLA} is source from chip internal LDO output voltage.
2. Number of program/erase cycles. The Flash data can only be programmed once at the same address after Flash erase.
3. Guaranteed by design.

Table 8.7-1 Flash Characteristics

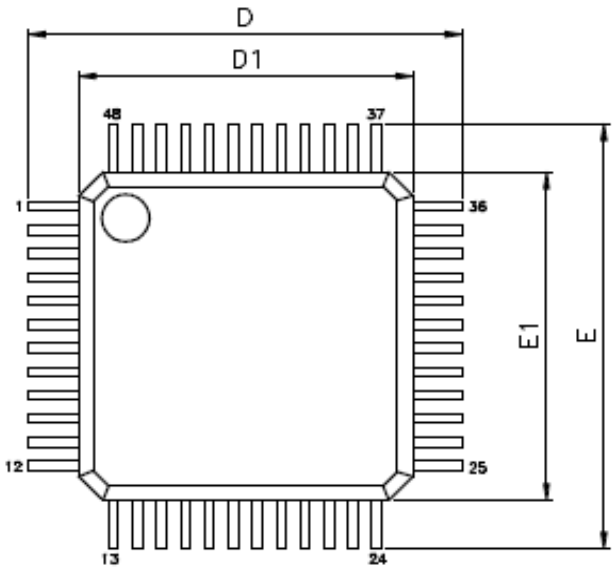
9 PACKAGE DIMENSIONS

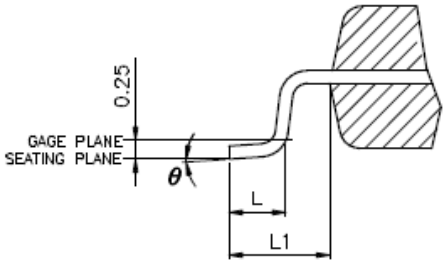
9.1 LQFP 64L (7x7x1.4 mm footprint 2.0 mm)

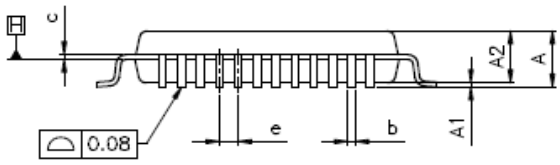


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

9.2 LQFP 48L (7x7x1.4 mm footprint 2.0 mm)



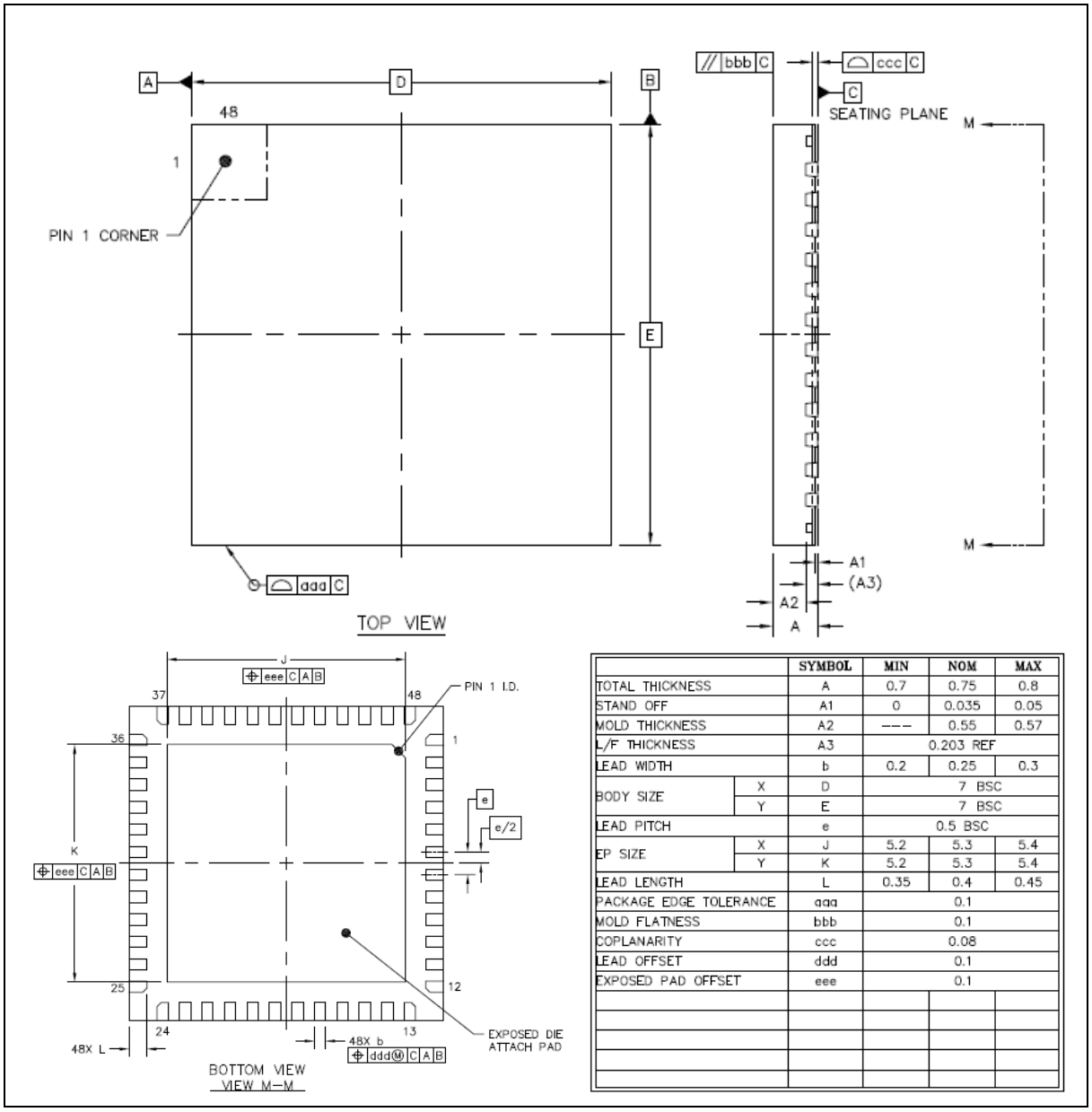




VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
S	0.20	--	--
θ	0°	3.5°	7°
θ1	0°	--	--
θ2	11°	12°	13°
θ3	11°	12°	13°

9.3 QFN 48L (7x7x0.8mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	5.2	5.3	5.4
	Y	K	5.2	5.3	5.4
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

10 ABBREVIATIONS

10.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
DAP	Debug Access Port
DES	Data Encryption Standard
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
QEI	Quadrature Encoder Interface
SD	Secure Digital
SPI	Serial Peripheral Interface

SPS	Samples per Second
TDES	Triple Data Encryption Standard
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 10.1-1 List of Abbreviations

11 REVISION HISTORY

Date	Revision	Description
2021.09.22	1.00	Initial version.
2021.11.17	1.01	1. Modified Pin 46 of LQFP48 and QFN48 from AV_{SS} to GPB11 in sections 3.2, 4.1.1.2, 4.1.1.3, 4.1.2.2, 4.1.2.3 and 4.2. 2. Changed Pin 59 of LQFP64 to NC pin in sections 3.2, 4.1.1.1, 4.1.2.1 and 4.2. 3. Fixed packaging errors in sections 9.1, 9.2 and 9.3.

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